256K x 36, 512K x 18
3.3V Synchronous ZBT™ SRAMs   *AS8C803601*
ZBT™ Feature   *AS8C801801*
3.3V I/O, Burst Counter
Pipelined Outputs

Features

- **256K x 36, 512K x 18 memory configurations**
- **Supports high performance system speed - 150MHz (3.8ns Clock-to-Data Access)**
- **ZBT™ Feature - No dead cycles between write and read cycles**
- **Internally synchronized output buffer enable eliminates the need to control $\overline{OE}$**
- **Single R/$\overline{W}$ (READ/WRITE) control pin**
- **Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications**
- **4-word burst capability (interleaved or linear)**
- **Individual byte write ($\overline{BW}_1$ - $\overline{BW}_4$) control (May tie active)**
- **Three chip enables for simple depth expansion**
- **3.3V power supply (±5%)**
- **3.3V I/O Supply (V$_{DDQ}$)**
- **Power down controlled by ZZ input**
- **Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP).**

Description

The AS8C803601/801801 are 3.3V high-speed 9,437,184 bit (9 Megabit) synchronous SRAMS. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The AS8C803601/801801 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable($\overline{CEN}$) pin allows operation of the AS8C803601/801801 to be suspended as long as necessary. All synchronous inputs are ignored when ($\overline{CEN}$)is high and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE}_1$, CE2, $\overline{CE}_2$) that allow the user to deselect the device when desired. If any one of these three are not asserted when ADV/$\overline{LD}$ is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after chip is deselected or a write is initiated.

The AS8C803601/801801 have an on-chip burst counter. In the burst mode, the AS8C803601/801801 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the $\overline{LBO}$ input pin. The $\overline{LBO}$ pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH).

The AS8C803601/801801 SRAM utilize IDT's latest high-performance CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) .

Pin Description Summary

A$_0$-A$_{18}$	Address Inputs	Input	Synchronous
$\overline{CE}_1$, CE2, $\overline{CE}_2$	Chip Enables	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
R/$\overline{W}$	Read/Write Signal	Input	Synchronous
$\overline{CEN}$	Clock Enable	Input	Synchronous
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/$\overline{LD}$	Advance burst address / Load new address	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	Static
ZZ	Sleep Mode	Input	Asynchronous
I/O$_0$-I/O$_{31}$, I/O$_{P1}$-I/O$_{P4}$	Data Input / Output	I/O	Synchronous
V$_{DD}$, V$_{DDQ}$	Core Power, I/O Power	Supply	Static
V$_{SS}$	Ground	Supply	Static

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Pin Definitions[1]

Symbol	Pin Function	I/O	Active	Description
A0-A18	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/$\overline{LD}$ low, $\overline{CEN}$ low, and true chip enables.
ADV/$\overline{LD}$	Advance / Load	I	N/A	ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/$\overline{LD}$ is low with the chip deselected, any burst in progress is terminated. When ADV/$\overline{LD}$ is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/$\overline{LD}$ is sampled high.
R/$\overline{W}$	Read / Write	I	N/A	R/$\overline{W}$ signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.
$\overline{CEN}$	Clock Enable	I	LOW	Synchronous Clock Enable Input. When $\overline{CEN}$ is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CEN}$ sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, $\overline{CEN}$ must be sampled low at rising edge of clock.
$\overline{BW}_1$-$\overline{BW}_4$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled low) the appropriate byte write signal ($\overline{BW}_1$-$\overline{BW}_4$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/$\overline{W}$ is sampled high. The appropriate byte(s) of data are written into the device two cycles later. $\overline{BW}_1$-$\overline{BW}_4$ can all be tied low if always doing write to the entire 36-bit word.
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enables	I	LOW	Synchronous active low chip enable. $\overline{CE}_1$ and $\overline{CE}_2$ are used with CE2 to enable the AS8C 803601/ 801801 ($\overline{CE}_1$ or $\overline{CE}_2$ sampled high or CE2 sampled low) and ADV/$\overline{LD}$ low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.
CE2	Chip Enable	I	HIGH	Synchronous active high chip enable. CE2 is used with $\overline{CE}_1$ and $\overline{CE}_2$ to enable the chip. CE2 has inverted polarity but otherwise identical to $\overline{CE}_1$ and $\overline{CE}_2$.
CLK	Clock	I	N/A	This is the clock input to the AS8C803601/801801. Except for $\overline{OE}$, all timing references for the device are made with respect to the rising edge of CLK.
I/O0-I/O31 I/OP1-I/OP4	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{LBO}$	Linear Burst Order	I	LOW	Burst order selection input. When $\overline{LBO}$ is high the Interleaved burst sequence is selected. When $\overline{LBO}$ is low the Linear burst sequence is selected. $\overline{LBO}$ is a static input and it must not change during device operation.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. $\overline{OE}$ must be low to read data from the AS8C803601/801801. When $\overline{OE}$ is high the I/O pins are in a high-impedance state. $\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied low.
ZZ	Sleep Mode	I	N/A	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the AS8C803601/801801 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.
VDD	Power Supply	N/A	N/A	3.3V core power supply.
VDDQ	Power Supply	N/A	N/A	3.3V I/O Supply.
VSS	Ground	N/A	N/A	Ground.

NOTE:

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1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Functional Block Diagram

Input Register inputs: $\overline{LBO}$, Address A [0:18], $\overline{CE1}$, CE2, $\overline{CE2}$, R/$\overline{W}$, $\overline{CEN}$, ADV/$\overline{LD}$, $\overline{BW}$x

512x18 BIT MEMORY ARRAY — Address, Control, DI, DO

Control Logic

Mux / Sel

Output Register — D, Clk, Q

Gate

Clock, $\overline{OE}$

Data I/O [0:15], I/O P[1:2]
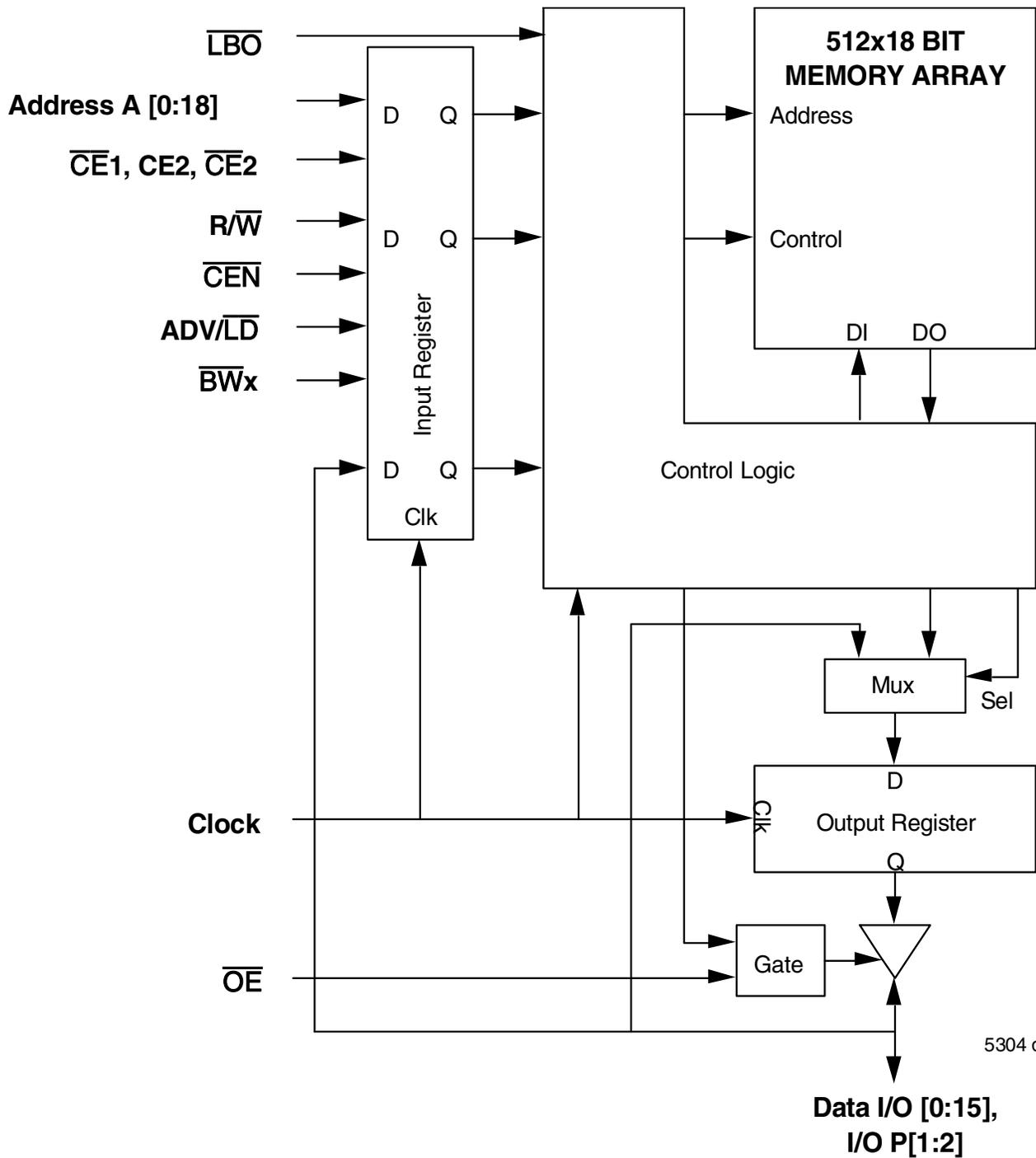
5304 drw 01

Functional Block Diagram

LBO̅

Address A [0:18]

CE̅1, CE2, CE̅2

R/W̅

CE̅N

ADV/LD̅

BW̅x

Input Register

D Q

D Q

D Q

Clk

512x18 BIT MEMORY ARRAY

Address

Control

DI   DO

Control Logic

Mux   Sel

D

Output Register

Clk

Q

Gate

Clock

OE̅

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Data I/O [0:15], I/O P[1:2]
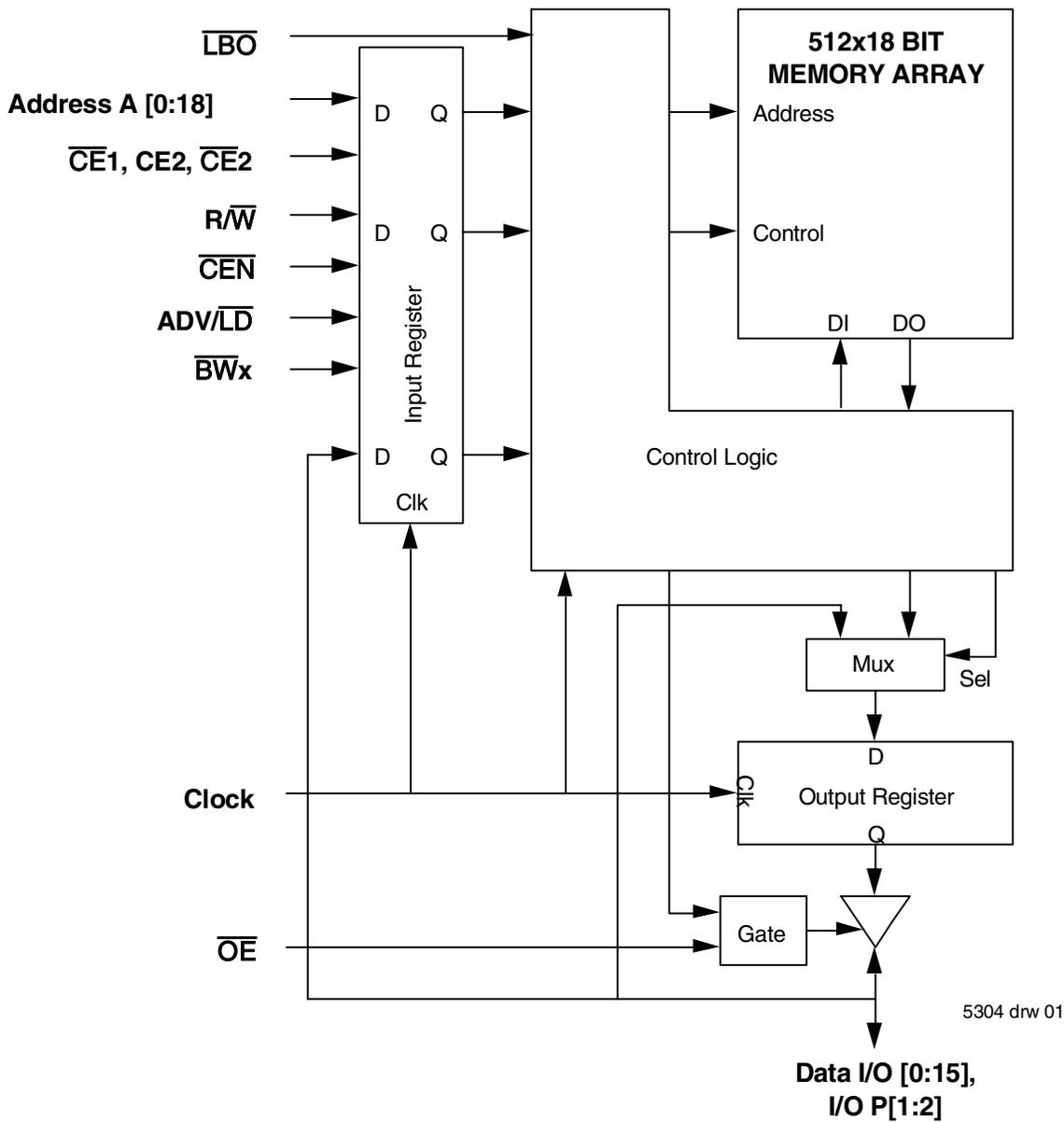
Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD}+0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ}+0.3	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

5304 tbl 04

NOTES:
1. V_{IL} (min.) = –1.0V for pulse width less than t_{CYC}/2, once per cycle.
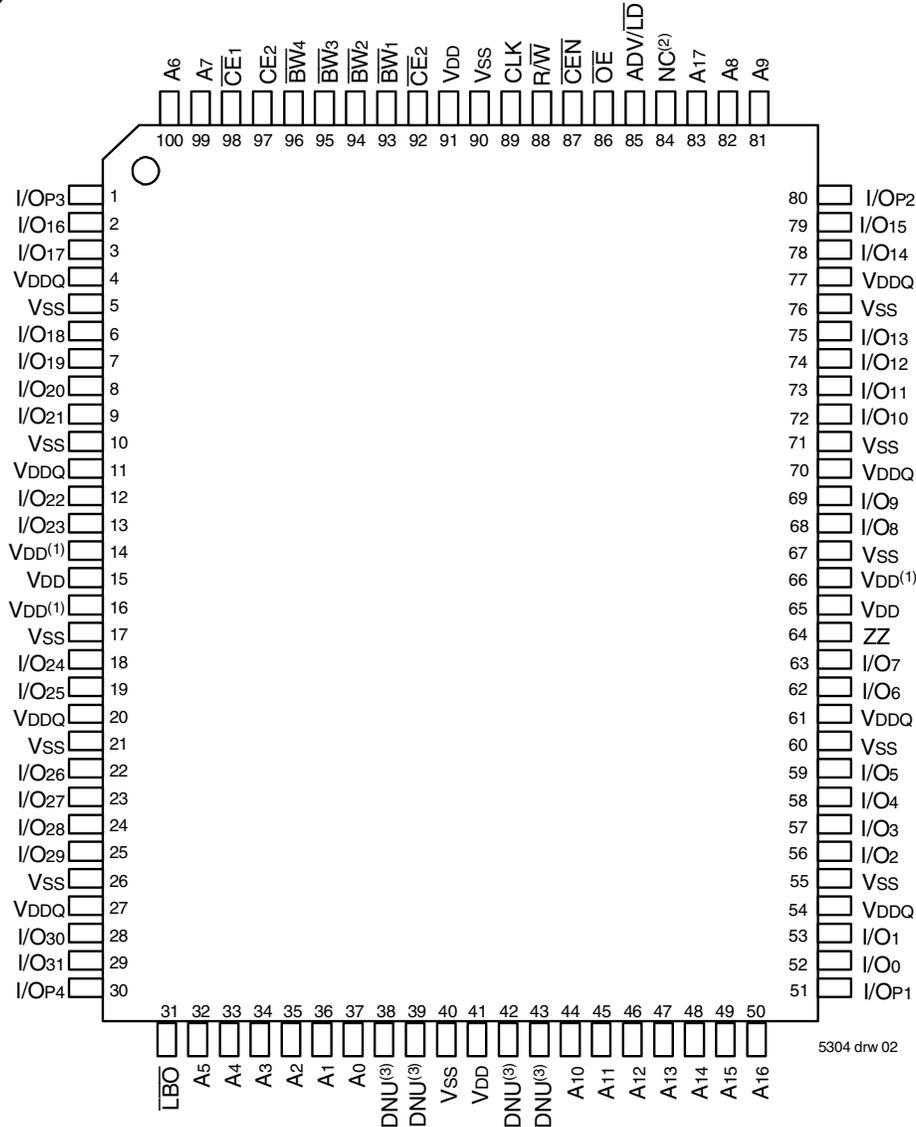
Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature[1]	V_{SS}	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

NOTES:

1. During production testing, the case temperature equals the ambient temperature.
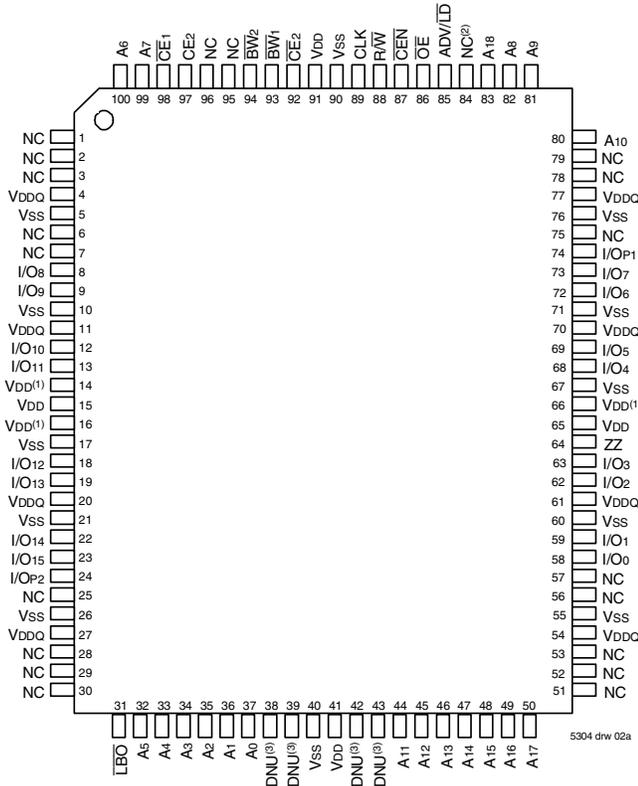
Pin Configuration - 256K x 36

**Top View
100 TQFP**

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NOTES:

1. Pins 14, 16 and 66 do not have to be connected directly to VDD as long as the input voltage is ≥ VIH.
2. Pin 84 is reserved for a future 16M.
3. DNU=Do not use. Pins 38, 39, 42 and 43 are reserved for respective JTAG pins: TMS, TDI, TDO and TCK. The current die revision allows these pins to be left unconnected, tied LOW (VSS), or tied HIGH (VDD).

Pin Configuration - 512K x 18

Top pins (100-81): A6 A7 CE1̄ CE2 NC NC BW2̄ BW1̄ CE2̄ VDD VSS CLK R/W̄ CEN̄ OĒ ADV/LD̄ NC(2) A8 A9

Left pins (1-30):
Pin	Signal
1	NC
2	NC
3	NC
4	VDDQ
5	VSS
6	NC
7	NC
8	I/O8
9	I/O9
10	VSS
11	VDDQ
12	I/O10
13	I/O11
14	VDD(1)
15	VDD
16	VDD(1)
17	VSS
18	I/O12
19	I/O13
20	VDDQ
21	VSS
22	I/O14
23	I/O15
24	I/OP2
25	NC
26	VSS
27	VDDQ
28	NC
29	NC
30	NC

Right pins (80-51):
Pin	Signal
80	A10
79	NC
78	NC
77	VDDQ
76	VSS
75	NC
74	I/OP1
73	I/O7
72	I/O6
71	VSS
70	VDDQ
69	I/O5
68	I/O4
67	VSS
66	VDD(1)
65	VDD
64	ZZ
63	I/O3
62	I/O2
61	VDDQ
60	VSS
59	I/O1
58	I/O0
57	NC
56	NC
55	VSS
54	VDDQ
53	NC
52	NC
51	NC

Bottom pins (31-50): LBO A5 A4 A3 A2 A1 A0 DNU(3) DNU(3) VSS VDD DNU(3) DNU(3) A11 A12 A13 A14 A15 A16 A17

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Top View
100 TQFP

NOTES:
1. Pins 14, 16 and 66 do not have to be connected directly to VDD as long as the input voltage is ≥ VIH.
2. Pin 84 is reserved for a future 16M.
3. DNU=Do not use. Pins 38, 39, 42 and 43 are reserved for respective JTAG pins: TMS, TDI, TDO and TCK. The current die revision allows these pins to be left unconnected, tied LOW (VSS), or tied HIGH (VDD).

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}[3,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}[4,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}[5,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A[7]	**Commercial** Operating Temperature	-0 to +70	ºC
	Industrial Operating Temperature	-40 to +85	ºC
T_{BIAS}	Temperature Under Bias	-55 to +125	ºC
T_{STG}	Storage Temperature	-55 to +125	ºC
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

5304 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. During production testing, the case temperature equals T_A.

100 TQFP Capacitance[1]
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5304 tbl 07

165 fBGA Capacitance[1]
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	TBD	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	TBD	pF

5304 tbl 07b

119 BGA Capacitance[1]
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5304 tbl 07a

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Synchronous Truth Table[1]

$\overline{CEN}$	R/$\overline{W}$	Chip[5] Enable	ADV/$\overline{LD}$	$\overline{BW}x$	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (2 cycles later)
L	L	Select	L	Valid	External	X	LOAD WRITE	D[7]
L	H	Select	L	X	External	X	LOAD READ	Q[7]
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter)[2]	D[7]
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter)[2]	Q[7]
L	X	Deselect	L	X	X	X	DESELECT or STOP[3]	HiZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HiZ
H	X	X	X	X	X	X	SUSPEND[4]	Previous Value

5304 tbl 08

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. When ADV/$\overline{LD}$ signal is sampled high, the internal burst counter is incremented. The R/$\overline{W}$ signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either ($\overline{CE}_1$, or $\overline{CE}_2$ is sampled high or CE $_2$ is sampled low) and ADV/$\overline{LD}$ is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4. When $\overline{CEN}$ is sampled high at the rising edge of clock, that clock edge is blocked from propogating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires $\overline{CE}_1$ = L, $\overline{CE}_2$ = L, CE $_2$ = H on these chip enables. Chip is deselected if any one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
7. Q - Data read from the device, D - data written to the device.

Partial Truth Table for Writes[1]

OPERATION	R/$\overline{W}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$[3]	$\overline{BW}_4$[3]
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O[0:7], I/O$_{P1}$)[2]	L	L	H	H	H
WRITE BYTE 2 (I/O[8:15], I/O$_{P2}$)[2]	L	H	L	H	H
WRITE BYTE 3 (I/O[16:23], I/O$_{P3}$)[2,3]	L	H	H	L	H
WRITE BYTE 4 (I/O[24:31], I/O$_{P4}$)[2,3]	L	H	H	H	L
NO RITE W	L	H	H	H	H

5304 tbl 09

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.
3. N/A for X18 configuration.

Interleaved Burst Sequence Table ($\overline{\text{LBO}}$=V$_{DD}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address[1]	1	1	1	0	0	1	0	0

5304 tbl 10

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.
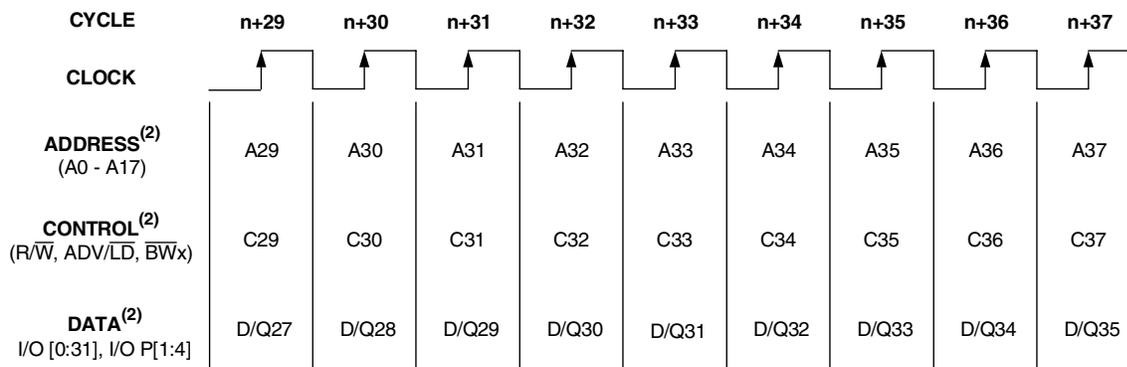
Linear Burst Sequence Table ($\overline{\text{LBO}}$=V$_{SS}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address[1]	1	1	0	0	0	1	1	0

5304 tbl 11

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram[1]

CYCLE	n+29	n+30	n+31	n+32	n+33	n+34	n+35	n+36	n+37
CLOCK									
ADDRESS[2] (A0 - A17)	A29	A30	A31	A32	A33	A34	A35	A36	A37
CONTROL[2] (R/$\overline{\text{W}}$, ADV/$\overline{\text{LD}}$, $\overline{\text{BW}}$x)	C29	C30	C31	C32	C33	C34	C35	C36	C37
DATA[2] I/O [0:31], I/O P[1:4]	D/Q27	D/Q28	D/Q29	D/Q30	D/Q31	D/Q32	D/Q33	D/Q34	D/Q35

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NOTES:
1. This assumes $\overline{\text{CEN}}$, $\overline{\text{CE}}$1, CE 2, $\overline{\text{CE}}$2 are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles[2]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[1]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Load read
n+1	X	X	H	X	L	X	X	X	Burst read
n+2	A_1	H	L	L	L	X	L	Q_0	Load read
n+3	X	X	L	H	L	X	L	Q_{0+1}	Deselect or STOP
n+4	X	X	H	X	L	X	L	Q_1	NOOP
n+5	A_2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	X	Z	Burst read
n+7	X	X	L	H	L	X	L	Q_2	Deselect or STOP
n+8	A_3	L	L	L	L	L	L	Q_{2+1}	Load write
n+9	X	X	H	X	L	L	X	Z	Burst write
n+10	A_4	L	L	L	L	L	X	D_3	Load write
n+11	X	X	L	H	L	X	X	D_{3+1}	Deselect or STOP
n+12	X	X	H	X	L	X	X	D_4	NOOP
n+13	A_5	L	L	L	L	L	X	Z	Load write
n+14	A_6	H	L	L	L	X	X	Z	Load read
n+15	A_7	L	L	L	L	L	X	D_5	Load write
n+16	X	X	H	X	L	L	L	Q_6	Burst write
n+17	A_8	H	L	L	L	X	X	D_7	Load read
n+18	X	X	H	X	L	X	X	D_{7+1}	Burst read
n+19	A_9	L	L	L	L	L	L	Q_8	Load write

5304tbl 12

NOTES:
1. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.
2. H = High; L = Low; X = Don't Care; Z = High Impedance.

Read Operation[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup and V
n+2	X	X	X	X	X	X	L	Q_0	Contents of Address A_0 Read Out

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Burst Read Operation[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q_{0+1}	Address A_{0+1} Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q_{0+2}	Address A_{0+2} Read Out, Inc. Count
n+5	A_1	H	L	L	L	X	L	Q_{0+3}	Address A_{0+3} Read Out, Load A_1
n+6	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	Q_1	Address A_1 Read Out, Inc. Count
n+8	A_2	H	L	L	L	X	L	Q_{1+1}	Address A_{1+1} Read Out, Load A_2

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance..
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE $_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE $_2$ = L.

Write Operation[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D_0	Write to Address A_0

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE $_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE $_2$ = L.

Burst Write Operation[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+3	X	X	H	X	L	L	X	D_{0+1}	Address A_{0+1} Write, Inc. Count
n+4	X	X	H	X	L	L	X	D_{0+2}	Address A_{0+2} Write, Inc. Count
n+5	A_1	L	L	L	L	L	X	D_{0+3}	Address A_{0+3} Write, Load A_1
n+6	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+7	X	X	H	X	L	L	X	D_1	Address A_1 Write, Inc. Count
n+8	A_2	L	L	L	L	L	X	D_{1+1}	Address A_{1+1} Write, Load A_2

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE $_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE $_2$ = L.

Read Operation with Clock Enable Used[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A_1	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	Q_0	Clock Ignored, Data Q0 is on the bus.
n+4	X	X	X	X	H	X	L	Q_0	Clock Ignored, Data Q0 is on the bus.
n+5	A_2	H	L	L	L	X	L	Q_0	Address A0 Read out (bus trans.)
n+6	A_3	H	L	L	L	X	L	Q_1	Address A1 Read out (bus trans.)
n+7	A_4	H	L	L	L	X	L	Q_2	Address A2 Read out (bus trans.)

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE 2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE 2 = L.

Write Operation with Clock Enable Used[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A_1	L	L	L	L	L	X	X	Clock Valid.
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A_2	L	L	L	L	L	X	D_0	Write Data D0
n+6	A_3	L	L	L	L	L	X	D_1	Write Data D1
n+7	A_4	L	L	L	L	L	X	D_2	Write Data D2

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE 2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE 2 = L.
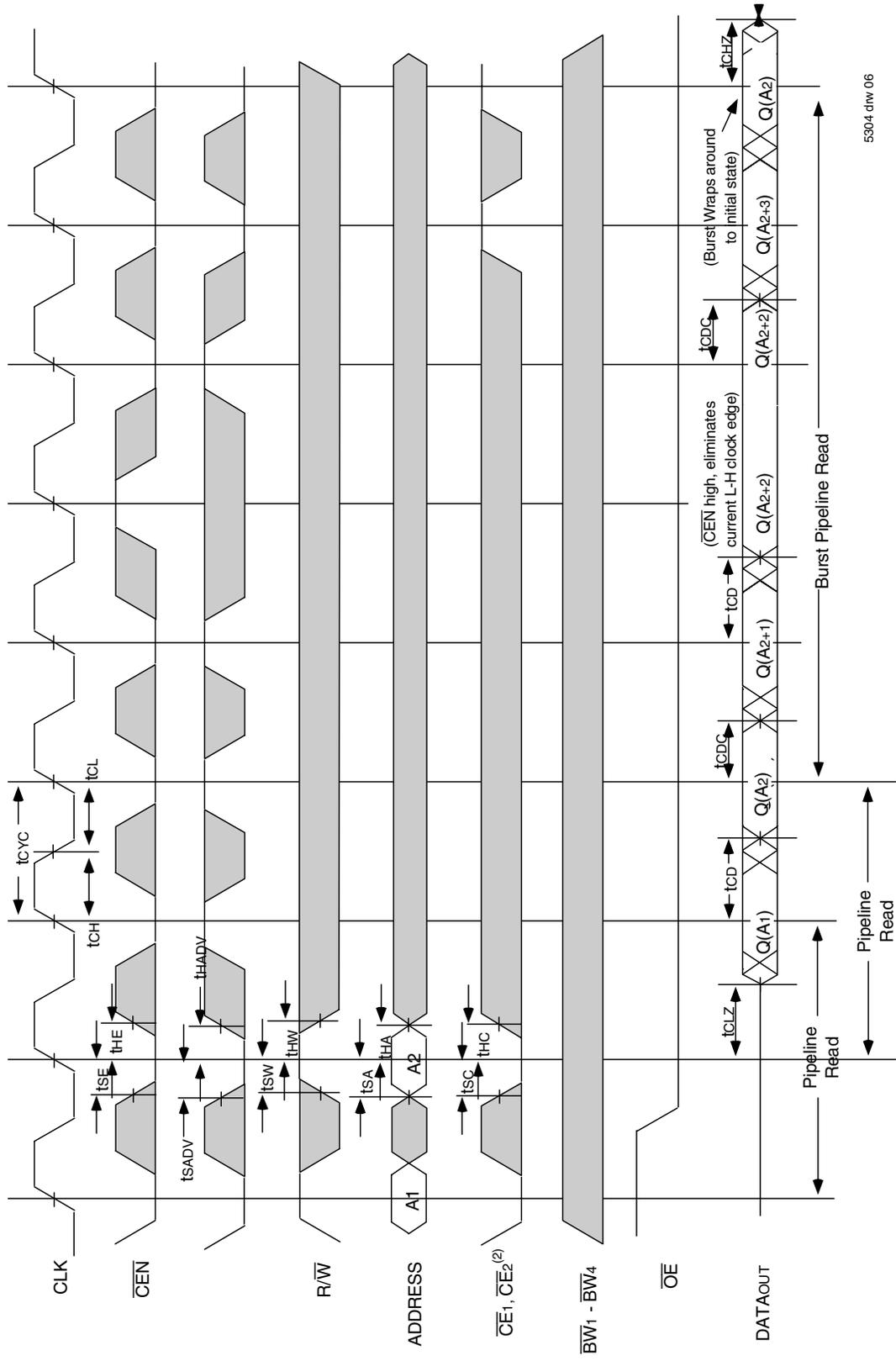
Read Operation with Chip Enable Used[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O[3]	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A_0	H	L	L	L	X	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A_1	H	L	L	L	X	L	Q_0	Address A_0 Read out. Load A_1.
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	L	Q_1	Address A_1 Read out. Deselected.
n+7	A_2	H	L	L	L	X	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	L	Q_2	Address A_2 Read out. Deselected.

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE$_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE$_2$ = L.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

Write Operation with Chip Enable Used[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O[3]	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A_0	L	L	L	L	L	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A_1	L	L	L	L	L	X	D_0	Address D_0 Write in. Load A_1.
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	X	D_1	Address D_1 Write in. Deselected.
n+7	A_2	L	L	L	L	L	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	X	D_2	Address D_2 Write in. Deselected.

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE$_2$ = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE$_2$ = L.

AC Electrical Characteristics
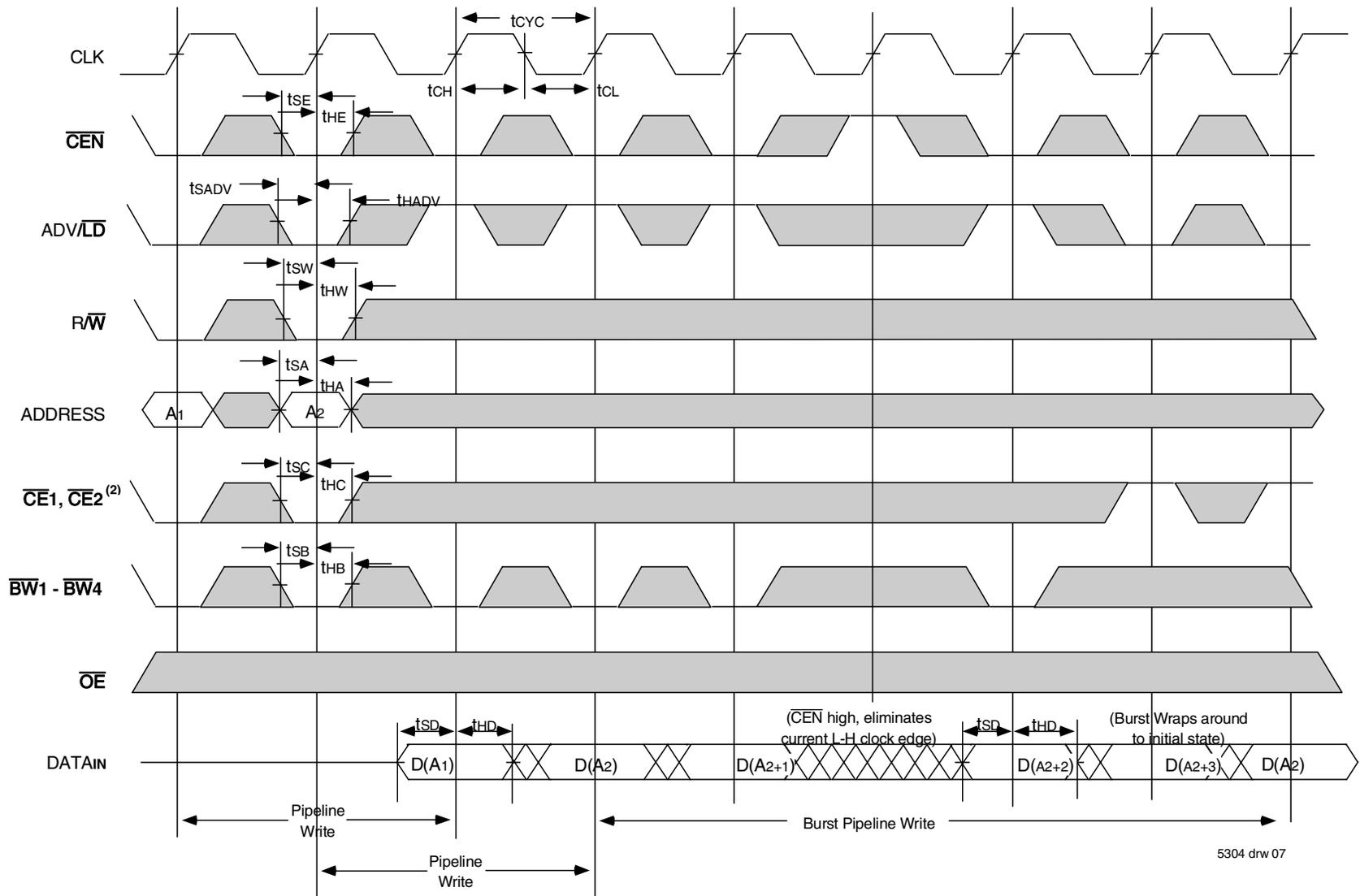## (VDD = 3.3V +/-5%, Industrial Temperature Range)

Symbol	Parameter	150MHz Min.	150MHz Max.	133MHz Min.	133MHz Max.	100MHz Min.	100MHz Max.	Unit
t_{CYC}	Clock Cycle Time	6.7	—	7.5	—	10	—	ns
$t_F^{(1)}$	Clock Frequency	—	150	—	133	—	100	MHz
$t_{CH}^{(2)}$	Clock High Pulse Width	2.0	—	2.2	—	3.2	—	ns
$t_{CL}^{(2)}$	Clock Low Pulse Width	2.0	—	2.2	—	3.2	—	ns
Output Parameters								
t_{CD}	Clock High to Valid Data	—	3.8.	—	4.2	—	5	ns
t_{CDC}	Clock High to Data Change	1.5	—	1.5	—	1.5	—	ns
$t_{CLZ}^{(3,4,5)}$	Clock High to Output Active	1.5	—	1.5	—	1.5	—	ns
$t_{CHZ}^{(3,4,5)}$	Clock High to Data High-Z	1.5	3	1.5	3	1.5	3.3	ns
t_{OE}	Output Enable Access Time	—	3.8	—	4.2	—	5	ns
$t_{OLZ}^{(3,4)}$	Output Enable Low to Data Active	0	—	0	—	0	—	ns
$t_{OHZ}^{(3,4)}$	Output Enable High to Data High-Z	—	3.8	—	4.2	—	5	ns
Set Up Times								
t_{SE}	Clock Enable Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SA}	Address Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SD}	Data In Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SW}	Read/Write (R/$\overline{W}$) Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SADV}	Advance/Load (ADV/$\overline{LD}$) Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SB}	Byte Write Enable ($\overline{BW}$x) Setup Time	1.5	—	1.7	—	2.0	—	ns
Hold Times								
t_{HE}	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Read/Write (R/$\overline{W}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HADV}	Advance/Load (ADV/$\overline{LD}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HB}	Byte Write Enable ($\overline{BW}$x) Hold Time	0.5	—	0.5	—	0.5	—	ns

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NOTES:
1. $t_F = 1/t_{CYC}$.
2. Measured as HIGH above 0.6V $_{DDQ}$ and LOW below 0.4V $_{DDQ}$.
3. Transition is measured ±200mV from steady-state.
4. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
5. To avoid bus contention, the output buffers are designed such that t $_{CHZ}$ (device turn-off) is about 1ns faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 3.135V).
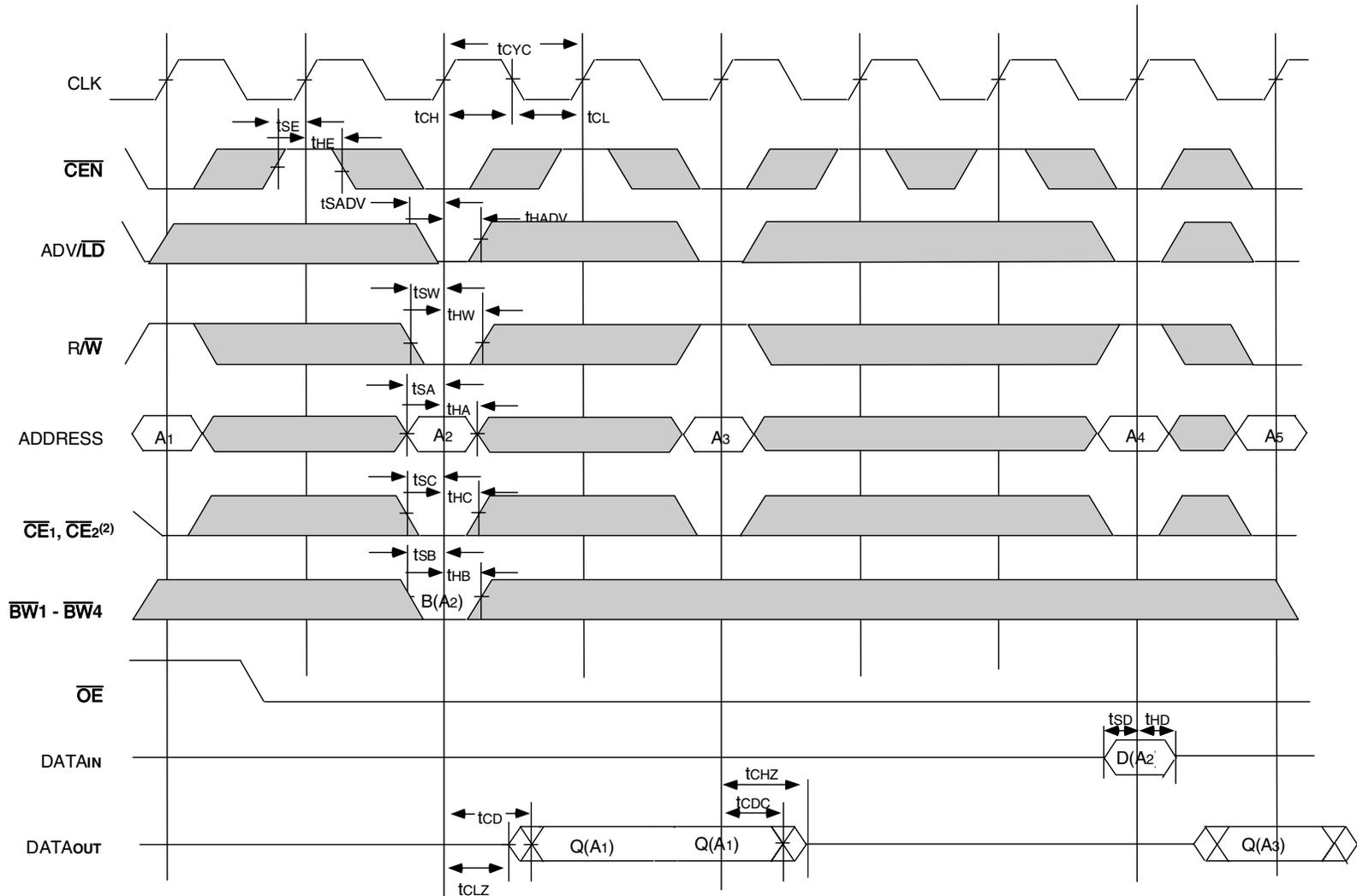
CLK

$\overline{CEN}$

R/$\overline{W}$

ADDRESS

$\overline{CE}_1$, $\overline{CE}_2^{(2)}$

$\overline{BW}_1$ - $\overline{BW}_4$

$\overline{OE}$

DATAout

tCYC

tCL

tCH

tHE

tSE

tSADV

tHADV

tSW

tHW

tSA

tHA

A1

A2

tSC

tHC

tCLZ

tCD

tCDC

tCD

tCDC

tCDC

tCHZ

Q(A1)

Q(A2)

Q(A2+1)

Q(A2+2)

Q(A2)

Q(A2+2)

Q(A2+3)

Q(A2)

Pipeline Read

Pipeline Read

Pipeline Read

Burst Pipeline Read

($\overline{CEN}$ high, eliminates current L-H clock edge)

(Burst Wraps around to initial state)

5304 drw 06

CLK

tCYC

tCH tCL

$\overline{CEN}$

tSE

tHE

ADV/$\overline{LD}$

tSADV

tHADV

R/$\overline{W}$

tSW

tHW

ADDRESS

tSA

tHA

A₁   A₂

$\overline{CE}1$, $\overline{CE}2$ [2]

tSC

tHC

$\overline{BW}1$ - $\overline{BW}4$

tSB

tHB

$\overline{OE}$

DATAIN

tSD tHD

($\overline{CEN}$ high, eliminates current L-H clock edge)

tSD tHD

(Burst Wraps around to initial state)

D(A₁)   D(A₂)   D(A₂₊₁)   D(A₂₊₂)   D(A₂₊₃)   D(A₂)

Pipeline Write

Pipeline Write

Burst Pipeline Write

5304 drw 07

5304 drw 08

NOTES:

1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the CE̅1 and CE̅2 signals. For example, when CE̅1 and CE̅2 are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals (BW̅x) must be valid on all write and burst-write cycles. A write cycle is initiated when RW̅ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

5304 drw 09

CLK

$\overline{CEN}$

ADV/$\overline{LD}$

R/$\overline{W}$

ADDRESS

$\overline{CE}1$, $\overline{CE}2$ [2]

$\overline{BW}1$ - $\overline{BW}4$

$\overline{OE}$

DATA$_{IN}$

DATA$_{OUT}$

tCYC tCH tCL

tSE tHE

tSADV tHADV

tSW tHW

tSA tHA

tSC tHC

tSB tHB

tCD tCLZ

tCHZ tCDC

tSD tHD

A1 A2 A3 A4 A5

Q(A1) Q(A2) D(A3) Q(A4)

5304 drw 10
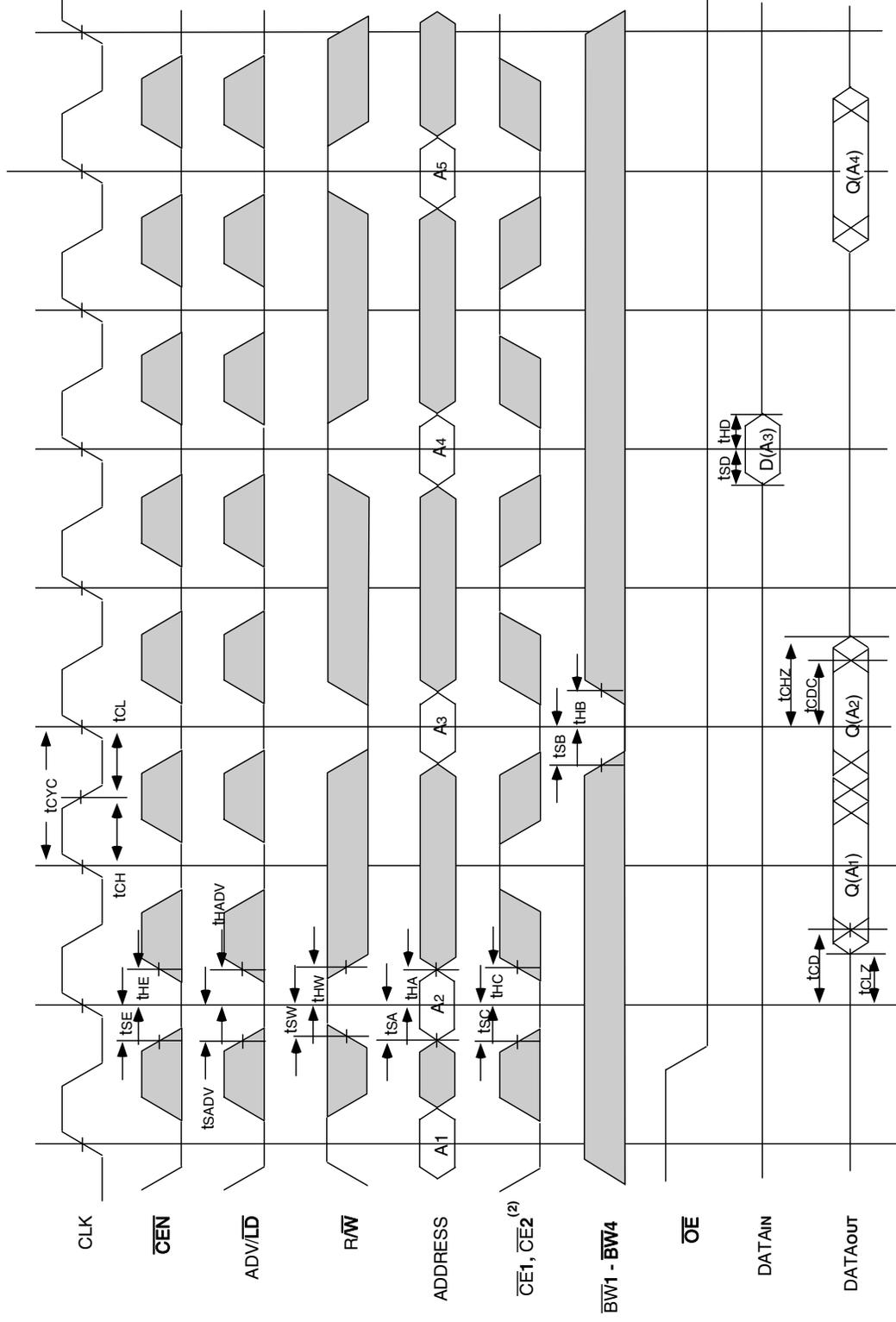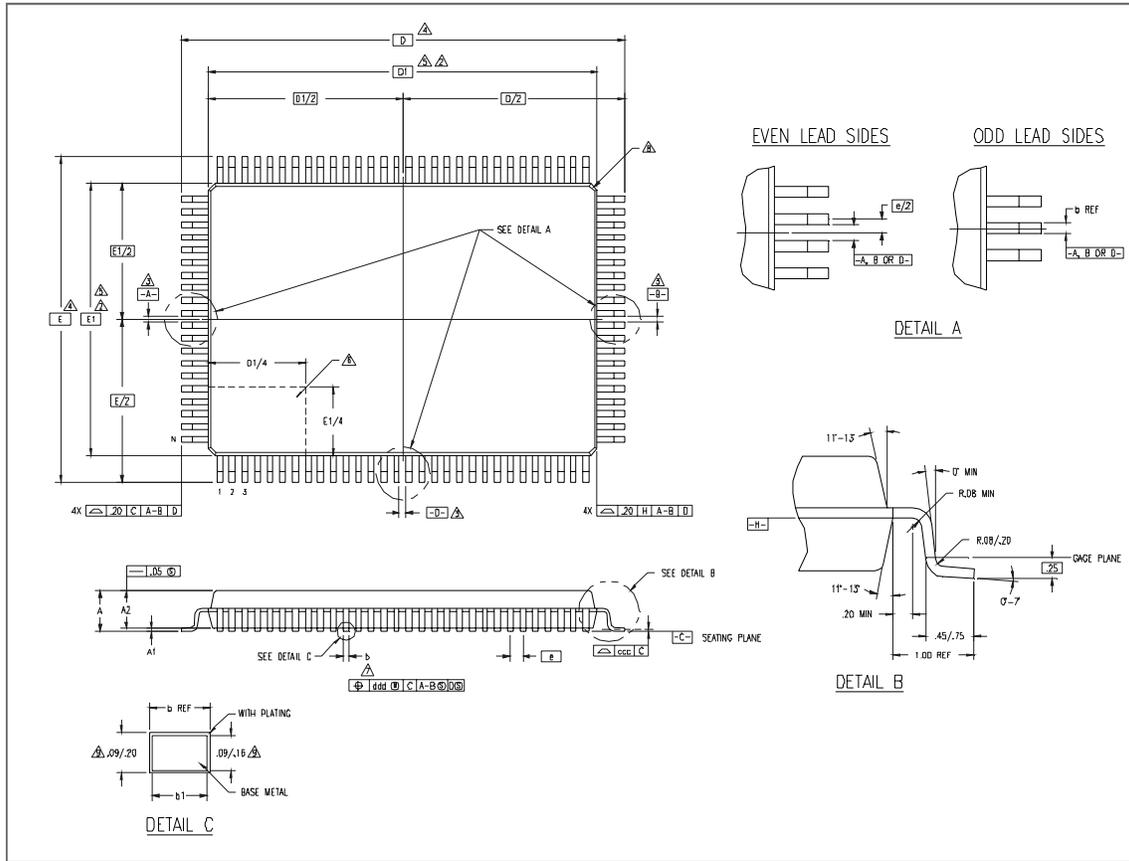
SYMBOL	JEDEC VARIATION DJ			NOTE
	MIN	NOM	MAX	
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	22.00 BSC			4
D1	20.00 BSC			5,2
E	16.00 BSC			4
E1	14.00 BSC			5,2
N	100			
ND	30			
NE	20			
e	.65 BSC			
b	.22	.32	.38	7
b1	.22	.30	.33	
ccc	–	–	.10	
ddd	–	–	.13	

LAND PATTERN DIMENSIONS
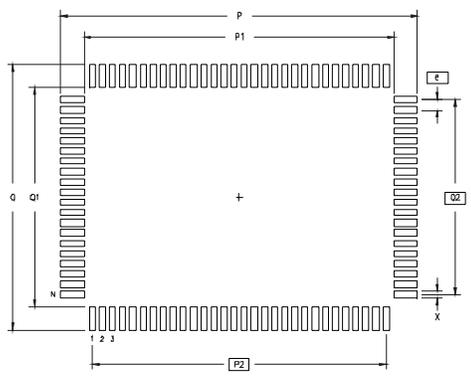
	MIN	MAX
P	22.80	23.00
P1	19.80	20.00
P2	18.85 BSC	
Q	16.80	17.00
Q1	13.80	14.00
Q2	12.35 BSC	
X	.30	.50
e	.65 BSC	
N	100	

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE -C-

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION DJ AND BX

Timing Waveform of $\overline{OE}$ Operation[1]
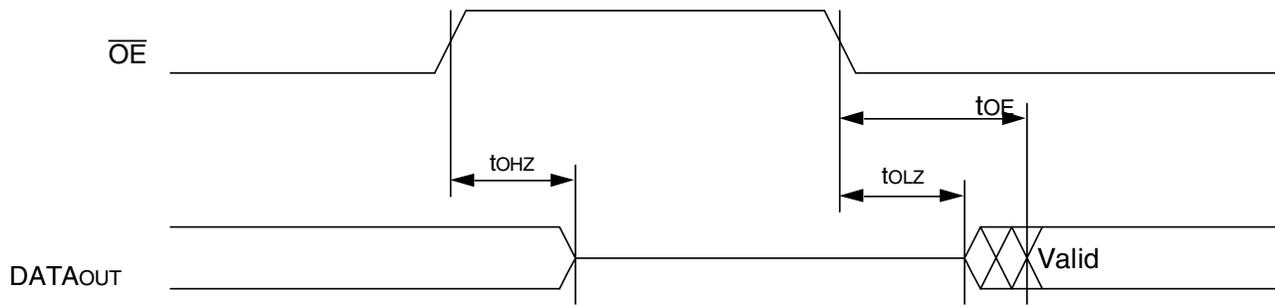
5304 drw 11

NOTE:

1. A read operation is assumed to be in progress.

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ORDERING INFORMATION

Alliance	Organization	VCC Range	Package	Operating Temp	Speed Mhz
AS8C803601-QC150N	256K x 36	3.1 - 3.4V	100 pin TQFP	Comercial 0 - 70C	150
AS8C801801-QC150N	512K x 18	3.1 - 3.4V	100 pin TQFP	Comercial 0 - 70C	150

PART NUMBERING SYSTEM

AS8C	Device	Conf.	Mode	Package	Operating Temp	Speed	N
Sync. SRAM prefix	80 = 8M	18= x18￼ 36 = x36	01= ZBT￼ 00 = Pipelined￼ 25 = Flow- Thru	Q = 100 Pin TQFP	0 ~ 70C	150MHz	N= Leadfree

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