0 Hz/DC to 14 GHz, Single-Pole, Four-Throw MEMS Switch with Integrated Driver

Data Sheet **ADGM1304**

FEATURES

- Fully operational down to 0 Hz/dc
  - On resistance: 1.6 Ω (typical)
  - Off leakage: 0.5 nA (maximum)
- –3 dB bandwidth
  - 11 GHz (typical) for RF1, RF4
  - 14 GHz (typical) for RF2, RF3
- RF performance characteristics
  - Insertion loss: 0.26 dB (typical) at 2.5 GHz
  - Isolation: 24 dB (typical) at 2.5 GHz
  - IIP3: 69 dBm (typical)
  - RF power: 36 dBm (maximum)
- Actuation lifetime: 1 billion cycles (minimum)
  - Hermetically sealed switch contacts
  - On switching time: 30 µs (typical)
- Integrated driver removes the need for an external driver
  - Supply voltage: 3.1 V to 3.3 V
  - CMOS-/LVTTL-compatible
  - Parallel interface
  - Independently controllable switches
  - I_{DD} sleep mode current: 1 µA typical power consumption
- Switch is in an open state with no power supply present
- Requirement to mitigate floating nodes on all RF pins, see the Applications Information section
- 24-lead, 5 mm × 4 mm × 0.95 mm, LFCSP

APPLICATIONS

- Relay replacements
- Automatic test equipment (ATE): RF/digital/mixed signals
- Load/probe boards: RF/digital/mixed signals
- RF test instrumentation
- Reconfigurable filters/attenuators
- High performance RF switching

GENERAL DESCRIPTION

The ADGM1304 is a wideband, single-pole, four-throw (SP4T) switch, fabricated using Analog Devices, Inc., microelectromechanical system (MEMS) switch technology. This technology enables a small, wide bandwidth, highly linear, low insertion loss switch that is operational down to 0 Hz/dc, making it an ideal switching solution for a wide range of RF applications.

An integrated control chip generates the high voltage necessary to electrostatically actuate the switch via a complementary metal-oxide semiconductor (CMOS)-/low voltage transistor-transistor logic (LVTTL)-compatible parallel interface. All four switches are independently controllable.

The ADGM1304 is packaged in a 24-lead, 5 mm × 4 mm × 0.95 mm, lead frame chip-scale package (LFCSP).

FUNCTIONAL BLOCK DIAGRAM

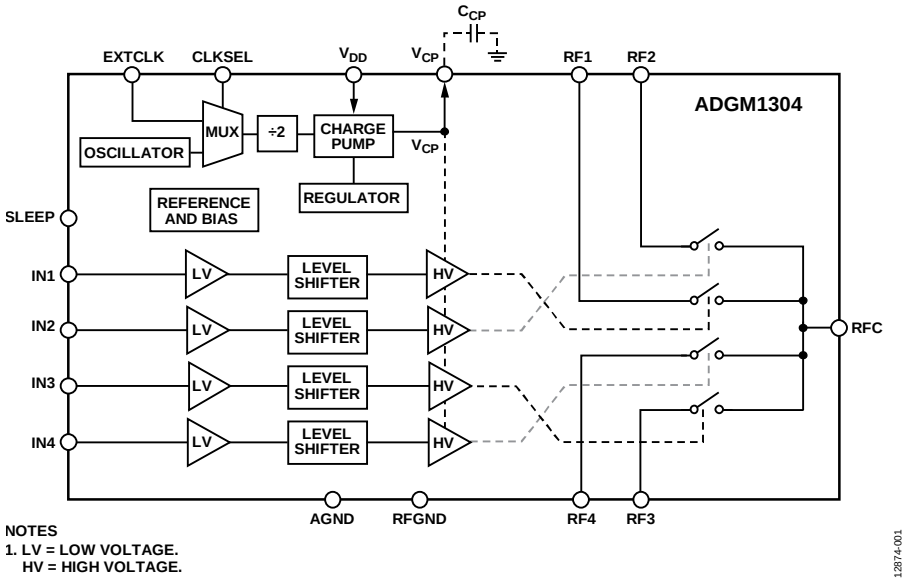

Figure 1.

Rev. D

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

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REVISION HISTORY

3/2018—Rev. C to Rev. D

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Added Eye Diagrams Section and Figure 17 to Figure 22; Renumbered Sequentially ... 10
Added Figure 30, Figure 31, and Figure 32 ... 12
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10/2016—Revision C: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V, AGND = 0 V, RFGND = 0 V, all specifications T_{MIN} to T_{MAX} = 0°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
DYNAMIC CHARACTERISTICS						
−3 dB Bandwidth[3]	BW					
RF1, RF4		9.3	11		GHz	RF1 to RFC and RF4 to RFC channels
RF2, RF3		12	14		GHz	RF2 to RFC and RF3 to RFC channels
Insertion Loss[3]	IL		0.26	0.55	dB	At 2.5 GHz; RFC to RFx channel; 25°C
			0.4	0.9	dB	At 6.0 GHz; RFC to RFx channel; 25°C
Isolation[3]	I_{SO}	23	24		dB	At 2.5 GHz; RFC to RFx channel
		17	19		dB	At 6.0 GHz; RFC to RFx channel
Crosstalk[3]	C_{TK}	27	30		dB	At 2.5 GHz; RFx to RFx channel
		22	24		dB	At 6.0 GHz; RFx to RFx channel
Return Loss[3]	RL	13	18		dB	Up to 6.0 GHz
Input Third-Order Intermodulation Intercept	IIP3		69		dBm	Input: 900 MHz and 901 MHz; input power = 27 dBm
Input Second-Order Intermodulation Intercept	IIP2		119		dBm	Input: 900 MHz and 901 MHz; input power = 27 dBm
Second Harmonic	HD2		−90		dBc	Input: 5.4 MHz; input power = 0 dBm
	HD2		−85		dBc	Input: 150 MHz and 800 MHz; input power = 36 dBm
Third Harmonic	HD3		−85		dBc	Input: 150 MHz and 800 MHz; input power = 36 dBm
Total Harmonic Distortion and Noise	THD + N		−110		dBc	R_L = 300 Ω, f = 1 kHz, RFx pin = 2.5 V p-p
Radio Frequency (RF) Power Rating[3, 4]				36	dBm	50 Ω termination
DC Voltage Range		−6		+6	V	On switch dc voltage operation range
Time						
On Switching	t_{ON}		30	75	µs	50% INx pin to 90% RFx pin, 50 Ω termination
Off Switching	t_{OFF}		5	30	µs	50% INx pin to 10% RFx pin, 50 Ω termination
Settling						
Rising Edge[3]			40		µs	50% INx pin to 0.05 dB final IL value, 50 Ω termination
Falling Edge[3]			8		µs	50% INx pin to 0.05 dB final IL value, 50 Ω termination
Wake-Up			0.55	1.2	ms	C_{CP} = 47 pF; 50% INx pin to 90% RFx pin
Actuation Frequency[3]				5	kHz	All switches toggled simultaneously
Video Feedthrough[3]			16		mV peak	1 MΩ termination
Internal Oscillator Frequency		7.9		15	MHz	
Internal Oscillator Feedthrough[3, 5]			−115		dBm	Spectrum analyzer resolution bandwidth (RBW) = 200 Hz; one switch in on state, all other switches off with 50 Ω terminations; see Note 6 for measurement setup details[6]
SWITCH PROPERTIES						
On Resistance	R_{ON}		1.6	3.6	Ω	I_{DS} = 50 mA, 0 V input bias, at 1 ms after actuation
On Resistance Stability[3]	ΔR_{ON}		1.4		Ω	10^9 actuations; full temperature range; 1 kHz cycling frequency; 220 mA load between toggles
RF Port						
On Capacitance[3]	C_{RF} On		3.3		pF	At 1 MHz
Off Capacitance[3]	C_{RF} Off		1.6		pF	At 1 MHz
On Leakage				5	nA	RFx (off channels) = −6 V; RFC/RFx (on channel) = −6 V
Off Leakage				0.5	nA	RFx pin = 6 V; RFC = −6 V
Continuously On Lifetime[3]			7.2		Years	Median time before failure[7] at 50°C
Actuation Lifetime[3]		10^9			Cycles	Cold switched; load between toggling is 220 mA; tested at 85°C

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
EXTCLK PROPERTIES						
EXTCLK Input Range		20		23	MHz	
EXTCLK Input High Voltage	EV_{INH}	1.5			V	
EXTCLK Input Low Voltage	EV_{INL}			0.5	V	
EXTCLK Input Current	EI_{INL}/EI_{INH}			±10	µA	$EV_{IN} = EV_{INL}$ or EV_{INH}
DIGITAL INPUTS						
Input High Voltage	V_{INH}	2			V	
Input Low Voltage	V_{INL}			0.8	V	
Input Current	I_{INL}/I_{INH}		0.025	1	µA	$V_{IN} = V_{INL}$ or V_{INH}
POWER REQUIREMENTS						
Supply Voltage	V_{DD}	3.1		3.3	V	
Supply Current	I_{DD}		2.9	3.2	mA	V_{DD} = 3.3 V; digital inputs = 0 V or 3.3 V
I_{DD} Sleep Mode Current			1		µA	

[1] Typical specifications tested at 25°C with V_{DD} = 3.3 V.
[2] RFx is the RF1, RF2, RF3, and RF4 pins, and INx is the IN1, IN2, IN3, and IN4 pins.
[3] Guaranteed by design, not subject to production test.
[4] The 1 dB compression point (P1dB) is not reached up to the maximum power rating of the switch.
[5] Disable the internal oscillator to eliminate feedthrough. See the Driver IC Oscillator section and the External Clock (EXTCLK) section.
[6] The spectrum analyzer setup is as follows: RBW = 200 Hz, video bandwidth (VBW) = 2 Hz, span = 100 kHz, input attenuator = 0 dB, the detector type is peak, and the maximum hold is off. The fundamental feedthrough noise or harmonic thereof (whichever is higher) is tested.
[7] This value shows the median time it takes for 50% of a sample lot to fail.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +6 V
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA (whichever occurs first)
DC Voltage Rating[2]	±10 V
Current Rating[2]	250 mA
RF Power Rating	37 dBm
Stand Off Voltage[3]	100 V (RFC pin)
	20 V (RFx pins)
Hot Switching[4]	0 V
EXTCLK Input Voltage	−0.3 V to V_{DD} + 0.3 V or 30 mA (whichever occurs first)
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering (Pb-Free)	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 30 sec
ESD	
Human Body Model (HBM)[5]	
RF1 to RF4 Pins and RFC Pin	100 V
All Other Pins	2.5 kV
Field-Induced Charged-Device Model (FICDM)[6]	
All Pins	500 V
Group D	
Mechanical Shock[7]	1500 *g* with 0.5 ms pulse
Vibration	20 Hz to 2000 Hz acceleration at 50 *g*
Constant Acceleration	30,000 *g*

[1] Clamp overvoltages at INx pin by internal diodes. Limit the current to the maximum ratings given.
[2] This rating is with respect to the switch in the on position with no RF signal applied.
[3] This rating is with respect to the switch in the off position.
[4] Hot switching is not recommended.
[5] Take proper precautions during handling as outlined in the Handling Precautions section.
[6] A safe automated handling and assembly process is achieved at this rating level by implementing industry-standard ESD controls.
[7] If the device is dropped during handling, do not use the device.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-9[1]	49.1	11.5	°C/W

[1] See JEDEC standard JESD51-2 for additional information on optimizing the thermal impedance (PCB with 3 × 3 vias).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

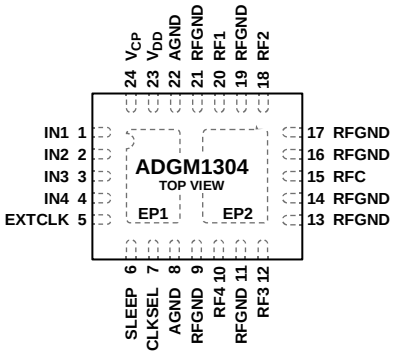

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	Digital Control Input 1. The voltage applied to this pin controls the gate of the MEMS switch RF1 to RFC. If IN1 is low, RF1 to RFC is open (off). If IN1 is high, connect RF1 to RFC (on).
2	IN2	Digital Control Input 2. The voltage applied to this pin controls the gate of the MEMS switch RF2 to RFC. If IN2 is low, RF2 to RFC is open (off). If IN2 is high, connect RF2 to RFC (on).
3	IN3	Digital Control Input 3. The voltage applied to this pin controls the gate of the MEMS switch RF3 to RFC. If IN3 is low, RF3 to RFC is open (off). If IN3 is high, connect RF3 to RFC (on).
4	IN4	Digital Control Input 4. The voltage applied to this pin controls the gate of the MEMS switch RF4 to RFC. If IN4 is low, RF4 to RFC is open (off). If IN4 is high, connect RF4 to RFC (on).
5	EXTCLK	External Clock Input. The ADGM1304 has a built-in oscillator that drives the internal driver boost circuitry. An external clock source provided by the EXTCLK pin can disable and replace this internal oscillator. To enable the EXTCLK pin, set the CLKSEL pin to high. See the Specifications section for the allowable input range for the EXTCLK pin. In normal operation, when not using an external clock source, EXTCLK must be connected to ground.
6	SLEEP	Digital Input Pin. This feature shuts down internal circuitry, thereby reducing current consumption to minimum levels. If SLEEP is low, the ADGM1304 is in normal operating mode. If SLEEP is high, the ADGM1304 is in power-down mode, and the RFx pins are in a high impedance state.
7	CLKSEL	Internal Oscillator Control. In normal operation, set CLKSEL low and use the built-in oscillator to clock the driver boost circuitry. When CLKSEL is high, an external clock source on the EXTCLK pin can drive the boost circuitry. Note that setting CLKSEL high and EXTCLK low disables the internal oscillator and driver boost circuitry. Disabling the internal oscillator eliminates associated noise feedthrough into the switch. In this configuration, supply 80 V to the V_{CP} pin to drive the switches via the IN1 to IN4 pins
8, 22	AGND	Analog Ground Connection.
9, 11, 13, 14, 16, 17, 19, 21	RFGND	RF Ground Connection
10	RF4	RF4 Port. This pin can be an input or an output. If unused, connect this pin to RFGND.
12	RF3	RF3 Port. This pin can be an input or an output. If unused, connect this pin to RFGND.
15	RFC	Common RF Port. This pin can be an input or an output.
18	RF2	RF2 Port. This pin can be an input or an output. If unused, connect this pin to RFGND.
20	RF1	RF1 Port. This pin can be an input or an output. If unused, connect this pin to RFGND.
23	V_{DD}	Positive Power Supply Input. For the recommend input voltage for this chip, see the Specifications section. Boost up the input voltage internally to generate the voltage required to turn on the MEMS switch.
24	V_{CP}	Charge Pump Capacitor Terminal. The recommended capacitor value is 47 pF. To disable the internal oscillator, set the CLKSEL pin high and the EXTCLK pin low. Disabling the internal oscillator eliminates associated noise feedthrough into the switch. Applying 80 V to the V_{CP} pin to drive the switches via the IN1 to IN4 pins.
	EP1	Exposed Pad 1. EP1 is internally connected to AGND. It is recommended to connect to both AGND and RFGND.
	EP2	Exposed Pad 2. EP2 is internally connected to RFGND. It is recommended to connect to both RFGND and AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

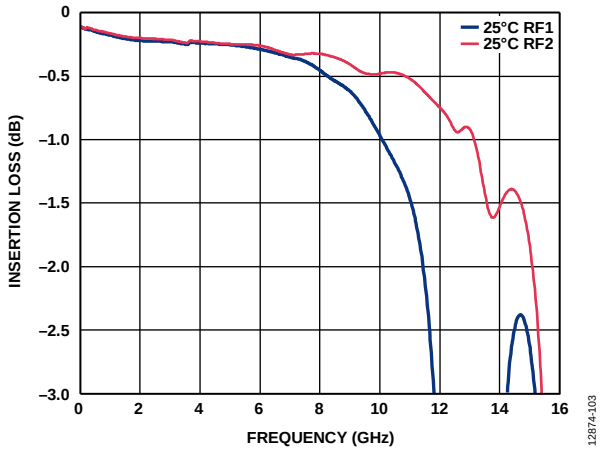

Figure 3. Insertion Loss vs. Frequency on Linear Scale (V_{DD} = 3.3 V)

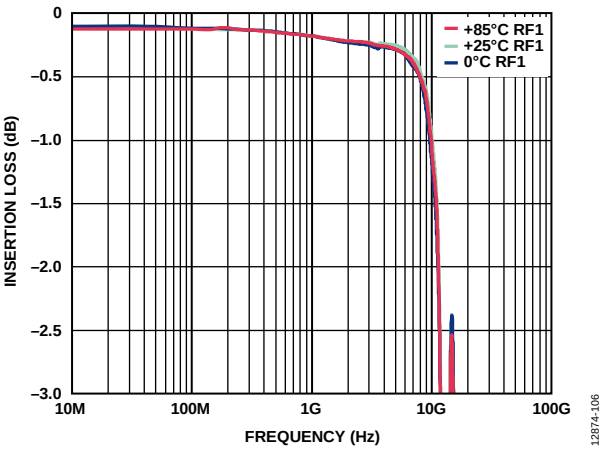

Figure 6. Insertion Loss vs. Frequency over Temperature on Log Scale (V_{DD} = 3.3 V, RF1 to RFC)

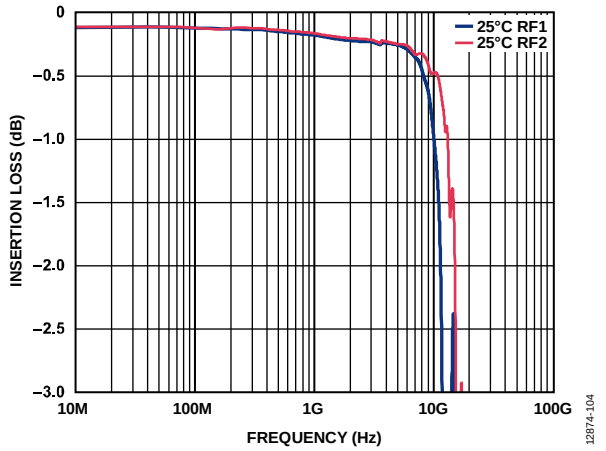

Figure 4. Insertion Loss vs. Frequency on Log Scale (V_{DD} = 3.3 V)

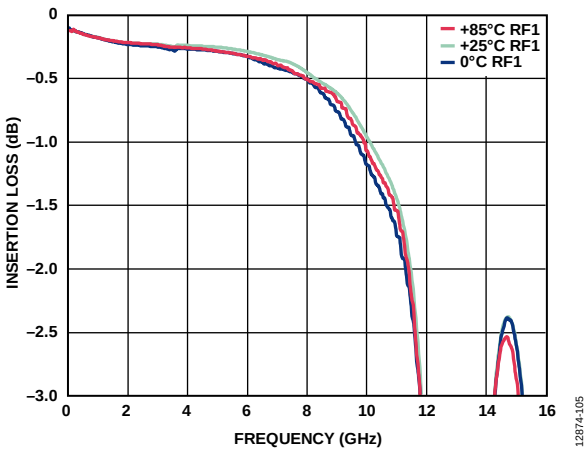

Figure 7. Insertion Loss vs. Frequency over Temperature on Linear Scale (V_{DD} = 3.3 V, RF1 to RFC)

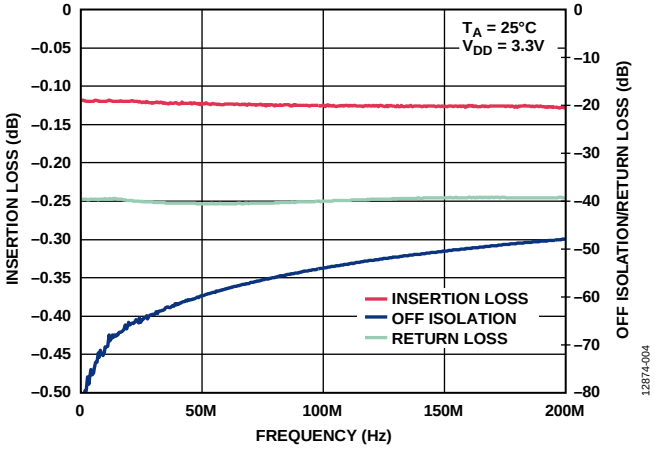

Figure 5. Insertion Loss and Off Isolation/Return Loss vs. Frequency (V_{DD} = 3.3 V, RF1 to RFC)

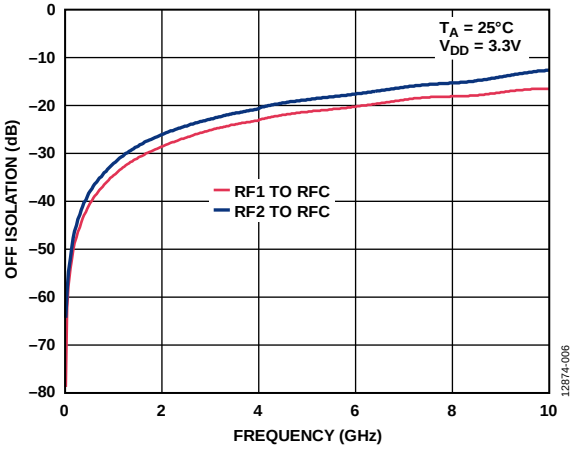

Figure 8. Off Isolation vs. Frequency (V_{DD} = 3.3 V)

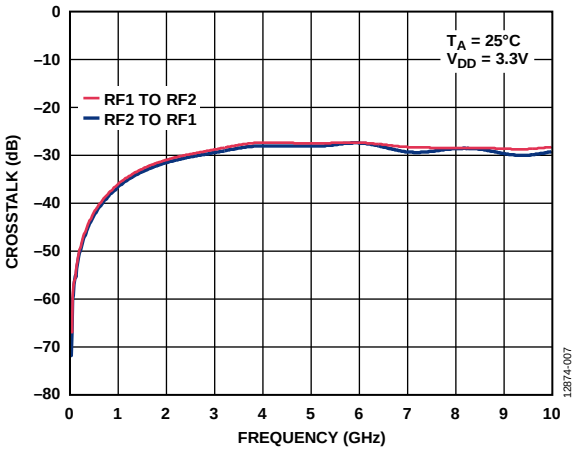

Figure 9. Crosstalk vs. Frequency (V_{DD} = 3.3 V)

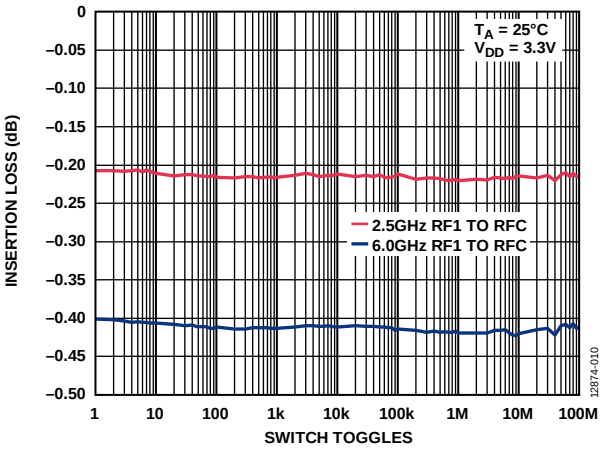

Figure 12. Insertion Loss vs. Switching Toggles (V_{DD} = 3.3 V)

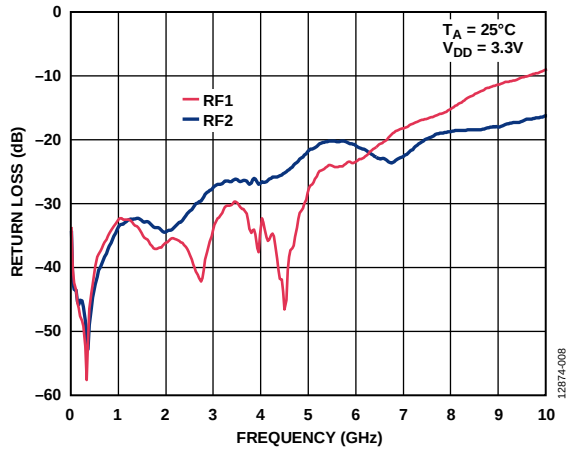

Figure 10. Return Loss vs. Frequency (V_{DD} = 3.3 V)

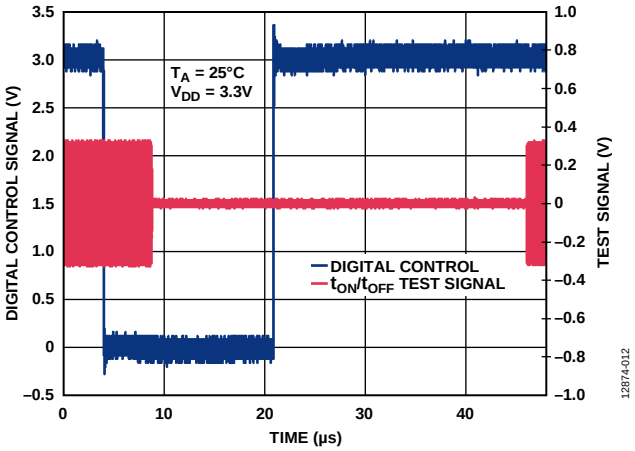

Figure 13. Digital Control Signal and Test Signal vs. Time (V_{DD} = 3.3 V)

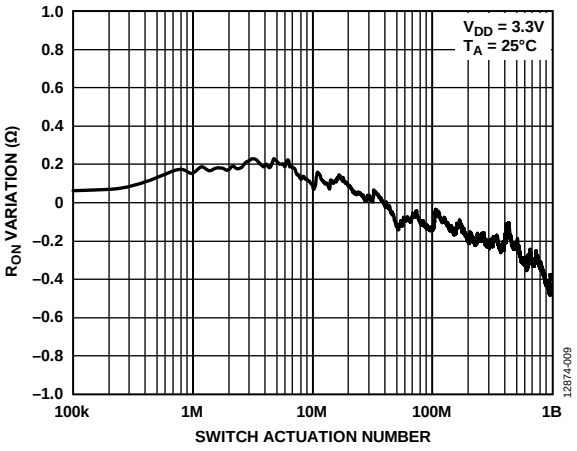

Figure 11. R_{ON} Variation vs. Switch Actuation Number (V_{DD} = 3.3 V, RF1 to RFC, Actuation Frequency = 1 kHz)

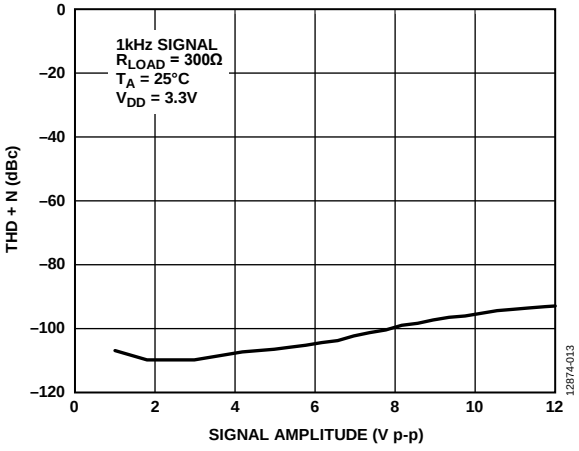

Figure 14. Total Harmonic Distortion Plus Noise (THD + N) vs. Signal Amplitude (V_{DD} = 3.3 V)

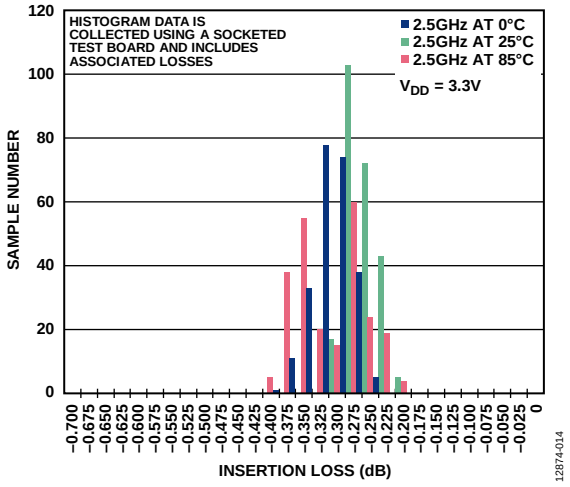

Figure 15. 2.5 GHz Insertion Loss Histogram vs. Temperature (V_{DD} = 3.3 V)

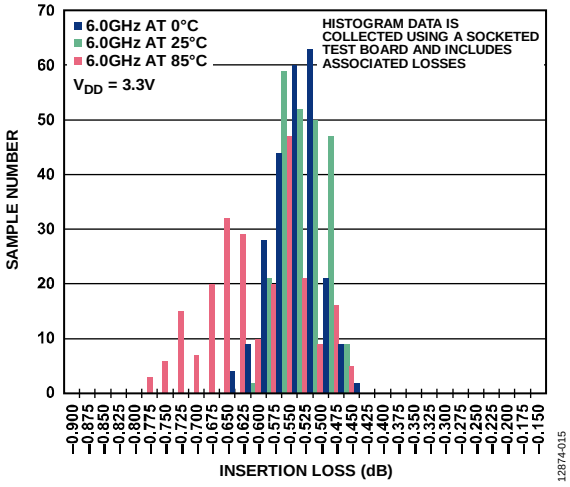

Figure 16. 6.0 GHz Insertion Loss Histogram vs. Temperature (V_{DD} = 3.3 V)

EYE DIAGRAMS

Pattern used for eye diagram measurements = pseudorandom binary sequence (PRBS) $2^{23} - 1$.

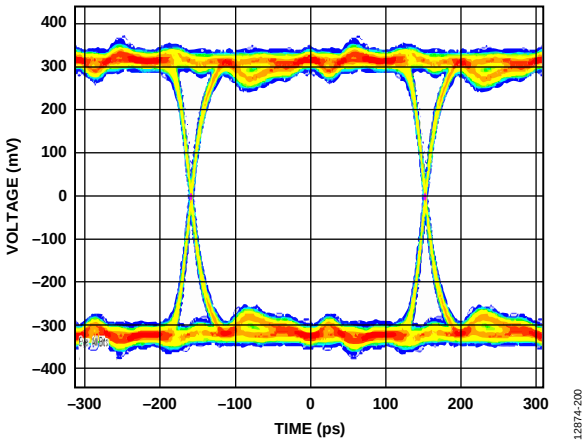

Figure 17. RF1 to RFC with Reference Trace at 3.2 Gbps

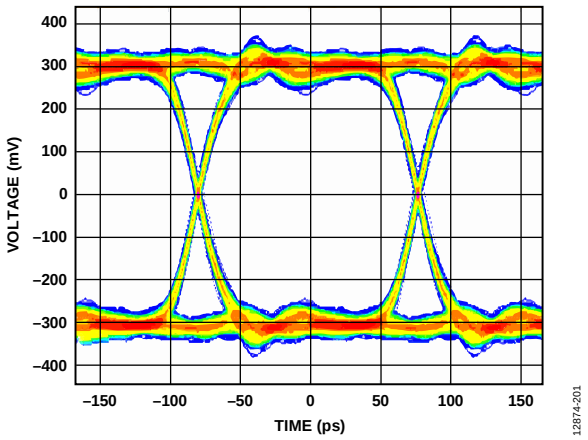

Figure 18. RF1 to RFC with Reference Trace at 6.4 Gbps

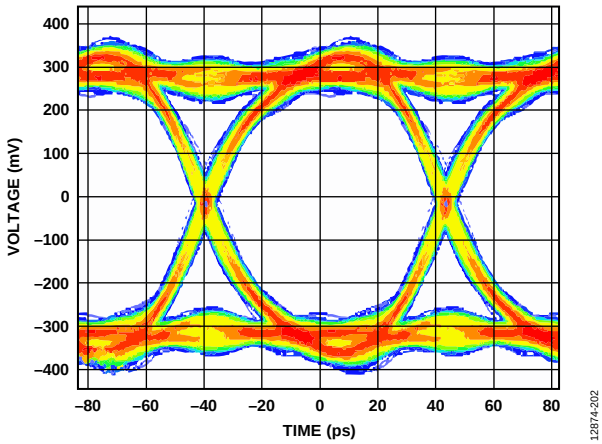

Figure 19. RF1 to RFC with Reference Trace at 12.5 Gbps

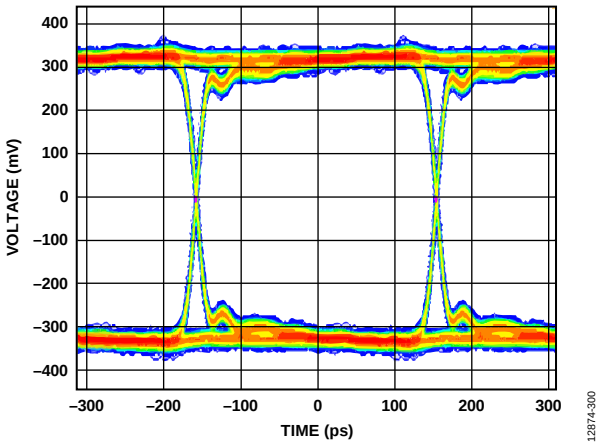

Figure 20. Eye Diagram Reference Trace at 3.2 Gbps

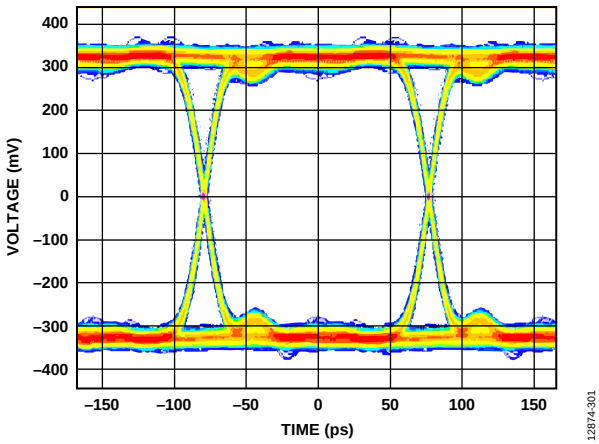

Figure 21. Eye Diagram Reference Trace at 6.4 Gbps

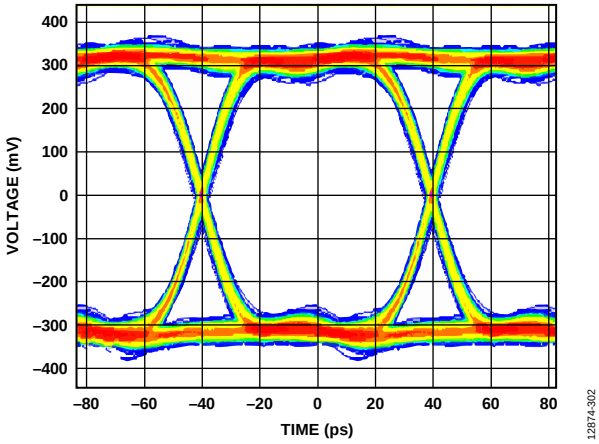

Figure 22. Eye Diagram Reference Trace at 12.5 Gbps

TEST CIRCUITS

Test circuits applicable to all channels; additional pins omitted for clarity.

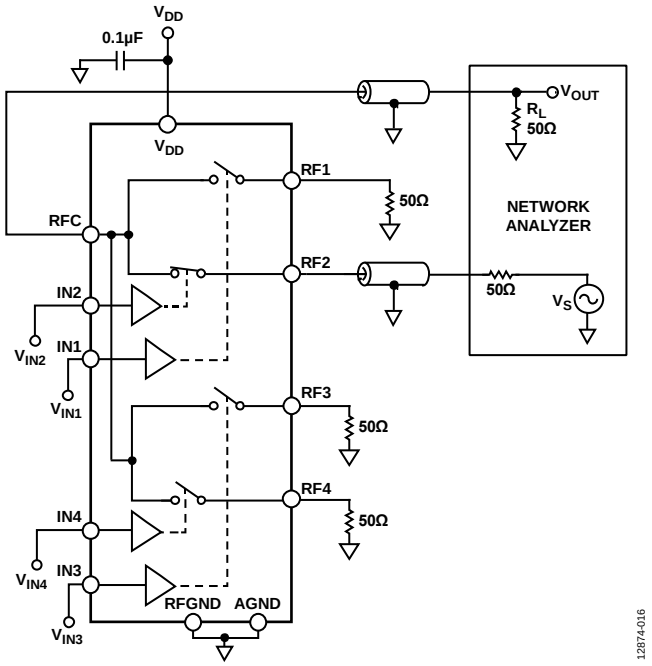

Figure 23. Insertion Loss/Return Loss

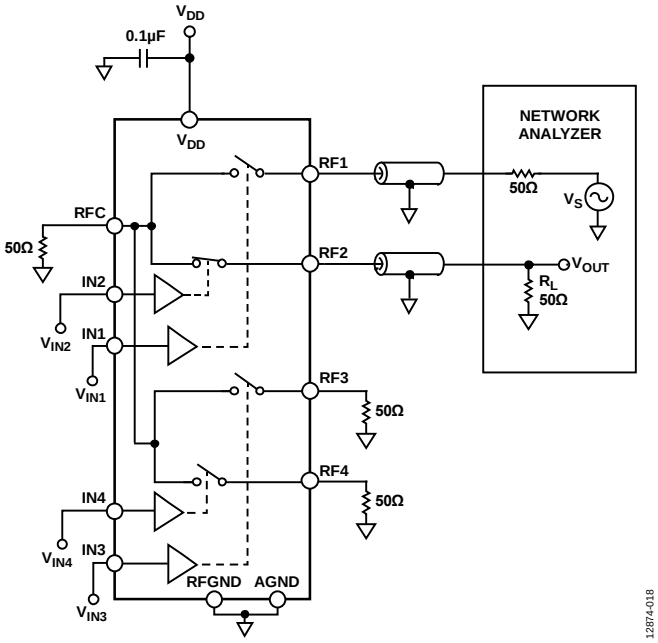

Figure 25. Crosstalk

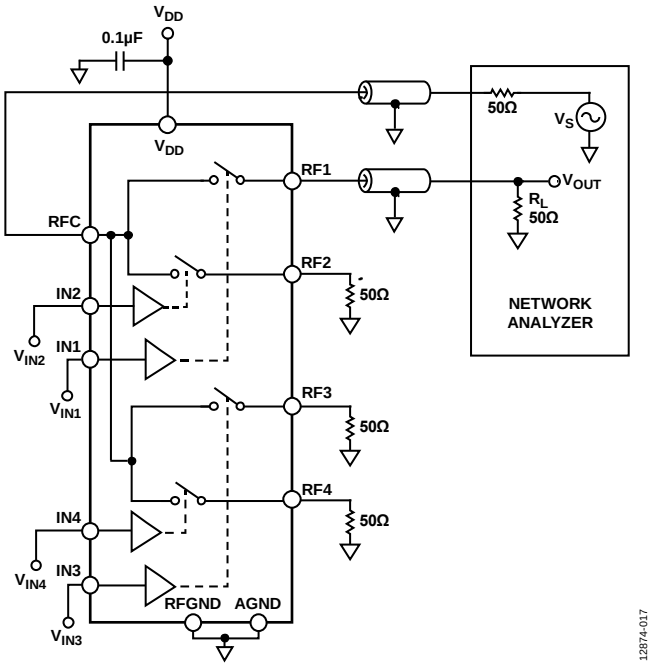

Figure 24. Isolation

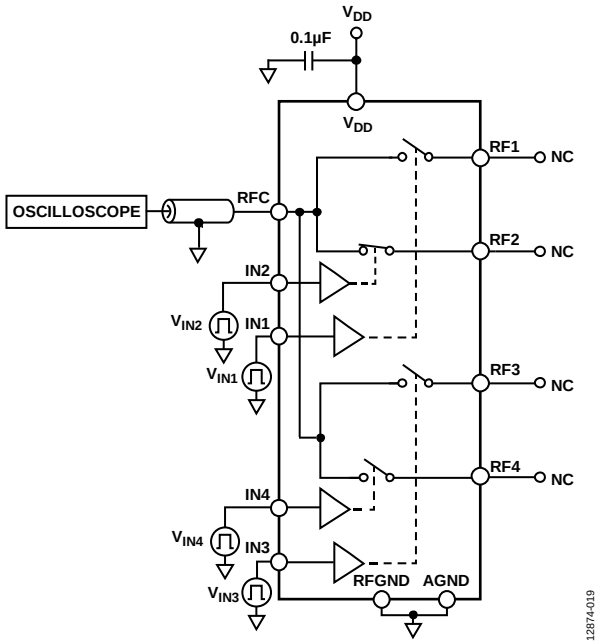

Figure 26. Video Feedthrough

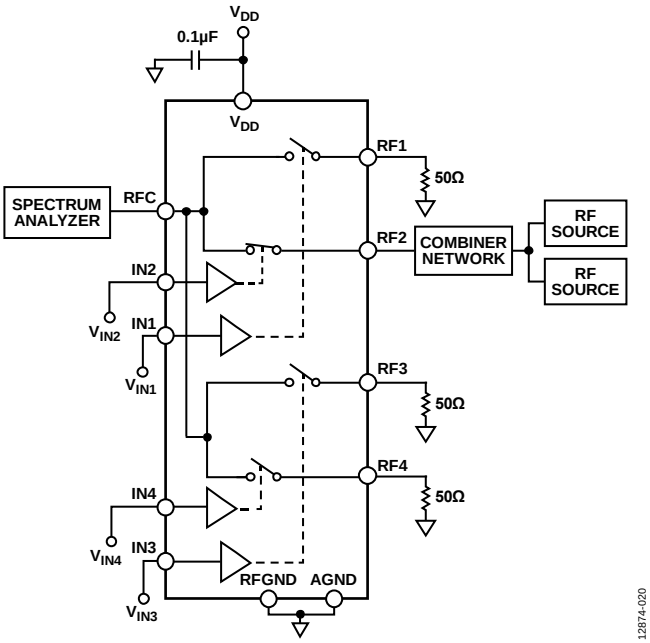

Figure 27. Input Second-Order Intermodulation Intercept (IP2) and Input Third-Order Intermodulation Intercept (IIP3)

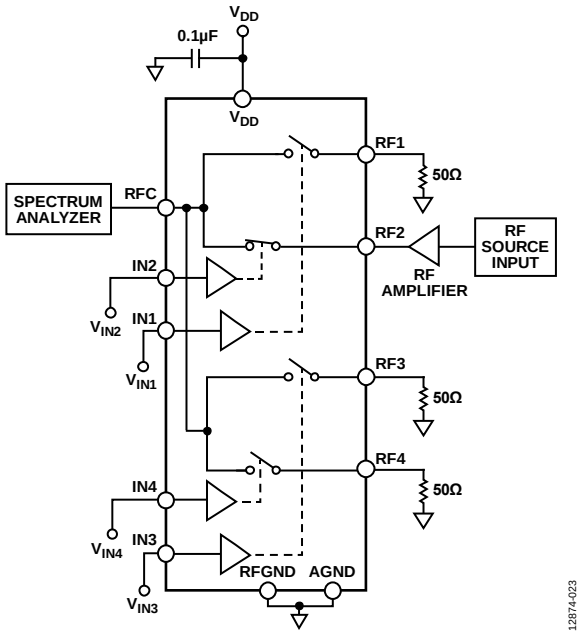

Figure 28. Second and Third Harmonics, RF Power

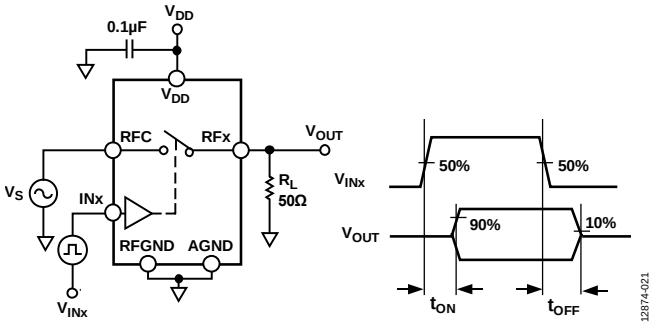

Figure 29. Switch Timings, t_{ON} and t_{OFF}

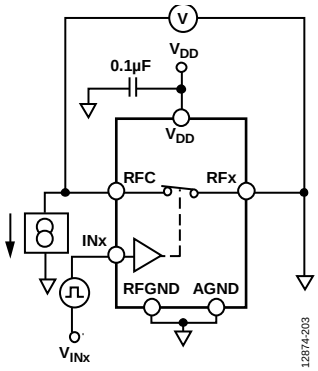

Figure 30. On Resistance

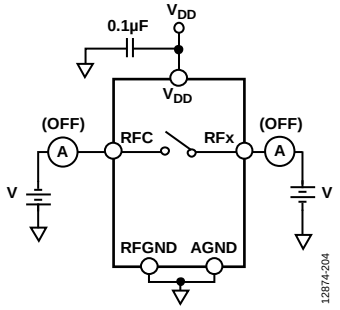

Figure 31. Off Leakage

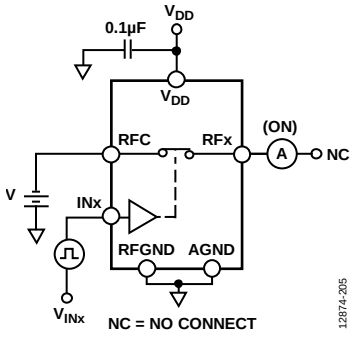

Figure 32. On Leakage

TERMINOLOGY

Insertion Loss (IL)
IL is the amount of signal attenuation between the input and output ports of the switch when the switch is in the on state. Expressed in decibels, ensure that insertion loss is as small as possible for maximum power transfer.

An example calculation of insertion loss based on the setup in Figure 23 is as follows:

$$IL = -20\log_{10}|S_{RF2RFC}| \text{ [dB]}$$

where S_{RF2RFC} is the transmission coefficient measured from RF2 to RFC with RF2 in the on position. All unused switches are in the off position and terminated in a purely resistive load of 50 Ω.

Isolation (I_{SO})
I_{SO} is the amount of signal attenuation between the input and output ports of the switch when the switch is in the off state. Expressed in decibels, ensure that isolation is as large as possible.

An example calculation of isolation based on the setup in Figure 24 is as follows:

$$I_{SO} = -20\log_{10}|S_{RFCRF1}| \text{ [dB]}$$

where S_{RFCRF1} is the transmission coefficient measured from RFC to RF1 with RF1 in the off position. All unused switches are in the off position and terminated in a purely resistive load of 50 Ω.

Crosstalk (C_{TK})
C_{TK} is a measure of unwanted signals coupled through from one channel to another because of parasitic capacitance.

An example calculation of crosstalk based on the setup in Figure 25 is as follows:

$$C_{TK} = -20\log_{10}|S_{RF1RF2}| \text{ [dB]}$$

where S_{RF1RF2} is the transmission coefficient measured from RF1 to RF2 with RF1 in the off position and RF2 in the on position. All unused switches are in the off position and terminated in a purely resistive load of 50 Ω.

Return Loss (RL)
RL is the magnitude of the reflection coefficient expressed in decibels, and the amount of reflected signal relative to the incident signal. A large return loss value indicates good matching.

An example calculation of return loss based on the setup in Figure 23 is as follows:

$$RL = -20\log_{10}|S_{11}| \text{ [dB]}$$

where S_{11} is the reflection coefficient of the port under test.

Input Third-Order Intermodulation Intercept (IIP3)
IIP3 is the intersection point of the fundamental P_{OUT} vs. P_{IN} extrapolated line and the third-order intermodulation products extrapolated line of a two tone test. IIP3 is a figure of merit that characterizes the switch linearity.

Input Second-Order Intermodulation Intercept (IIP2)
IIP2 is the intersection point of the fundamental P_{OUT} vs. P_{IN} extrapolated line and the second-order intermodulation products extrapolated line of a two tone test. IIP2 is a figure of merit that characterizes the switch linearity.

Second Harmonic (HD2)
HD2 is the amplitude of the second harmonic, where, for a signal whose fundamental frequency is f, the second harmonic has a frequency 2 f. This measurement is a single tone test, expressed with reference to the carrier signal (dBc).

Third Harmonic (HD3)
HD3 is the amplitude of the third harmonic, where, for a signal whose fundamental frequency is f, the third harmonic has a frequency 3 f. This measurement is a single tone test, expressed with reference to the carrier signal (dBc).

RF Power Rating
The RF power rating is the maximum level of RF power that passes through the switch without degradation to the switch lifetime when it is in the on state.

On Switching Time (t_{ON})
t_{ON} is the time it takes for the switch to turn on. It is measured from 50% of the control signal (INx) to 90% of the on level. No power is applied through the switch during this test (cold switched). The switch is terminated into a 50 Ω load.

Off Switching Time (t_{OFF})
t_{OFF} is the time it takes for the switch to turn off. It is measured from 50% of the control signal (INx) to 10% of the on level. No power is applied through the switch during this test (cold switched). The switch is terminated into a 50 Ω load.

Settling Time Rising Edge
The settling time rising edge is the time it takes for the power of an RF signal to settle within 0.05 dB of the final steady state value. The switch is terminated into a 50 Ω load.

Settling Time Falling Edge
The settling time falling edge is the time it takes for the power of an RF signal to settle within 0.05 dB of the final steady state value. The switch is terminated into a 50 Ω load.

Actuation Frequency
The actuation frequency refers to the speed at which the ADGM1304 can be switched on and off. It is dependent on both settling times and on to off switching times.

Wake-Up Time
The wake-up time is a measure of the time required for the voltage on V_{CP} to reach the typical voltage of 80 V after the device exits sleep mode.

Video Feedthrough
Video feedthrough is a measure of the spurious signals present at the RF ports of the switch when the control voltage is switched from high to low or from low to high without an RF signal present.

Internal Oscillator Frequency
The internal oscillator frequency is the value of the on-board oscillator that drives the gate control chip of the ADGM1304. The oscillator frequency can be overdriven through the EXTCLK pin.

Internal Oscillator Feedthrough
The internal oscillator feedthrough is the amount of internal oscillator signal that feeds through to the RF pins of the switch. This signal appears as a noise spur on the RFx and RFC pins of the switch at the frequency the oscillator is operating at and harmonics thereof.

On Resistance (R_{ON})
R_{ON} is the resistance of a switch in the closed/on state measured between the package pins. Measure resistance in 4-wire mode to null out any cabling or printed circuit board (PCB) series resistances.

On Resistance Stability (ΔR_{ON})
ΔR_{ON} is the variation in the on resistance of the switch over the lifetime of the switch.

Continuously on Lifetime
The continuously on lifetime measures how long the switch is left in a continuously on state. If the switch is left in the on position for an extended period, it affects the turn off mechanism of the device.

Actuation Lifetime
Actuation lifetime is the number of consecutive open-close-open cycles that can complete without the on resistance exceeding a specified limit and no occurrence of failures to open (FTO) or failures to close (FTC).

Cold Switching
Cold switching operates the switch in a mode so that no voltage differential exists between source and drain when the switch is closed and/or no current is flowing source to drain when the switch opens. All switches have longer lives when cold switched.

Hot Switching
Hot switching is operating the switch in a mode where a voltage differential exists between source and drain when the switch is closed and/or current is flowing RFx channel to RFC channel when the switch is opened. Hot switching results in a reduced switch life, depending on the magnitude of the open circuit voltage between the source and the drain.

EXTCLK Input Range
The EXTCLK input range is the allowable input frequency range when using an external oscillator to drive the gate control chip of the ADGM1304.

EXTCLK Input High Voltage (EV_{INH})
EV_{INH} is the minimum input voltage for a recognized high when using an external clock.

EXTCLK Input Low Voltage (EV_{INL})
EV_{INL} is the maximum input voltage for a recognized low when using an external clock.

I_{DD} Sleep Mode Current
I_{DD} sleep mode current is the measurement of the quiescent current of the chip after the device enters sleep mode.

Input High Voltage (V_{INH})
V_{INH} is the minimum input voltage for Logic 1.

Input Low Voltage (V_{INL})
V_{INL} is the maximum input voltage for Logic 0.

THEORY OF OPERATION

The ADGM1304 is a wideband single-pole, four-throw (SP4T) switch fabricated using Analog Devices, Inc., MEMS switch technology. This technology enables high power, low loss, low distortion gigahertz switches to be realized for demanding RF applications.

Figure 33 shows a stylized cross section graphic of the switch with dimensions. The switch is an electrostatically actuated cantilever beam connected in a three terminal configuration. Functionally, it is analogous to a field effect transistor (FET); the terminals can be used as a source, gate, and drain.

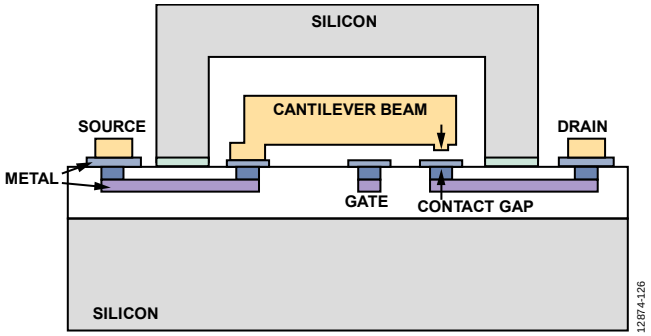

Figure 33. Cross Section of the MEMS Switch Design Showing the Cantilever Switch Beam (Not to Scale)

When a dc actuation voltage is applied between the gate electrode and the source (the switch beam), an electrostatic force generates, resulting in attracting the beam toward the substrate. A separate on-board charge pump IC generates the bias voltage; 80 V is used for actuation.

When the bias voltage between the gate and the source exceeds the threshold voltage of the switch, V_{TH}, the contacts on the beam touch the drain, which completes the circuit between the source and the drain and turns the switch on. When the bias voltage is removed, that is, 0 V on the gate electrode, the beam acts as a spring generating a sufficient restoring force to open the connection between the source and the drain, thus breaking the circuit and turning the switch off.

Figure 34 shows the SP4T MEMS switch and controller die within the LFCSP package. Some of the LFCSP plastic molding material is removed to allow the MEMS switch die (right) and controller die (left) with associated wire bonds to be visible. The silicon hermetically sealed cap covering the switch die can be seen on the right as a black rectangle. Hermetically sealing the switches improves the reliability and lifetime of the switches by keeping them in a controlled atmosphere. The switch contacts do not suffer from dry switching or low power switching lifetime degradation.

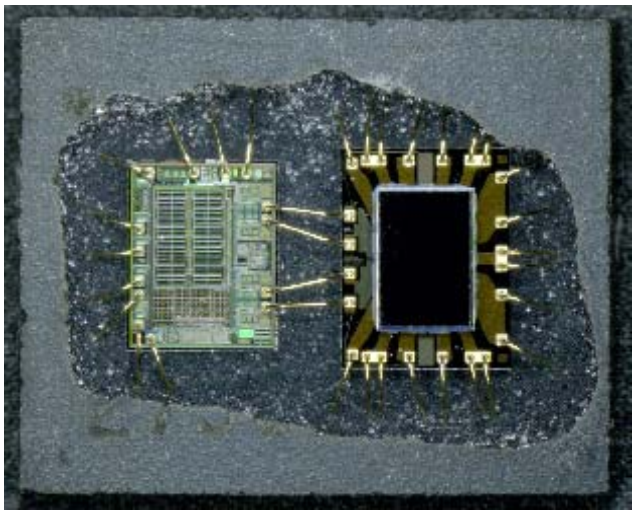

Figure 34. ADGM1304 LFCSP Package with Molding Compound Partially Removed to Show MEMS Switch Die (Right), Controller Die (Left), and Associated Wire Bonds

DIGITAL INTERFACE

The ADGM1304 is controlled via a parallel interface. Standard CMOS/LVTTL signals applied through this interface controls the actuation/release of all of the switch channels of the ADGM1304. Applied gate signals are boosted to give the required voltages needed to actuate the MEMS switches.

Pin IN1 to Pin IN4 control the switching functions of the ADGM1304. When Logic 1 is applied to one of the INx pins, the gate of the corresponding switch is activated, and the switch turns on. Conversely, when Logic 0 is applied to any of these pins, the switch turns off. Note that, it is possible to connect more than one RFx input to the RFC pin at a time. The truth table for the ADGM1304 is given in Table 5.

SLEEP MODE (SLEEP)

Use the SLEEP pin to shut down the ADGM1304. Tying the pin high places the device into a low power quiescent state, drawing only 1 μA supply current.

The low power state is especially useful for portable electronic applications and other applications that rely on low power states to deliver the desired field life.

Table 5. Truth Table (X Means Any Logic State)

IN1	IN2	IN3	IN4	SLEEP	RF1 to RFC	RF2 to RFC	RF3 to RFC	RF4 to RFC
0	0	0	0	0	Off	Off	Off	Off
0	0	0	1	0	Off	Off	Off	On
0	0	1	0	0	Off	Off	On	Off
0	0	1	1	0	Off	Off	On	On
0	1	0	0	0	Off	On	Off	Off
0	1	0	1	0	Off	On	Off	On
0	1	1	0	0	Off	On	On	Off
0	1	1	1	0	Off	On	On	On
1	0	0	0	0	On	Off	Off	Off
1	0	0	1	0	On	Off	Off	On
1	0	1	0	0	On	Off	On	Off
1	0	1	1	0	On	Off	On	On
1	1	0	0	0	On	On	Off	Off
1	1	0	1	0	On	On	Off	On
1	1	1	0	0	On	On	On	Off
1	1	1	1	0	On	On	On	On
X	X	X	X	1	Off	Off	Off	Off

DRIVER IC OSCILLATOR

A companion driver IC drives the MEMS switch. This driver IC converts the supply voltage to 80 V, which electrostatically actuates the switch, turning it on. The driver IC contains a control logic interface, a charge pump to generate 80 V, and a ramping drive circuit to shape the 80 V output voltage.

A nominal 11.5 MHz oscillator is part of the charge pump architecture. Although this oscillator is very low power, the 11.5 MHz signal is coupled to the switch and can be seen as a noise spur on the switch channels. The magnitude of this feedthrough noise spur is specified in Table 1 and is typically −115 dBm when one switch is on. When all four switches are simultaneously on, the feedthrough goes up to −94 dBm.

Note that the V_{DD} level and temperature changes affect the frequency of the noise spur. The maximum and minimum frequency range over temperature and voltage supply range is as detailed in Table 1.

EXTERNAL CLOCK (EXTCLK)

In some applications, using a known external clock source instead of the on-board oscillator is more convenient. The ADGM1304 offers an EXTCLK pin that allows a user to provide a clock source to drive the boost circuitry of the device. Setting the CLKSEL pin high activates the EXTCLK pin. The allowable frequency range of an external clock source is 20 MHz to 23 MHz.

In applications where the system noise floor level is important, set the CLKSEL pin high and the EXTCLK pin low to disable the charge pump and oscillator. In addition, there is zero oscillator feedthrough. To drive the switch with the charge pump disabled, apply an external 80 V drive voltage to the V_{CP} pin, and the digital interface can control the switch (see Table 5).

TYPICAL OPERATING CIRCUIT

Figure 35 shows the typical operating circuit for the ADGM1304. A 47 pF external capacitor is required on the V_{CP} pin; this is a holding capacitor for the 80 V gate drive voltage. V_{DD} is connected to 3.3 V. However, it can operate from 3.1 V to 3.3 V. RFGND is separated from AGND internally in the device.

It is recommended to connect RFGND to AGND using one large pad on the PCB to short together EP1 and EP2. Figure 35 displays the ADGM1304 configured to use the internal oscillator as the reference to the control circuit of the device. The SLEEP pin is tied to ground, thereby operating the device in normal operating mode.

To disable the internal oscillator and eliminate all oscillator feedthrough, set the CLKSEL pin to high and apply an 80 V dc directly to the V_{CP} pin. Then control the switches as normal via the logic control interface IN1 to IN4 pins.

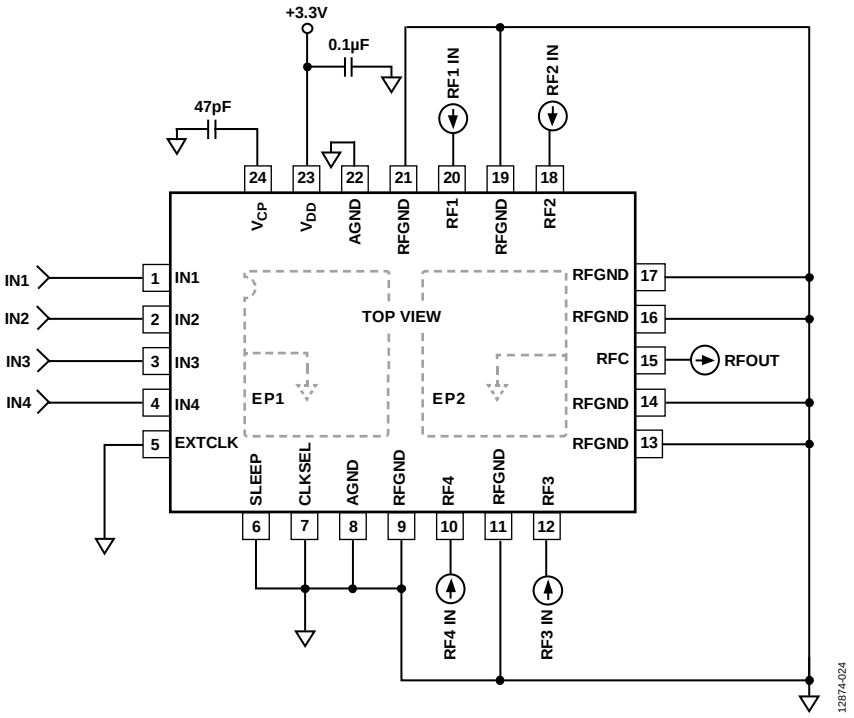

Figure 35. Typical Operating Circuit

APPLICATIONS INFORMATION

FLOATING NODE AVOIDANCE

As outlined in the Theory of Operation section, applying 80 V on the gate electrode under the beam of the switch creates an electrostatic attraction force that pulls the beam down to actuate the switch. Without an external impedance to a dc voltage reference, charges can increase on the switch terminals, causing voltages to float to unknown levels, which can lead to unreliable actuation behavior that may damage the switch. To ensure correct and reliable switch actuation, ensure that all switch nodes have a dc voltage reference, for example, a connection to another active component with an internal voltage reference or an impedance to ground. Figure 36 to Figure 39 show examples of four cases to avoid where floating nodes can occur when using the switch. These cases include the following conditions:

- The RFx pins must not be open circuit.
- Connecting a series capacitor directly to the switch can result in a floating node condition.
- Connecting the RFx pin of two switches together directly or connecting RFC to RFx can result in a floating node condition.

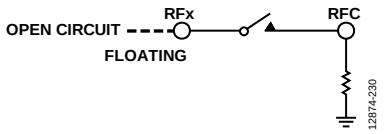

Figure 36. RFx Pins Left Open Circuit

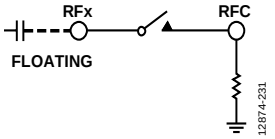

Figure 37. Connecting a Series Capacitor Directly to the Switch

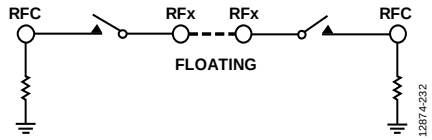

Figure 38. Connecting the RFx Pin of Two Switches Directly Together

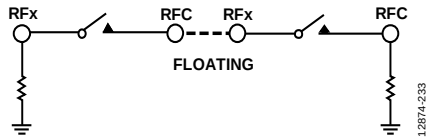

Figure 39. Connecting RFC to RFx

Providing a dc voltage reference to the switch ensures correct gate to beam voltage differential to drive the switch and prevents floating nodes and unreliable actuation. In a typical application, a 50 Ω termination connected to the switch provides a constant dc voltage reference. Most amplifiers and other active devices have an internal dc voltage reference. Therefore, directly connecting these devices to the switch provides a dc voltage reference and avoids any floating node issues. If there is no inherent dc voltage reference in the application circuit, a 10 MΩ shunt resistor or inductor on the source (RFx) pin of the MEMS switch must be added to provide a voltage reference. The addition of external shunt resistors increases the leakage above the specification shown in Table 1. Figure 40 shows this type of voltage reference configuration.

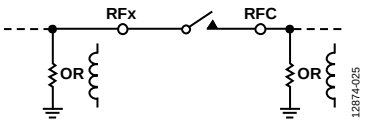

Figure 40. Switch Configuration Providing a Voltage Reference

Avoid a floating node condition on the RFC pin. If the RFC pin is left floating to an unknown voltage level when the switch is off, there is a hot switching risk when the switch is subsequently toggled on. A 10 MΩ shunt resistor can also be used to mitigate floating node risks on the RFC pin.

Figure 41 and Figure 42 illustrate typical cascaded switch use cases and the corresponding schemes to mitigate floating node risks.

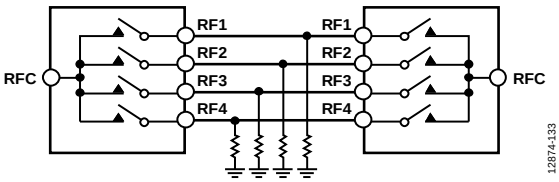

Figure 41. Two ADGM1304 Devices Connected Together with Shunt Resistors to Mitigate Floating Nodes

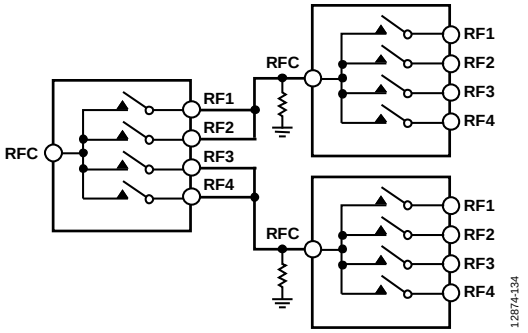

Figure 42. Three ADGM1304 Devices Connected Together with Shunt Resistors to Mitigate Floating Nodes

The path between the two switches needs a voltage reference to ground; otherwise, the path can float to an unknown voltage and subsequently cause unreliable actuations, possibly leading to hot switching events or switches remaining in the on state.

To avoid hot switching events or switches remaining in the on state, add high value resistors (typically 10 MΩ) to ground to the channel of the MEMS switch, which is cascaded to another MEMS switch, as shown in Figure 41 and Figure 42. These shunt resistors create a dc voltage reference.

Avoid connecting large shunt capacitors directly to the switch where possible. A capacitor can store a charge and can potentially give rise to hot switching events when the switch opens or closes where there are no alternative discharge paths, which affects the cycle lifetime of the switch.

CONTINUOUSLY ON LIFETIME

Turning the switch on for a long period affects the lifetime of the switch. The ADGM1304 has a continuous on lifetime specification of 7.2 years typical (see Table 1). The continuously on lifetime time of the switch must not exceed this specification when the switch is in the on state to preserve good turn off reliability.

Figure 43 shows the continuously on lifetime reliability data taken at 50°C for 31 parts. In the case of 50% of the population, expect a failure time of approximately 7.2 years. As the temperature increases above 50°C, the continuously on lifetime degrades significantly. When using the switch in duty cycle, less than 50% of the lifetime is significantly better.

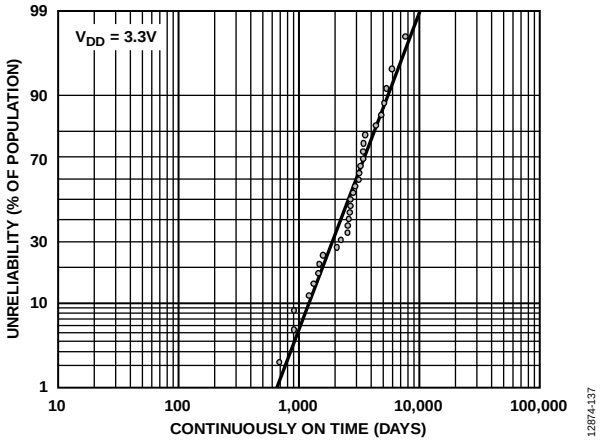

Figure 43. Continuously on Lifetime, V_{DD} = 3.3 V, 50°C, Sample Size 31 Parts

SUGGESTED APPLICATION CIRCUITS

SWITCHABLE RF ATTENUATOR

It is common to see RF attenuator networks used in RF instrumentation equipment such as vector network analyzers, spectrum analyzers, and signal generators. Routing RF signals through an attenuator can enable the equipment to accept higher power signals and, therefore, increase the dynamic range of the instrument. In RF attenuation applications like the vector network analyzers, spectrum analyzers, and signal generators, maintaining the bandwidth of the signal after it passes through the network is critical. Any degradation of the signal reduces the performance of the equipment. Therefore, the RF characteristics of the switches used for routing is an integral part of the quality of an attenuator network.

The ADGM1304 MEMS switch with low flat insertion loss, very wide RF bandwidth, and high reliability is suited for using it as a switchable RF attenuator. The ADGM1304, as an SP4T switch, also brings added flexibility. Figure 44 shows an example attenuation network configuration using two ADGM1304 switches and three different attenuators. The fourth channel of the switches is used as a nonattenuated route in Figure 44.

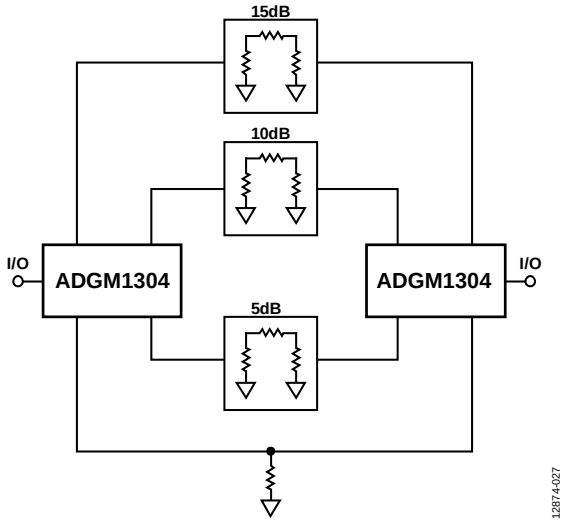

Figure 44. Switching RF Attenuators Using ADGM1304 MEMS Switches

RECONFIGURABLE RF FILTER

A reconfigurable RF filter is advantageous in many RF front-end applications. A reconfigurable RF filter provides more saved space. As space becomes more constrained in applications, the option to have an economical reconfigurable RF filter instead of individual frequency dependent filters is attractive.

The ADGM1304 with low flat insertion loss, very wide RF bandwidth, low parasitic, low capacitance, and high linearity is needed to turn on the lump components (capacitor, inductor), which make the MEMS switch suited for reconfigurable filter application.

In applications such as wireless communications or mobile radios, the number of bands and/or modes constantly increases. A reconfigurable RF filter allows more bands/modes to be covered using the same components.

Figure 45 shows an example of a reconfigurable band-pass filter. The topology shown is of a generalized two section, inductively coupled, single-ended band-pass filter, nominally centered on 400 MHz (UHF band). Note the MEMS switches are positioned in series with each of the shunt inductors.

The function of the switches includes or omits a shunt inductor from the circuit. Changing the shunt inductor value affects the bandwidth and center frequency of the filter. Using inductance values from 15 nH to 30 nH significantly alters the bandwidth and center frequency, allowing the filter to dynamically configure to operate in the ultrahigh frequency (UHF) or very high frequency (VHF) bands while preserving the 50 Ω match on the input and output ports. The low R_{ON} value and large bandwidth of the MEMS switch makes it an ideal choice for this application. The low R_{ON} reduces the negative effect a series resistance has on the quality factor of the shunt inductor. The large bandwidth enables higher frequency band-pass filters.

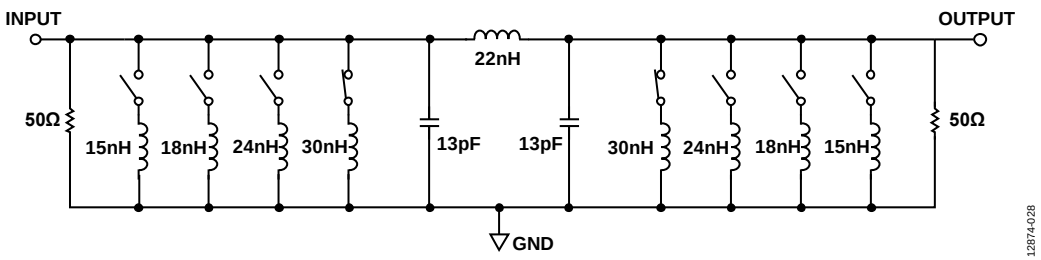

Figure 45. Reconfigurable Band-Pass Filter Realized Using Two ADGM1304 MEMS Switches

HANDLING PRECAUTIONS

ESD PRECAUTIONS

All RFx pins of the ADGM1304 pass the following ESD limits:

- 100 V, Class 0 human body model (HBM), ANSI/ESDA/JEDEC JS-001-2010
- 500 V, Class C2 field-induced charged-device model (FICDM), JEDEC JESD22_C101E

All the RFx pins are rated to 500 V FICDM, making the device safe for automated handling and assembly process, according to the Industry Council on ESD Target Levels, White Paper 2, "*A Case for Lowering Component Level CDM ESD Specifications and Requirements.*" Refer to the Absolute Maximum Ratings section for more information.

ELECTRICAL OVERSTRESS (EOS) PRECAUTIONS

A stored charge inadvertently conducted through the switches can result in immediate permanent damage to the ADGM1304. Therefore, observe the following precautions:

- Treat the ADGM1304 as a static sensitive device and observe all normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps or other ESD control devices, and storing unused devices in conductive foam.
- Avoid running measurement instruments (for example, digital multimeters (DMMs) in autorange modes). Some instruments can generate large transient compliance voltages when switching between ranges.
- Use the highest practical DMM range setting (that is, the lowest resolution) for resistance measurements minimizing compliance voltages.
- Coaxial cables can store charge and lead to EOS when directly connected to the switch. Discharge cables before connecting directly to the switch.
- Avoid connecting large capacitive terminations directly to the switch. A shunt capacitor can store a charge that can potentially give rise to hot switching events when the switch opens or closes, affecting the lifetime of the switch. Figure 46 shows where to avoid large capacitive terminations.

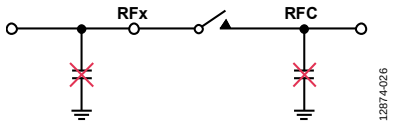

Figure 46. Avoid Large Capacitive Terminations Directly Connected to the Switch

DC Voltage Range

The dc voltage range of the switch is ±6 V (see Table 1), which is the dc signal range the switch is specified to carry.

Voltage Standoff Limit

The standoff voltage is the highest voltage that can be applied to the RFC drain electrode of the switch without adversely affecting the performance or reliability of the switch.

The standoff voltage limit of the switch is 100 V on the RFC pin (see Table 2).

MECHANICAL SHOCK PRECAUTIONS

The device passes an extensive mechanical shock qualification process. Table 6 shows a summary of the mechanical shock qualification tests used on the ADGM1304. These tests validate the robustness of the device to mechanical shocks.

Table 6. Mechanical Qualification Summary

Parameter	Qualification
Mechanical Shock	Powered (PMS) IEC 60068-2-27
Random Drop	AEC-Q100 Test G5, five drops from 0.6 m
Vibration Testing	MIL-STD-883, M2007.3, Condition B, 20 Hz to 2000 Hz at 50 *g*
Group D Sub 4 MIL-STD-883, M5005	Mechanical shock, 1500 *g*, 0.5 ms; vibration 50 *g* sine sweep, 20 Hz to 2000 Hz; acceleration 30,000 *g*

The device must be handled with care and, as is the case with electromechanical relays, do not use the device if dropped and ensure there are minimal mechanical shocks during the handling and manufacturing of the device.

Figure 47 shows examples of loose device handling situations to avoid due to mechanical shock and ESD event risk.

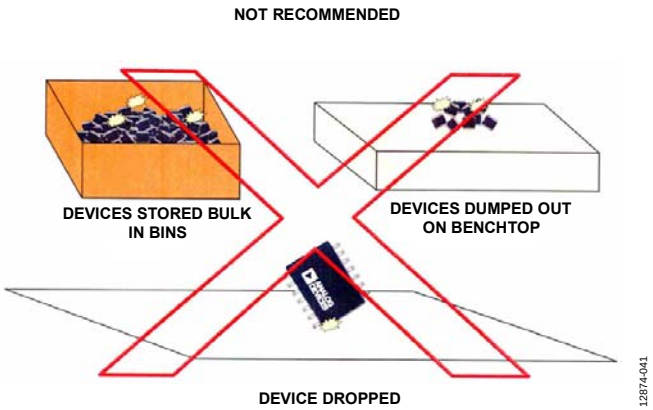

Figure 47. Device Handling Precautions

OUTLINE DIMENSIONS

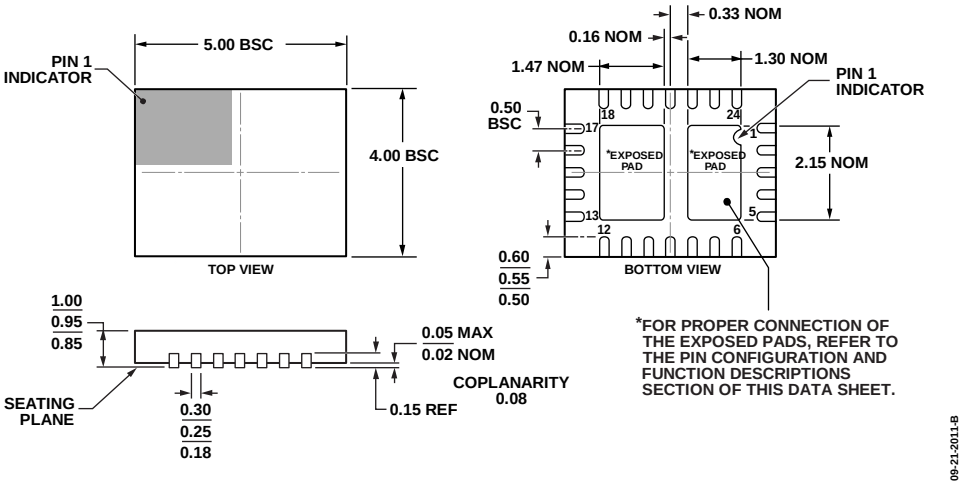

Figure 48. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 4 mm Body, Very Thin Quad
(CP-24-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADGM1304JCPZ-R2	0°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-9
ADGM1304JCPZ-RL7	0°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-9
EVAL-ADGM1304EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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