

# NB3N51032

## 3.3 V, Crystal to 25 MHz, 100 MHz, 125 MHz and 200 MHz Dual HCSL/LVDS Clock Generator

The NB3N51032 is a precision, low phase noise clock generator that supports PCI Express and Ethernet requirements. The device accepts a 25 MHz fundamental mode parallel resonant crystal and generates a differential HCSL output at 25 MHz, 100 MHz, 125 MHz or 200 MHz clock frequencies. Outputs can interface with LVDS with proper termination (See Figure 10). The NB3N51032 provides selectable spread options of  $-0.5\%$  and  $-0.75\%$  for applications demanding low Electromagnetic Interference (EMI) as well as optimum performance with no spread option.

### Features

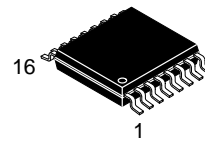
- Uses 25 MHz Fundamental Mode Parallel Resonant Crystal
- External Loop Filter is Not Required
- HCSL Differential Output or LVDS with Proper Termination
- Four Selectable Multipliers of the Input Frequency
- Output Enable with Tri-State Outputs
- PCIe Gen 1, Gen 2, Gen 3 Compliant
- Spread of  $-0.5\%$ ,  $-0.75\%$  and No Spread
- Phase Noise: @ 100 MHz
 

| Offset  | Noise Power   |
|---------|---------------|
| 100 Hz  | $-88$ dBc/Hz  |
| 1 kHz   | $-118$ dBc/Hz |
| 10 kHz  | $-131$ dBc/Hz |
| 100 kHz | $-132$ dBc/Hz |
| 1 MHz   | $-144$ dBc/Hz |
| 10 MHz  | $-155$ dBc/Hz |
- Typical Period Jitter RMS of 1.5 ps
- Operating Supply Voltage Range  $3.3\text{ V} \pm 5\%$
- Industrial Temperature Range  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
- Functionally Compatible with IDT557-03, IDT5V41065, IDT5V41235 with enhanced performance
- These are Pb-Free Devices



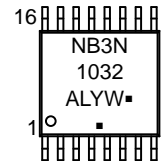
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TSSOP-16  
DT SUFFIX  
CASE 948F

### MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

### Applications

- Networking
- Consumer
- Computing and Peripherals
- Industrial Equipment
- PCIe Clock Generation Gen 1, Gen 2 and Gen 3
- Gigabit Ethernet
- FB DIMM

### End Products

- Switch and Router
- Set Top Box, LCD TV
- Servers, Desktop Computers
- Automated Test Equipment

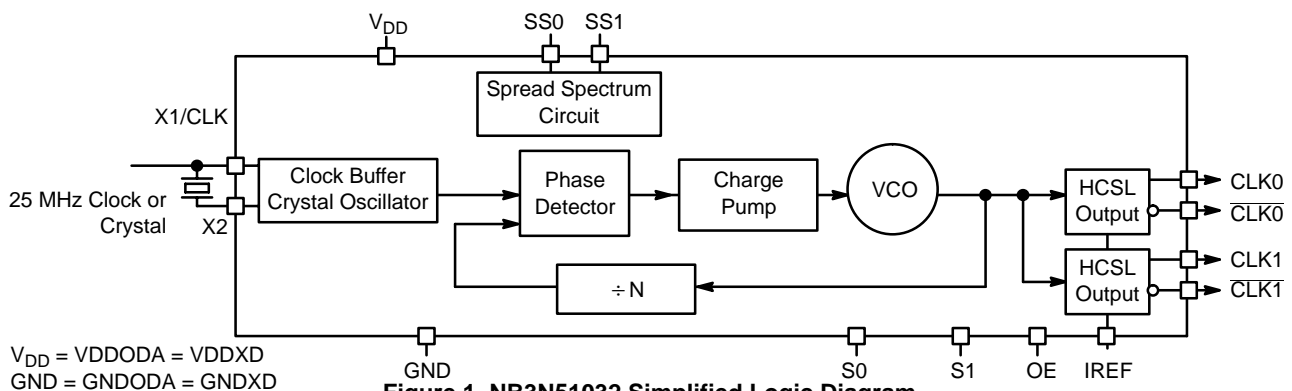
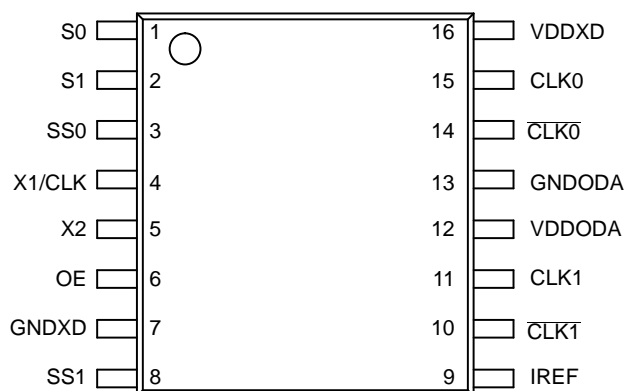


Figure 1. NB3N51032 Simplified Logic Diagram

## NB3N51032



**Table 1. PIN DESCRIPTION**

| Pin | Symbol                   | I/O                 | Description  |
|-----|--------------------------|---------------------|--|
| 1   | S0                       | Input               | LVTTL/LVCMOS frequency select input 0. Internal pullup resistor to VDDXD. See output select table 2 for details. |
| 2   | S1                       | Input               | LVTTL/LVCMOS frequency select input 1. Internal pullup resistor to VDDXD. See output select table 2 for details. |
| 3   | SS0                      | Input               | LVTTL/LVCMOS Spread select input 0. Internal pullup resistor to VDDXD. See Spread selection Table 3 for details. |
| 4   | X1/CLK                   | Input               | Crystal or Clock input. Connect to 25 MHz crystal source or single-ended clock.                                  |
| 5   | X2                       | Input               | Crystal input. Connect to a 25 MHz crystal or leave unconnected for clock input.                                 |
| 6   | OE                       | Input               | Output enable tri-states output when connected to GND. Internal pullup resistor to VDDXD.                        |
| 7   | GNDXD                    | Power Supply        | Ground 0 V. This pin provides GND return path for the device.  |
| 8   | SS1                      | Input               | LVTTL/LVCMOS Spread select input 1. Internal pullup resistor to VDDXD. See Spread selection Table 3 for details. |
| 9   | IREF                     | Output              | Output current reference pin. Precision resistor (typ. 475 Ω) is connected to set the output current.            |
| 10  | $\overline{\text{CLK1}}$ | HCSL or LVDS Output | Inverted clock output. (For LVDS levels see Figure 10)   |
| 11  | CLK1                     | HCSL or LVDS Output | Noninverted clock output. (For LVDS levels see Figure 10)  |
| 12  | VDDODA                   | Power Supply        | Positive supply voltage pin connected to +3.3 V supply voltage.  |
| 13  | GNDODA                   | Power Supply        | Ground 0 V. These pins provide GND return path for the devices.  |
| 14  | $\overline{\text{CLK0}}$ | HCSL or LVDS Output | Inverted clock output. (For LVDS levels see Figure 10)   |
| 15  | CLK0                     | HCSL or LVDS Output | Noninverted clock output. (For LVDS levels see Figure 10)  |
| 16  | VDDXD                    | Power Supply        | Positive supply voltage pin connected to +3.3 V supply voltage.  |

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**Table 2. OUTPUT FREQUENCY SELECT TABLE WITH 25MHz CRYSTAL**

| S1* | S0* | CLK Multiplier | f <sub>CLKout</sub> (MHz) |
|-----|-----|----------------|---------------------------|
| L   | L   | 1x             | 25                        |
| L   | H   | 4x             | 100                       |
| H   | L   | 5x             | 125                       |
| H   | H   | 8x             | 200                       |

\*Pins S1 and S0 default high when left open.

## Recommended Crystal Parameters

|                              |                    |
|------------------------------|--------------------|
| Crystal                      | Fundamental AT-Cut |
| Frequency                    | 25 MHz             |
| Load Capacitance             | 16–20 pF           |
| Shunt Capacitance, C0        | 7 pF Max           |
| Equivalent Series Resistance | 50 Ω Max           |
| Initial Accuracy at 25 °C    | ±20 ppm            |
| Temperature Stability        | ±30 ppm            |
| Aging                        | ±20 ppm            |

**Table 3. SPREAD SELECTION TABLE**

| SS1* | SS0* | Spread%   | Spread Type |
|------|------|-----------|-------------|
| 0    | 0    | No Spread | N/A         |
| 0    | 1    | -0.5      | Down        |
| 1    | 0    | -0.75     | Down        |
| 1    | 1    | No Spread | N/A         |

\*Pins S1 and S0 default high when left open.

**Table 4. ATTRIBUTES**

| Characteristic   | Value                |
|--|----------------------|
| ESD Protection Human Body Model                                | 2 kV                 |
| Pull-up Resistor (Pins OE, S0, S1, SS0 and SS1)                | 50 kΩ                |
| Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1) | Level 1              |
| Flammability Rating Oxygen Index: 28 to 34                     | UL 94 V-0 @ 0.125 in |
| Transistor Count   | 132000               |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test         |                      |

1. For additional information, see Application Note AND8003/D.

**Table 5. MAXIMUM RATINGS** (Note 2)

| Symbol           | Parameter  | Rating                           | Unit         |
|------------------|--|----------------------------------|--------------|
| V <sub>DD</sub>  | Positive Power Supply with respect to GND (VDDXD and VDDODA) | 4.6                              | V            |
| V <sub>I</sub>   | Input Voltage with respect to GND (V <sub>IN</sub> )         | -0.5 V to V <sub>DD</sub> +0.5 V | V            |
| T <sub>A</sub>   | Operating Temperature Range                                  | -40 to +85                       | °C           |
| T <sub>stg</sub> | Storage Temperature Range                                    | -65 to +150                      | °C           |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient) (Note 3)            | 0 lfpm<br>500 lfpm               | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)                        | 50                               | °C/W         |
| T <sub>sol</sub> | Wave Solder  | 265                              | °C           |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

**Table 6. DC CHARACTERISTICS** (V<sub>DD</sub> = 3.3 V ±5%, GND = 0 V, T<sub>A</sub> = -40°C to +85°C, Note 4)

| Symbol              | Characteristic  | Min       | Typ | Max                   | Unit |
|---------------------|---|-----------|-----|-----------------------|------|
| V <sub>DD</sub>     | Power Supply Voltage (VDDXD and VDDODA)                                   | 3.135     | 3.3 | 3.465                 | V    |
| GND                 | Power Supply Ground (GNDXD and GNDODA)                                    |           | 0   |                       | V    |
| I <sub>DD</sub>     | Power Supply Current, 200 MHz Output, -0.75% spread                       |           | 100 |                       | mA   |
| I <sub>DDOE</sub>   | Power Supply Current when OE is Set Low                                   |           | 55  |                       | mA   |
| V <sub>IH</sub>     | Input HIGH Voltage (X1/CLK, S0, S1, SS0, SS1 and OE)                      | 2000      |     | V <sub>DD</sub> + 300 | mV   |
| V <sub>IL</sub>     | Input LOW Voltage (X1/CLK, S0, S1, SS0, SS1 and OE)                       | GND – 300 |     | 800                   | mV   |
| V <sub>OH</sub>     | Output HIGH Voltage for HCSL Output (Note 5)                              | 660       |     | 850                   | mV   |
| V <sub>OL</sub>     | Output LOW Voltage for HCSL Output (Note 5)                               | -150      | 0   |                       | mV   |
| V <sub>cross</sub>  | Crossing Voltage Magnitude (Absolute) for HCSL Output (Notes 6 and 7)     | 250       |     | 550                   | mV   |
| ΔV <sub>cross</sub> | Change in Magnitude of V <sub>cross</sub> for HCSL Output (Notes 6 and 8) |           |     | 150                   | mV   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. VDDXD and VDDODA power pins must be shorted to power supply voltage V<sub>DD</sub> and GNDXD and GNDODA ground pins must be shorted to power supply ground GND. Measurement taken with outputs terminated with R<sub>S</sub> = 33.2 Ω, R<sub>L</sub> = 49.9 Ω, with test load capacitance of 2 pF and current biasing resistor set at 475 Ω. See Figure 9. Guaranteed by characterization.

5. Measurement taken from single-ended waveform.

6. Measured at crossing point where the instantaneous voltage value of the rising edge of CLKx+ equals the falling edge of CLKx-.

7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

8. Defined as the total variation of all crossing voltage of rising CLKx+ and falling CLKx-. This is maximum allowed variance in the V<sub>CROSS</sub> for any particular system.

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**Table 7. AC CHARACTERISTICS** ( $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; Note 9)

| Symbol             | Characteristic  | Min | Typ  | Max                    | Unit          |
|--------------------|---|-----|--|------------------------|---------------|
| $f_{CLKIN}$        | Clock/Crystal Input Frequency   |     | 25   |                        | MHz           |
| $f_{CLKOUT}$       | Output Clock Frequency  | 25  |  | 200                    | MHz           |
| $\Phi_{NOISE}$     | Phase-Noise Performance<br><br>$f_{CLKOUT} = 100\text{ Mhz}$<br>@ 100 Hz offset from carrier<br>@ 1 kHz offset from carrier<br>@ 10 kHz offset from carrier<br>@ 100 kHz offset from carrier<br>@ 1 MHz offset from carrier<br>@ 10 MHz offset from carrier |     | -88<br>-118<br>-131<br>-132<br>-144<br>-155  |                        | dBc/Hz        |
| $t_{JITTER}$       | Period Jitter Peak-to-Peak (Note 10)<br>Period Jitter RMS (Note 10)<br>Cycle-Cycle RMS Jitter (Note 11)<br>Cycle-to-Cycle Peak to Peak Jitter (Note 11)   |     | $f_{CLKOUT} = 200\text{ Mhz}$<br>10<br>$f_{CLKOUT} = 200\text{ MHz}$<br>1.5<br>$f_{CLKOUT} = 200\text{ MHz}$<br>2.0<br>$f_{CLKOUT} = 200\text{ MHz}$<br>20 | 20<br>3.0<br>5.0<br>35 | ps            |
| $t_{JIT(\Phi)}$    | Phase RMS Jitter, Integration Range 12 kHz to 20 MHz  |     | 0.5  |                        | ps            |
| $f_{MOD}$          | Spread Spectrum Modulation Frequency  | 30  | 31.5   | 33                     | kHz           |
| $SS_{RED}$         | Spectral Reduction, $f_{CLKOUT}$ of 100 MHz with -0.5% spread, 3 <sup>rd</sup> Harmonic (Note 12)   |     | -10  |                        | dB            |
| $t_{SKEW}$         | Within Device Output to Output Skew   |     |  | 40                     | ps            |
| Eppm               | Frequency Synthesis Error, All Outputs  |     | 0  |                        | ppm           |
| $t_{SPREAD}$       | Spread Spectructron Transition Time<br>(Stabilization Time After Spread Spectrum Changes)   | 7   |  | 30                     | ms            |
| $t_{OE}$           | Output Enable/Disable Time (Note 13)  |     |  | 10                     | $\mu\text{s}$ |
| $t_{DUTY\_CYCLE}$  | Output Clock Duty Cycle (Measured at cross point)   | 45  | 50   | 55                     | %             |
| $t_R$              | Output Risetime (Measured from 175 mV to 525 mV, Figure 11)   | 175 |  | 700                    | ps            |
| $t_F$              | Output Falltime (Measured from 525 mV to 175 mV, Figure 11)   | 175 |  | 700                    | ps            |
| $\Delta t_R$       | Output Risetime Variation (Single-Ended)  |     |  | 125                    | ps            |
| $\Delta t_F$       | Output Falltime Variation (Single-Ended)  |     |  | 125                    | ps            |
| Stabilization Time | Stabilization Time From Powerup $V_{DD} = 3.3\text{ V}$   |     | 3.0  |                        | ms            |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

9. VDDXD and VDDODA power pins must be shorted to power supply voltage  $V_{DD}$  and GNDXD and GNDODA ground pins must be shorted to power supply ground GND. Measurement taken from differential output on single-ended channel terminated with  $R_S = 33.2\ \Omega$ ,  $R_L = 49.9\ \Omega$ , with test load capacitance of 2 pF and current biasing resistor set at 475  $\Omega$ . See Figure 9. Guaranteed by characterization.

10. Sampled with 10000 cycles.

11. Sampled with 1000 cycles.

12. Spread spectrum clocking enabled.

13. Output pins are tri-stated when OE is asserted LOW. Output pins are driven differentially when OE is HIGH.

**Table 8. AC ELECTRICAL CHARACTERISTICS – PCI EXPRESS JITTER SPECIFICATIONS,**

$V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$

| Symbol                      | Parameter                                   | Test Conditions   |              | Min | Typ  | Max  | PCIe Industry Spec | Unit |
|-----------------------------|---|---|--------------|-----|------|------|--------------------|------|
| tj (PCIe Gen 1)             | Phase Jitter Peak-to-Peak (Notes 15 and 18) | f = 100 MHz, 25 MHz Crystal Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2) | SSOFF        |     | 10   | 20   | 86                 | pS   |
|                             |   |   | SSON (-0.5%) |     | 19   | 28   |                    |      |
| tREFCLK_HF_RMS (PCIe Gen 2) | Phase Jitter RMS (Notes 16 and 18)          | f = 100 MHz, 25 MHz Crystal Input High Band: 1.5 MHz – Nyquist (clock frequency/2)    | SSOFF        |     | 1.0  | 1.8  | 3.1                | pS   |
|                             |   |   | SSON (-0.5%) |     | 1.1  | 1.9  |                    |      |
| tREFCLK_LF_RMS (PCIe Gen 2) | Phase Jitter RMS (Notes 16 and 18)          | f = 100 MHz, 25 MHz Crystal Input Low Band: 10 kHz – 1.5 MHz                          | SSOFF        |     | 0.1  | 0.15 | 3                  | pS   |
|                             |   |   | SSON (-0.5%) |     | 0.8  | 1.1  |                    |      |
| tREFCLK_RMS (PCIe Gen 3)    | Phase Jitter RMS (Notes 17 and 18)          | f = 100 MHz, 25 MHz Crystal Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2) | SSOFF        |     | 0.35 | 0.7  | 1                  | pS   |
|                             |   |   | SSON (-0.5%) |     | 0.55 | 0.8  |                    |      |

14. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
15. Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86 ps peak-to-peak for a sample size of  $10^6$  clock periods.
16. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1 ps RMS for tREFCLK\_HF\_RMS (High Band) and 3.0 ps RMS for tREFCLK\_LF\_RMS (Low Band).
17. RMS jitter after applying system transfer function for the common clock architecture.
18. VDDXD and VDDODA power pins must be shorted to power supply voltage  $V_{DD}$  and GNDXD and GNDODA ground pins must be shorted to power supply ground GND. Measurement taken from differential output on single-ended channel terminated with  $R_S = 33.2\ \Omega$ ,  $R_L = 50\ \Omega$ , with test load capacitance of 2 pF and current biasing resistor set at 475  $\Omega$ . See Figure 11. This parameter is guaranteed by characterization. Not tested in production.

PHASE NOISE

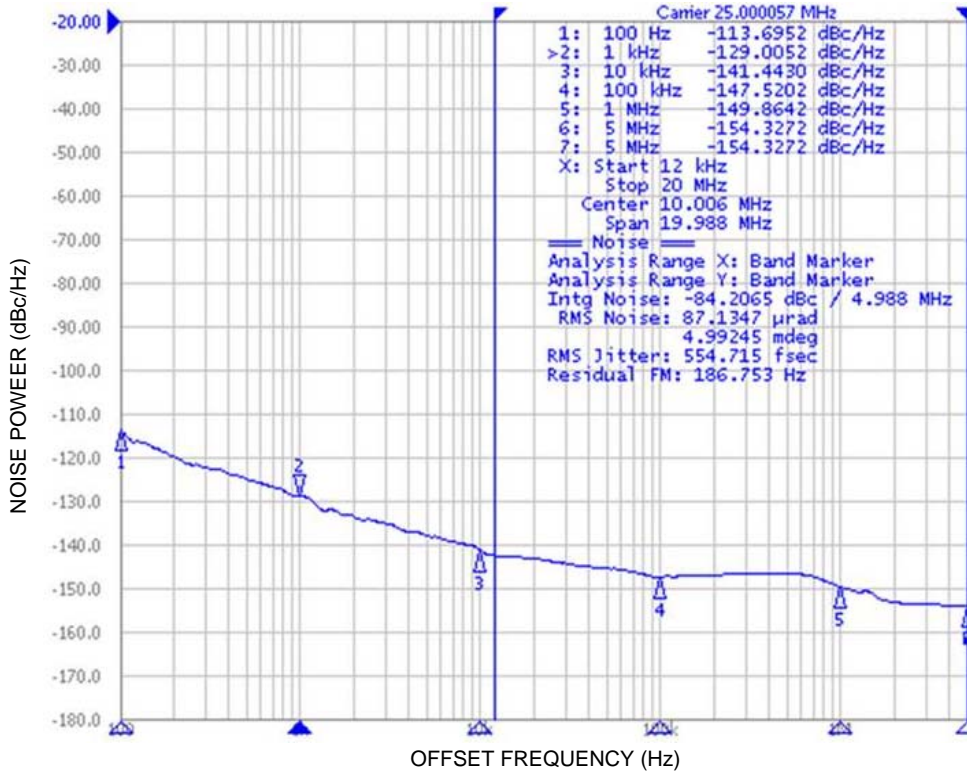


Figure 3. Typical Phase Noise Plot at 25 MHz; ( $f_{CLKIN}$  = 25 MHz Crystal ,  $f_{CLKOUT}$  = 25 MHz SS OFF, RMS Phase Jitter for Integration Range 12 kHz to 20 MHz = 554 fs, Output Termination = HCSL type)

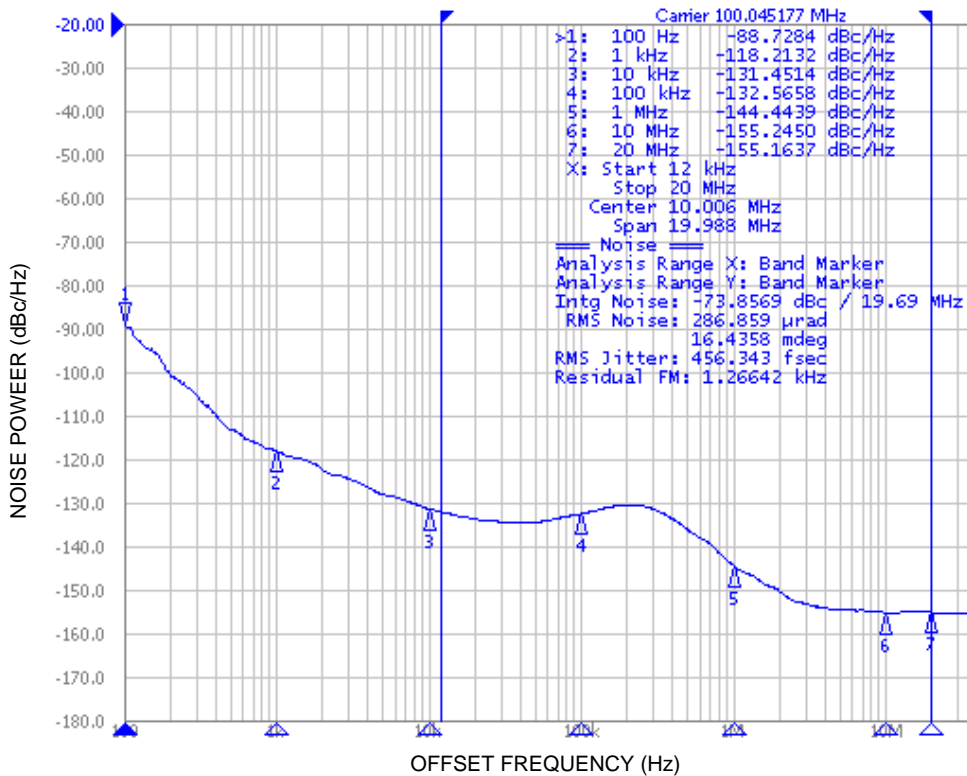


Figure 4. Typical Phase Noise Plot at 100 MHz; ( $f_{CLKIN}$  = 25 MHz Crystal ,  $f_{CLKOUT}$  = 100 MHz SS OFF, RMS Phase Jitter for Integration Range 12 kHz to 20 MHz = 456 fs, Output Termination = HCSL type)

PHASE NOISE

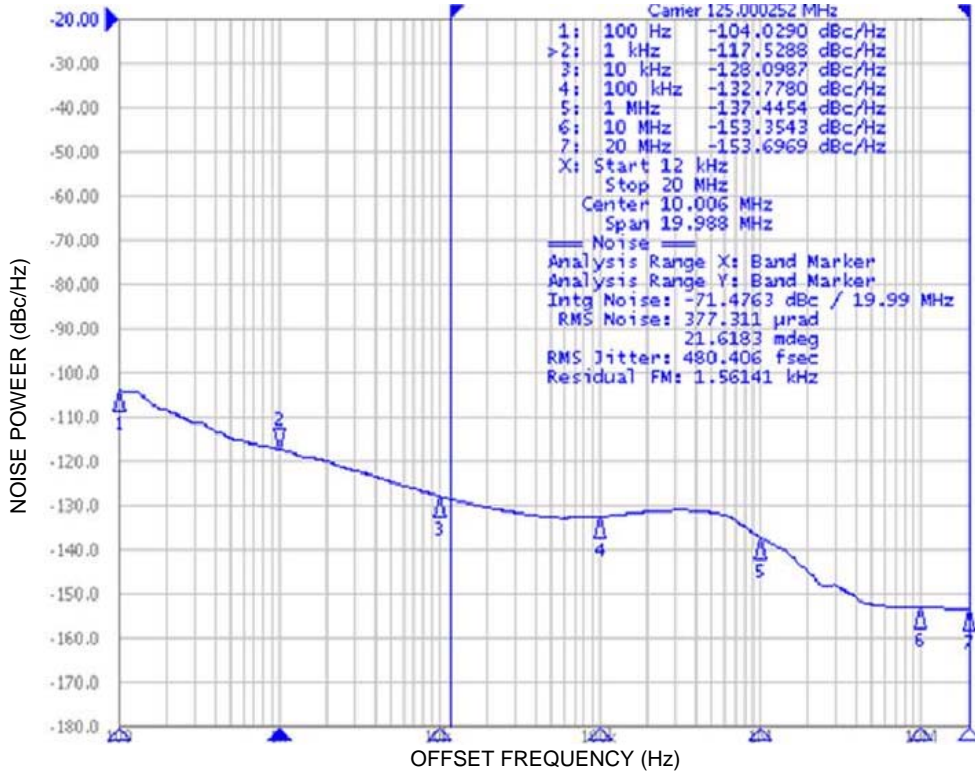


Figure 5. Typical Phase Noise Plot at 125 MHz; ( $f_{CLKIN} = 25$  MHz Crystal ,  $f_{CLKOUT} = 125$  MHz SS OFF, RMS Phase Jitter for Integration Range 12 kHz to 20 MHz = 480 fs, Output Termination = HCSL type)

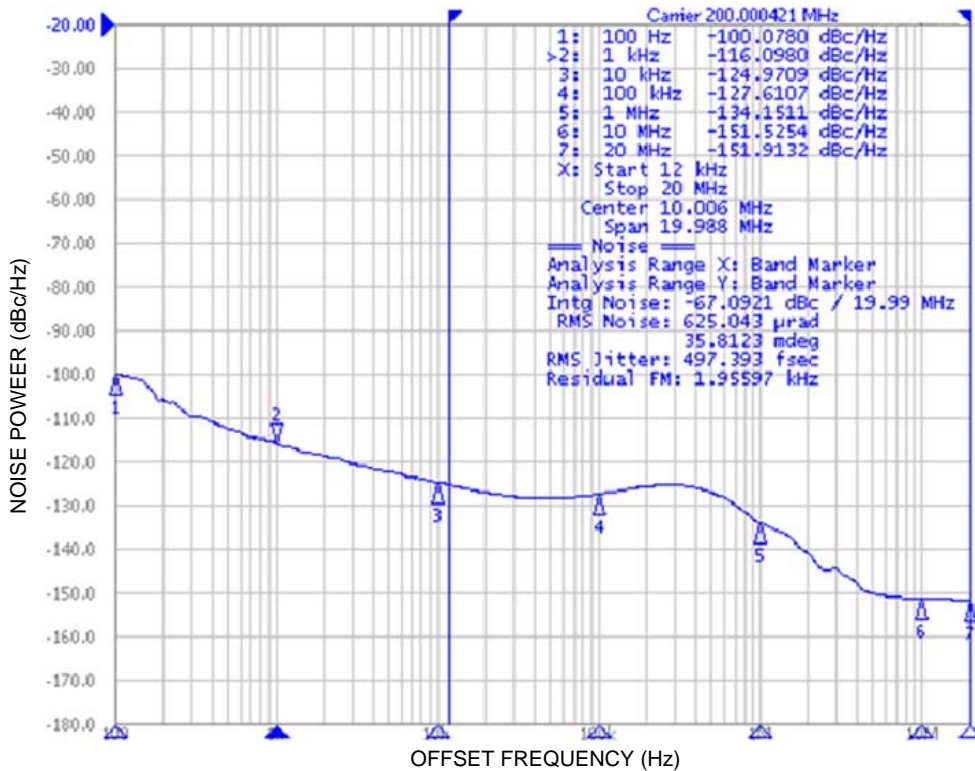


Figure 6. Typical Phase Noise Plot at 200 MHz; ( $f_{CLKIN} = 25$  MHz Crystal ,  $f_{CLKOUT} = 200$  MHz SS OFF, RMS Phase Jitter for Integration Range 12 kHz to 20 MHz = 497 fs, Output Termination = HCSL type)



APPLICATION INFORMATION

**Crystal Input Interface**

Figure 7 shows the NB3N51032 device crystal oscillator interface using a typical parallel resonant crystal. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors, C<sub>1</sub> and C<sub>2</sub>, need to consider the stray capacitances of the board and are used to match the nominally required crystal load capacitance C<sub>L</sub>. A parallel crystal with loading capacitance C<sub>L</sub> = 18 pF would use C<sub>1</sub> = 26 pF and C<sub>2</sub> = 26 pF

as nominal values, assuming approximately 2 pF of stray capacitance per trace and approximately 8 pF of internal capacitance.

$$C_L = (C_1 + C_{stray} + C_{in}) / 2; C_1 = C_2$$

The frequency accuracy and duty cycle skew can be fine-tuned by adjusting the C<sub>1</sub> and C<sub>2</sub> values. For example, increasing the C<sub>1</sub> and C<sub>2</sub> values will reduce the operational frequency.

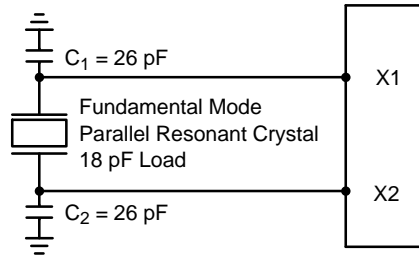


Figure 7. Crystal Interface Loading

**Power Supply Filter**

In order to isolate the NB3N51032 from system power supply, noise decoupling is required. The 10 μF and a 0.1 μF cap from supply pins to GND decoupling capacitor has to be connected between V<sub>DD</sub> (pins 12 and 16) and GND (pins 7 and 13). It is recommended to place decoupling capacitors

as close as possible to the device to minimize lead inductance.

**Termination**

The output buffer structure is shown in the Figure 8.

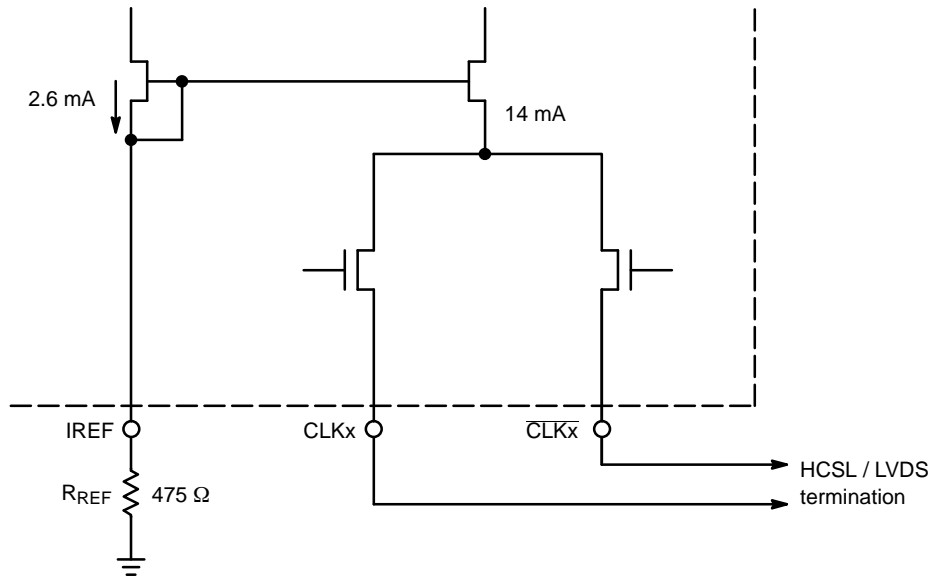


Figure 8. Simplified Output Structure

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The outputs can be terminated to drive HCSL receiver (see Figure 9) or LVDS receiver (see Figure 10). HCSL output interface requires  $49.9\ \Omega$  termination resistors to GND for generating the output levels. LVDS output

interface may not require the  $100\ \Omega$  near the LVDS receiver if the receiver has internal  $100\ \Omega$  termination. An optional series resistor  $R_L$  may be connected to reduce the overshoots in case of impedance mismatch.

### HCSL INTERFACE

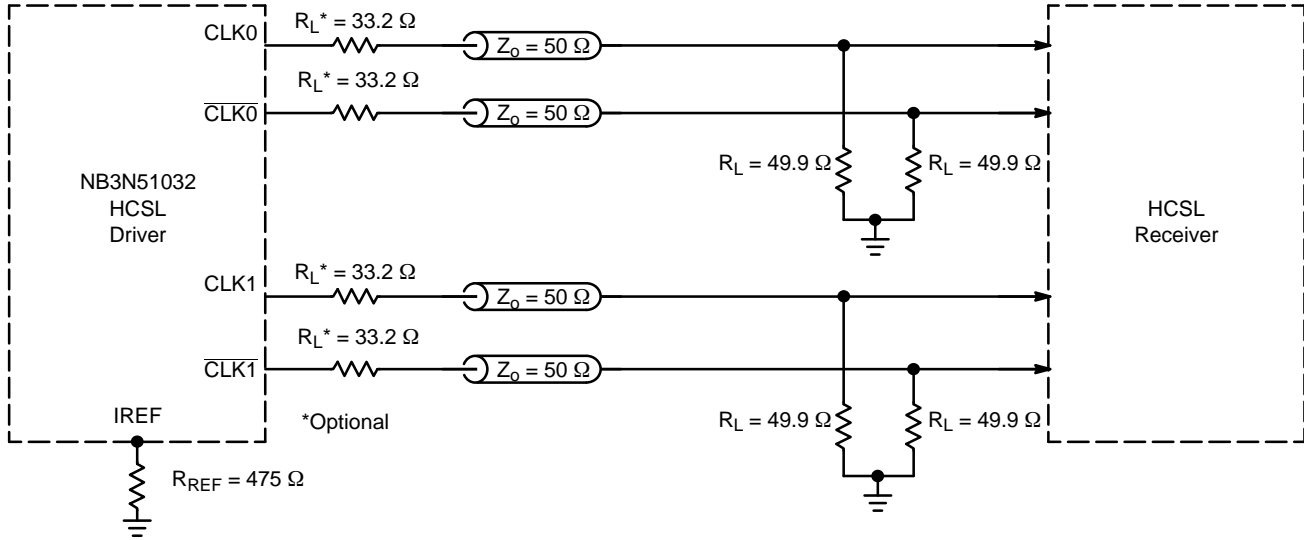


Figure 9. Typical Termination for Output Driver and Device Evaluation

### LVDS COMPATIBLE INTERFACE

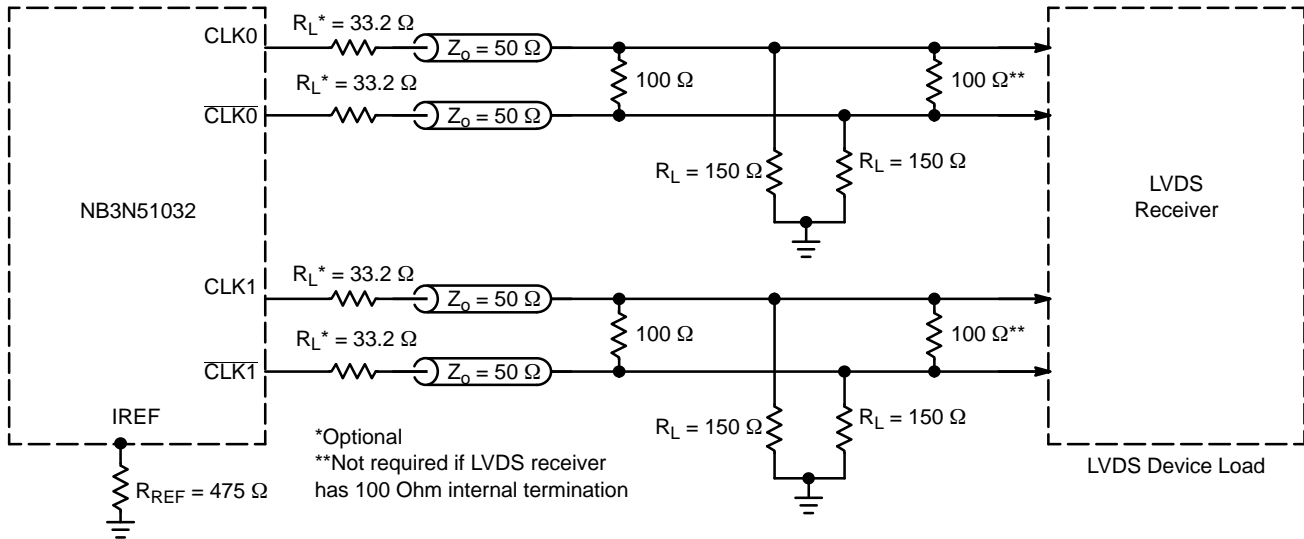


Figure 10. Typical Termination for LVDS Device Load

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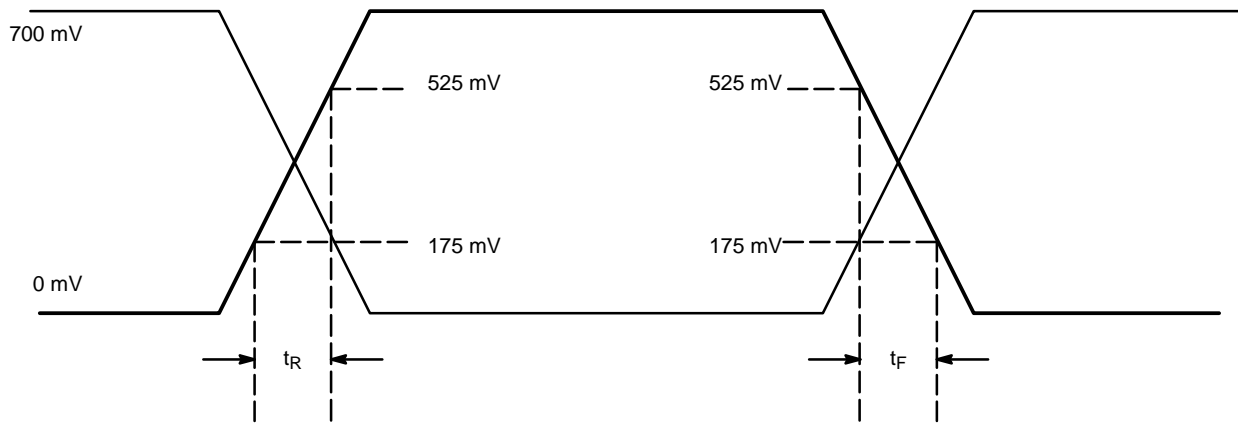


Figure 11. HCSL Output Parameter Characteristics

## ORDERING INFORMATION

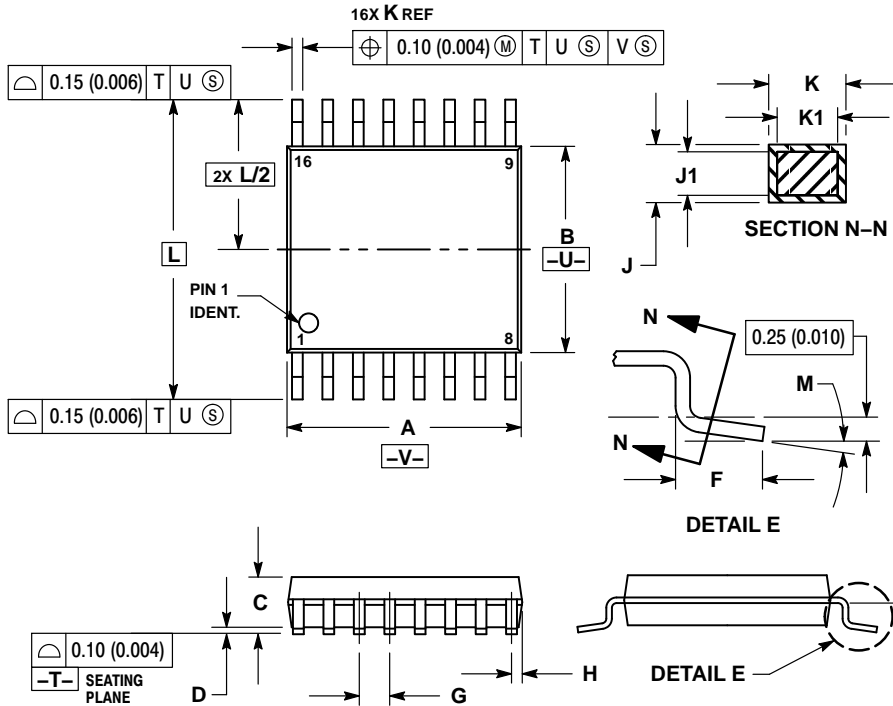
| Device         | Package               | Shipping†          |
|----------------|-----------------------|--------------------|
| NB3N51032DTG   | TSSOP-16<br>(Pb-Free) | 96 Units / Rail    |
| NB3N51032DTR2G | TSSOP-16<br>(Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NB3N51032

## PACKAGE DIMENSIONS

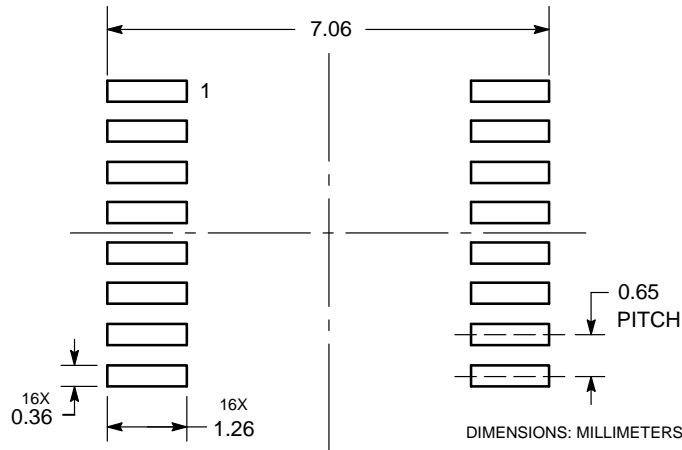
TSSOP-16  
CASE 948F  
ISSUE B




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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