Freescale Semiconductor
Product Brief

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MCF5253 ColdFire® Microprocessor Product Brief

This document provides an overview of the MCF5253 ColdFire processor and general descriptions of the MCF5253 features and modules.

The MCF5253 is an excellent general purpose system controller with over 125 Dhrystone 2.1 MIPS @ 140 MHz performance at a very competitive price. The integrated peripherals and eMAC allow the MCF5253 to replace both the microcontroller and the DSP in certain applications. Most peripheral pins can also be remapped as general purpose I/O pins.

Low-power features include flexible PLL (with power down mode) with dynamic clock switching, a hardwired CD ROM decoder, advanced 0.13 µm CMOS process technology, 1.2 V core power supply, and an on-chip 128-Kbyte SRAM.

Additional features of the MCF5253 microprocessor include USB 2.0 On-The-Go (OTG) technology with integrated high-speed physical layer (PHY), real-time clock (RTC), dedicated advanced technology attachment

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(ATA) hard disk interface supporting ATA-66, and two controller area network (CAN) modules for automotive control bus support in a single solution.

1 Application Examples

The MCF5253 processor is designed for various consumer applications. It is an excellent general purpose system controller with over 125 Dhrystone 2.1 MIPS @ 140 MHz performance. The integrated peripherals and eMAC allow the MCF5253 to replace both the microcontroller and the DSP in certain applications. Most peripheral pins can be remapped as general purpose I/O pins.

The MCF5253 is designed for the following consumer applications:

- Point of sale
- VoIP
- Medical instrumentation
- Industrial control markets (e.g., factory automation)
- Fire/security

For additional information regarding software drivers and for additional applications, refer to http://www.freescale.com/coldfire.

2 Features

The MCF5253 is a second generation 32-bit microprocessor which includes greater features, more memory, and improved power management over the MCF5249.

Distinguishing features of the MCF5253 are:

- USB 2.0 high-speed on-the-go (OTG) with integrated PHY
- Dedicated ATA hard disk interface
- Dedicated USB and ATA 16K SRAM with DMA support
- Digital audio interface (I^2S and SPDIF)
- SmartMedia interface (including IDE and compact flash)
- Three UARTs
- NOR flash interface
- Twin controller area network module (FlexCAN)
- Embedded BDM debug port
- On-chip real-time clock that works with a 32.768 kHz crystal. Real-time clock has tamper detection functionality.
- 225-pin MAPBGA package
- SD/MMC interface
- Keypad/battery level monitor ADC
- Two I^2C interfaces (400 KHz)

2.1 Block Diagram

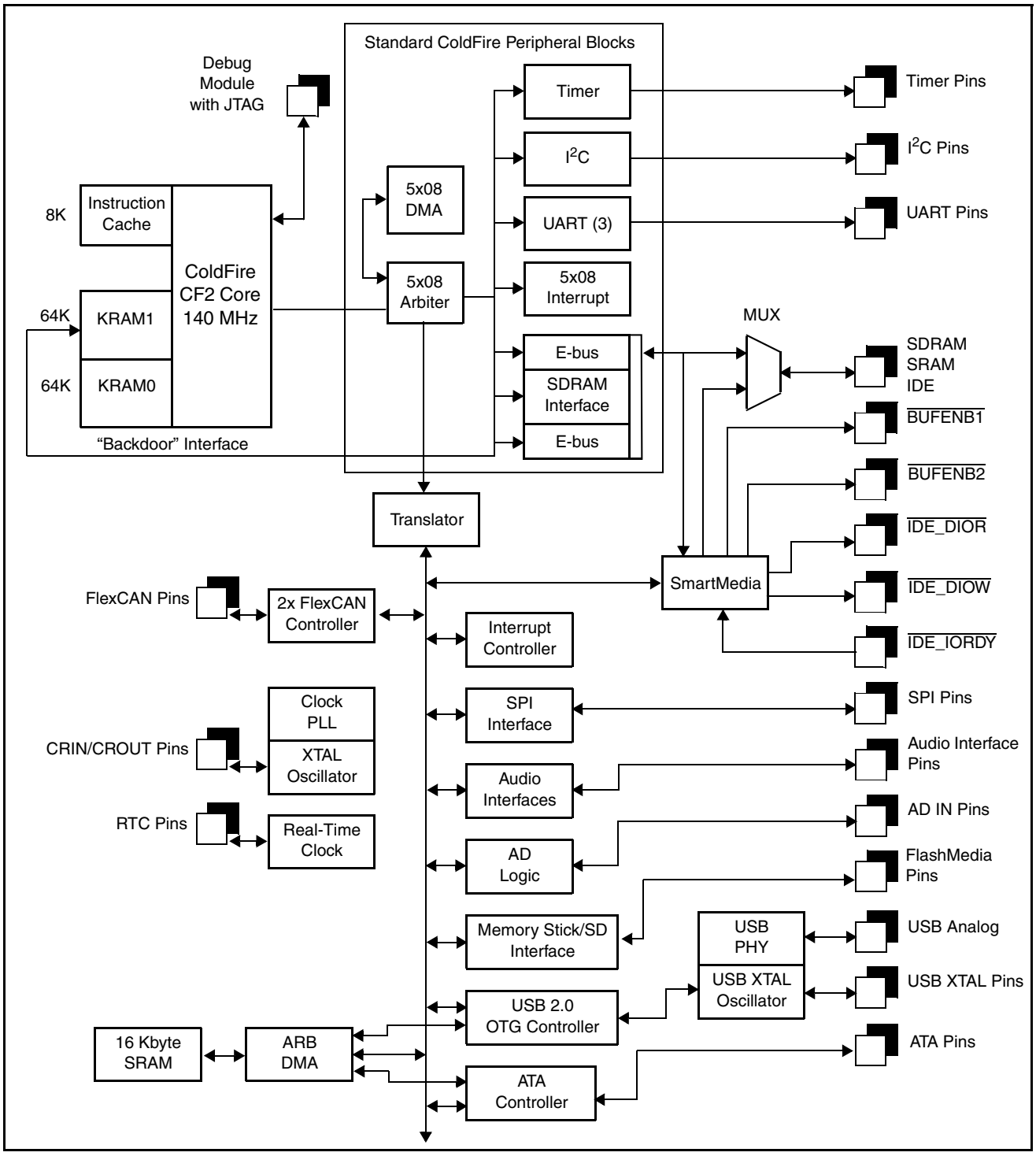

Figure 1. MCF5253 Block Diagram

2.2 Critical Performance Parameters

The following list provides the performance parameters of the MCF5253 processor.

- An internal 1.2 V regulator to supply the CPU and PLL
- Maximum 140 MHz operating core frequency
- Operating temperature range of -40° – +85° C
- Packaged in a 225 MAPBGA, 14 × 14 mm 0.8 mm pitch

2.3 Chip-Level Features

This section summarizes the features of the MCF5253 processor.

2.3.1 ColdFire CF2 Core

The ColdFire processor Version 2 (V2) core consists of two independent, decoupled, pipeline structures to maximize performance while minimizing core size.The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands, and then executes the required function. Because the IFP and OEP pipelines are decoupled by an instruction buffer that serves as a FIFO queue, the IFP can prefetch instructions in advance of their actual use by the OEP, which minimizes time stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC data path with a dual-read-ported register feeding an arithmetic/logic unit (ALU).

More features of the ColdFire V2 processor core include:

- Clock-doubled Version 2 microprocessor core
- 32-bit internal data bus, 16 bit external data bus
- 16 user-visible, 32-bit general-purpose registers
- Supervisor/user modes for system protection
- Vector base register to relocate exception-vector table
- Optimized for high-level language constructs

2.3.2 Module Features

Table 1 shows an alphabetical listing of the modules in the processor.

Table 1. Digital and Analog Modules

Block Mnemonic	Block Name	Functional Grouping	Brief Description
ATA	Advanced Technology Attachment Controller	Connectivity Peripheral	The ATA block is an AT attachment host interface. Its main use is to interface with IDE hard disc drives and ATAPI optical disc drives.
ADC	Battery Level/Keypad Analog/Digital Converter	Analog Input	The six-channel ADC is based on the Sigma-Delta concept with 12-bit resolution. Both the analog comparator and digital sections are integrated in the MCF5253.

Table 1. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description
AB	Audio Bus	Audio Interface	The audio interfaces connect to an internal bus that carries all audio data. Each receiver places its received data on the audio bus and each transmitter takes data from the audio bus for transmission.
AIM	Audio Interface	Audio Interface	The audio interface module provides the necessary input and output features to receive and transmit digital audio signals over serial audio interfaces (IIS/EIAJ) and over digital audio interfaces (IEC958).
BROM	Bootloader	Boot ROM	The MCF5253 incorporates a ROM Bootloader, which enables booting from UART, I2C, SPI, or IDE devices.
FlexCAN	Twin Controller Area Network 2.0B Communication Unit	Connectivity Peripheral	The FlexCan module is a full implementation of the Bosch CAN protocol specification 2.0B, which supports both standard and extended message frames.
CSM	Chip Select Module	Connectivity Peripheral	Three programmable chip-select outputs ($\overline{CS0}$/$\overline{CS4}$, $\overline{CS1}$, and $\overline{CS2}$) provide signals that enable glueless connection to external memory and peripheral circuits.
DMAC	Direct Memory Access Controller Module	Connectivity Peripheral	There are four fully programmable DMA channels for quick data transfer.
eMAC	Enhanced Multiply Accumulate Module	Core	The integrated eMAC unit provides a common set of DSP operations and enhances the integer multiply instructions in the ColdFire architecture.
MBUS	Memory Bus Interface	Bus Operation	The bus interface controller transfers data between the ColdFire core or DMA and memory, peripherals, or other devices on the external bus.
MMC/SD	Multimedia Card/Secure Digital Interface	Flash Memory Card Interface	The interface is Sony® Memory Stick®, SecureDigital, and Multi-Media card compatible. **Note:** The Sony Memory Interface does not support Sony MagicGate™.
GPIO	General Purpose I/O Interface	System integration	GPIO signals are multiplexed with various other signals.
GPT	General Timer Module	Timer peripheral	The timer module includes two general-purpose timers, each of which contains a free-running 16-bit timer.
IDE	Integrated Drive Electronics	Connectivity peripheral	The IDE hardware consists of bus buffers for address and data and are intended to reduce the load on the bus and prevent SDRAM and Flash accesses from propagating to the IDE bus.
INC	Instruction Cache	Core	The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock cycle.
I^2C	Inter IC Communication Module	Connectivity peripheral	The two-wire I^2C bus interfaces, compliant with the Philips I^2C bus standard, are bidirectional serial buses that exchange data between devices.
SRAM	Internal 128-KB SRAM	Internal memory	The 128-Kbyte on-chip SRAM is split over two banks, SRAM0 (64K) and SRAM1 (64K). It provides single clock-cycle access for the ColdFire core.
LIN	Internal Voltage Regulator	Linear regulator	An internal 1.2 V regulator is used to supply the CPU and PLL sections of the MCF5253, reducing the number of external components required and allowing operation from a single supply rail, typically 3.3 volts.

Table 1. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description
JTAG	Joint Test Action Group	Test and debug	To help with system diagnostics and manufacturing testing, the MCF5253 includes dedicated user-accessible test logic that complies with the IEEE 1149.1A standard for boundary scan testability, often referred to as Joint Test Action Group, or JTAG.
QSPI	Queued Serial Peripheral Interface	Connectivity Interface	The QSPI module provides a serial peripheral interface with queued transfer capability.
RTC	Real-Time Clock	Timer Peripheral	The RTC is a clock that keeps track of the current time even if the clock is turned off.
BDM	Background Debug Interface	Test and debug	A background-debug mode (BDM) interface provides system debug.
SDRAMC	Synchronous DRAM Memory Controller	Peripheral Interface	The SDRAM controller provides a glueless interface for one bank of SDRAM, and can address up to 32MB. The controller supports a 16-bit data bus. The controller operates in page mode, non-page mode, and burst-page mode and supports SDRAMs.
SIM	System Integration Module	System Integration	The SIM provides overall control of the internal and external buses and serves as the interface between the ColdFire core and the internal peripherals or external devices. The SIM is responsible for the two interrupt controllers (setting priorities and levels). And it also configures the GPIO ports.
PLL	System Oscillator and Phase Lock Loop	System Clocking	The oscillator operates from an external crystal connected across CRIN and CROUT. The circuit can also operate from an external clock connected to CRIN. The on-chip programmable PLL, which generates the processor clock, allows the use of almost any low frequency external clock (5–35 MHz).
UART	Universal Asynchronous Receiver /Transmitter Module	Connectivity Peripheral	Three UARTs handle asynchronous serial communication.
USBOTG	USB 2.0 High-Speed On-The-Go	Connectivity Peripheral	The USB module is used for communication to a PC or communication to slave devices; for example, to download data from a hard disc player to a flash player, and to other devices.

3 Developer Environment

The MCF5253 processor supports similar tools and third party developers as other Freescale ColdFire products, offering a widespread, established network of tools and software vendors.

The following development support are available:

- Evaluation boards (EVBs)
- Compilers and debuggers
- JTAG interfaces
- Initialization tool

The following software support are available:

- Code examples
- Various module drivers (e.g., USB stack, SPI, I^2C)
- Third party real-time operating systems (RTOS)

4 Document Revision History

Revision 1 is the first release of this document.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

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