



ATP405

N-Channel Power MOSFET 100V, 40A, 33mΩ, ATPAK

ON Semiconductor®

<http://onsemi.com>

Features

- ON-resistance $R_{DS(on)}=25m\Omega$ (typ.)
- 10V drive
- Input capacitance $C_{iss}=4000pF$ (typ.)
- Halogen free compliance

Specifications

Absolute Maximum Ratings at $T_a=25^\circ C$

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		100	V
Gate-to-Source Voltage	V_{GSS}		± 20	V
Drain Current (DC)	I_D		40	A
Drain Current (Pulse)	I_{DP}	$PW \leq 10\mu s$, duty cycle $\leq 1\%$	160	A
Allowable Power Dissipation	P_D	$T_c=25^\circ C$	70	W
Channel Temperature	T_{ch}		150	$^\circ C$
Storage Temperature	T_{stg}		-55 to +150	$^\circ C$
Avalanche Energy (Single Pulse) *1	E_{AS}		148	mJ
Avalanche Current *2	I_{AV}		40	A

Note : *1 $V_{DD}=30V$, $L=100\mu H$, $I_{AV}=40A$

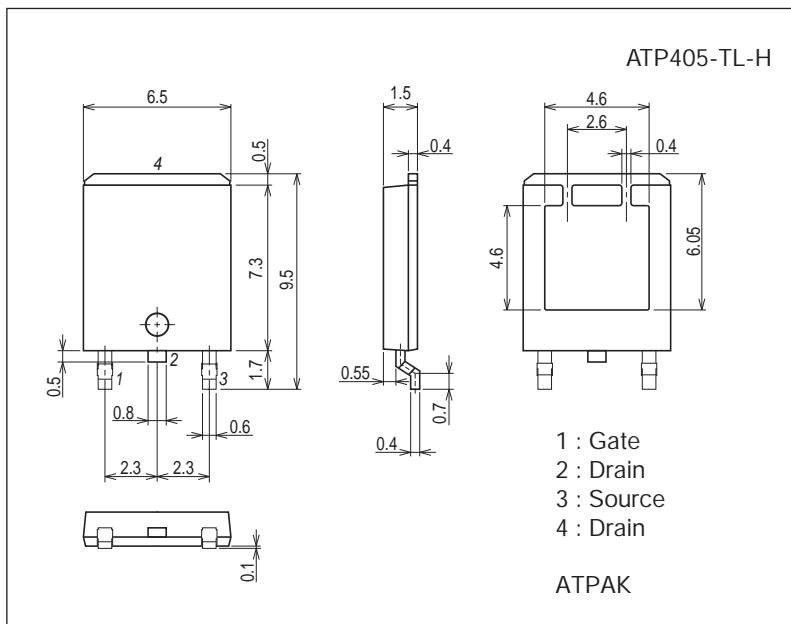
*2 $L \leq 100\mu H$, Single pulse

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

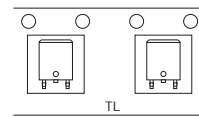
7057-001



Product & Package Information

- Package : ATPAK
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

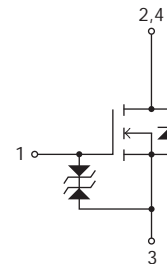
Packing Type: TL



Marking



Electrical Connection

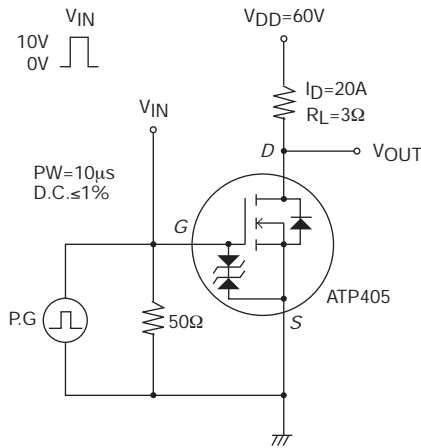


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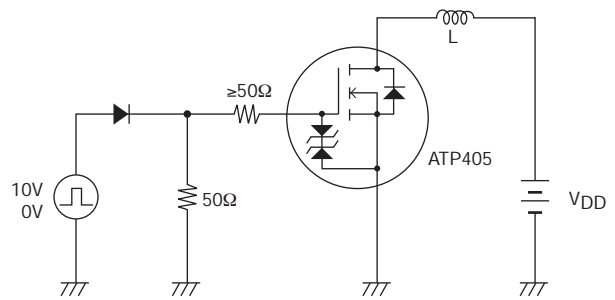
Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit	
			min	typ	max		
Drain-to-Source Breakdown Voltage	V(BR)DSS	I _D =1mA, V _{GS} =0V	100			V	
Zero-Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			10	μA	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} =±16V, V _{DS} =0V			±10	μA	
Cutoff Voltage	V _{GS(off)}	V _{DS} =10V, I _D =1mA	2.0		3.5	V	
Forward Transfer Admittance	y _{fs}	V _{DS} =10V, I _D =20A		62		S	
Static Drain-to-Source On-State Resistance	R _{DS(on)}	I _D =20A, V _{GS} =10V		25	33	mΩ	
Input Capacitance	C _{iss}	V _{DS} =20V, f=1MHz		4000		pF	
Output Capacitance	C _{oss}				300		pF
Reverse Transfer Capacitance	C _{rss}				170		pF
Turn-ON Delay Time	t _{d(on)}	See specified Test Circuit.		38		ns	
Rise Time	t _r			125		ns	
Turn-OFF Delay Time	t _{d(off)}			220		ns	
Fall Time	t _f			150		ns	
Total Gate Charge	Q _g	V _{DS} =60V, V _{GS} =10V, I _D =40A		68		nC	
Gate-to-Source Charge	Q _{gs}			14		nC	
Gate-to-Drain "Miller" Charge	Q _{gd}			15		nC	
Diode Forward Voltage	V _{SD}	I _S =40A, V _{GS} =0V		0.9	1.2	V	

Switching Time Test Circuit

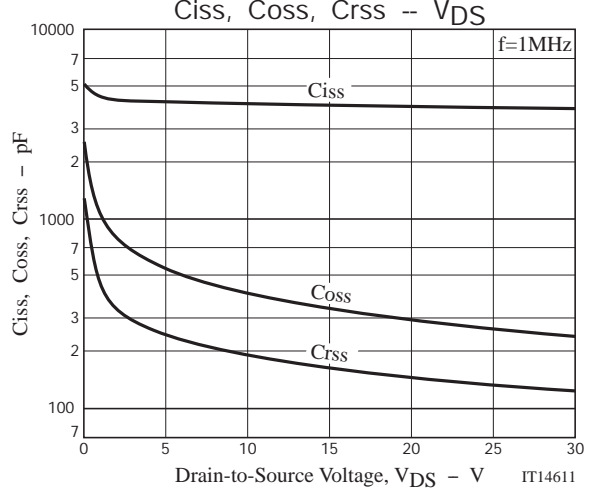
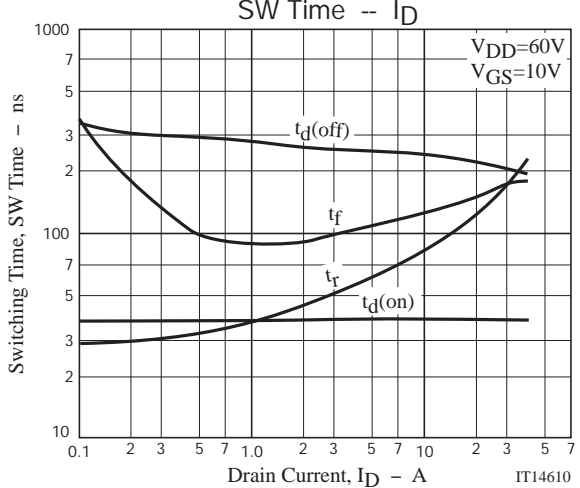
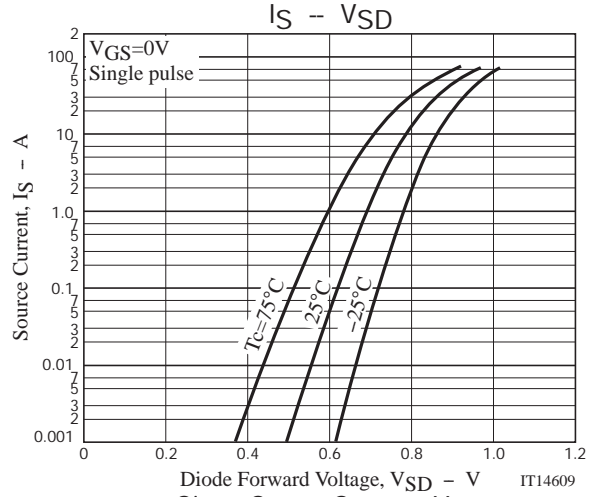
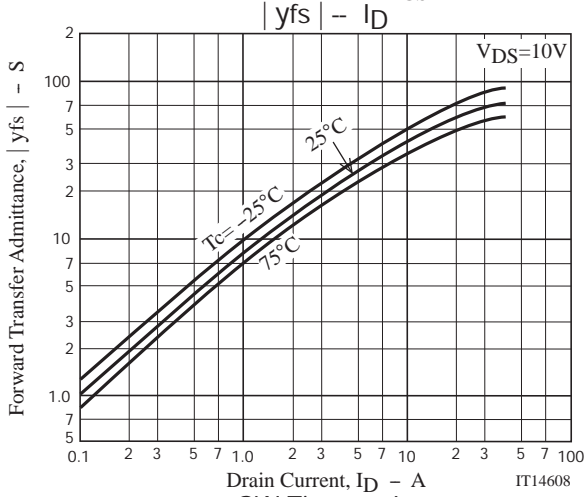
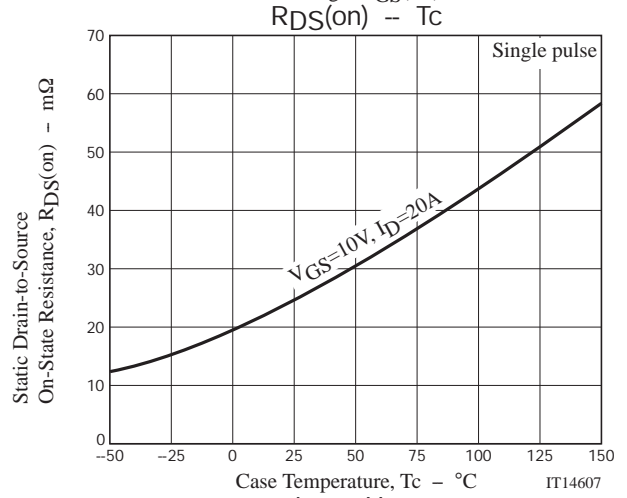
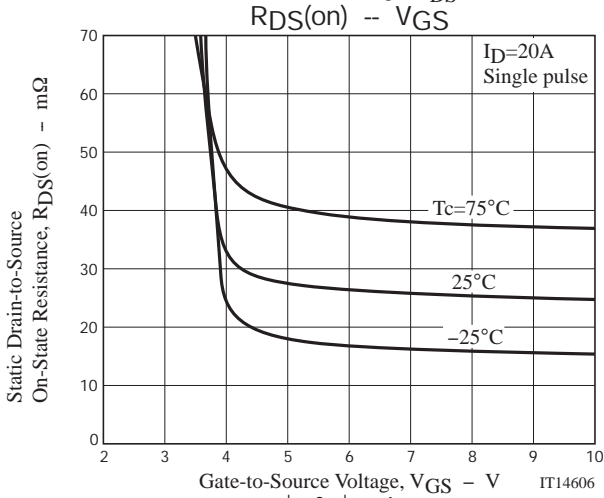
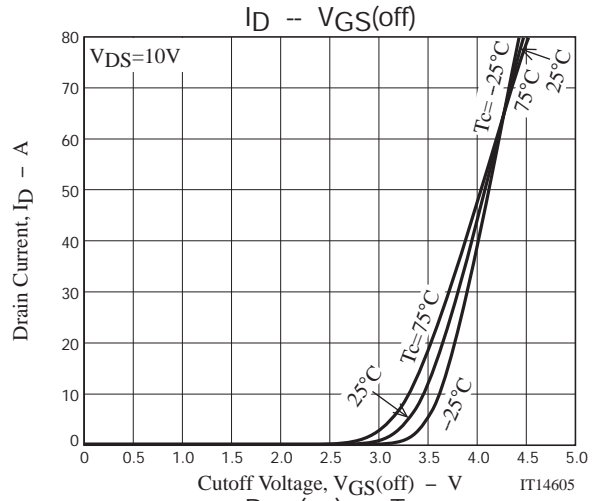
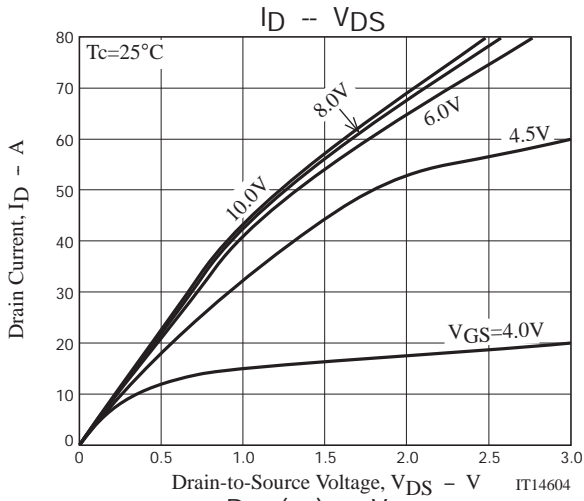


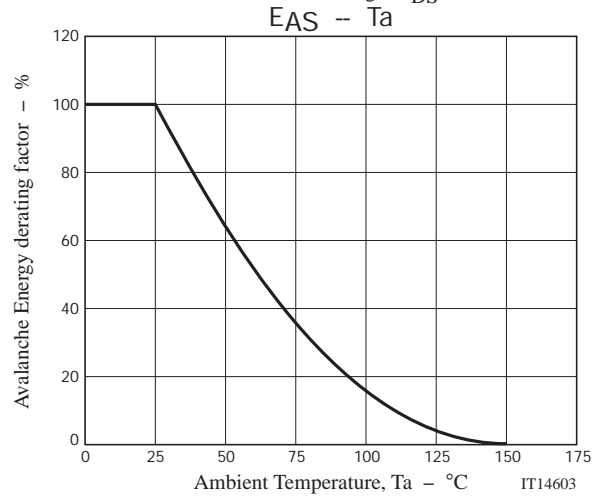
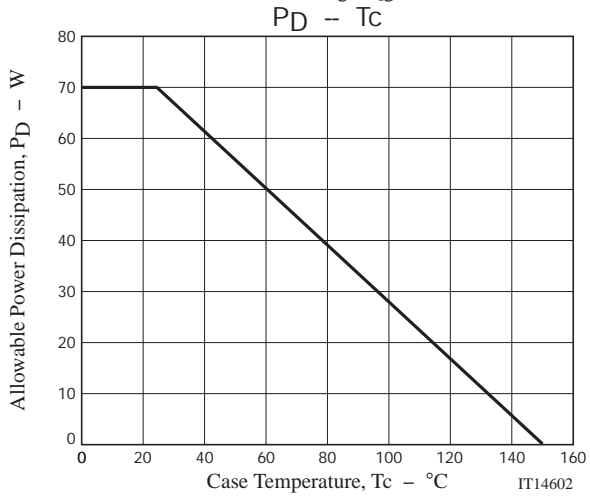
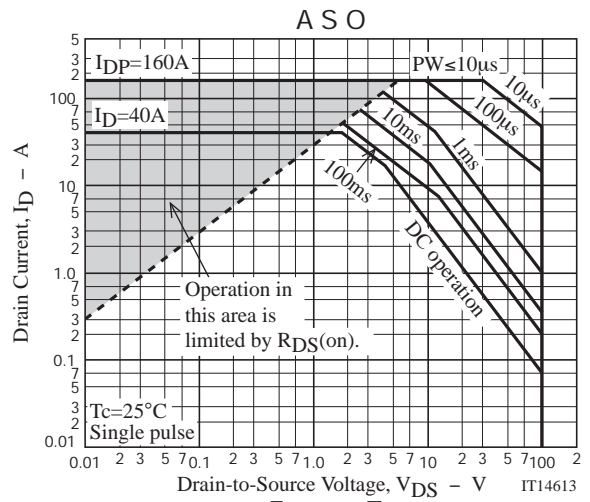
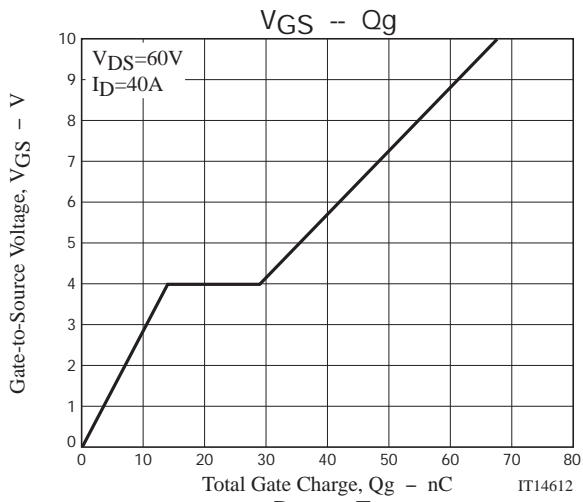
Avalanche Resistance Test Circuit



Ordering Information

Device	Package	Shipping	memo
ATP405-TL-H	ATPAK	3,000pcs./reel	Pb Free and Halogen Free





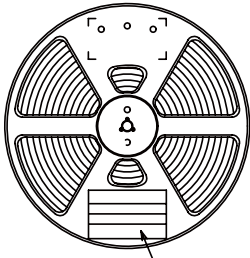
Taping Specification

ATP405-TL-H

1. Packing Format (TL)

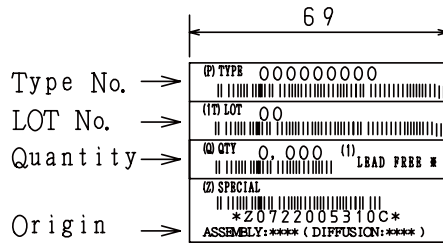
Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	INNER BOX SD-C-18	OUTER BOX SD-A-18
ATPAK	ATP	3,000	3,000	15,000	1 reels contained Dimensions:mm (external) 340×340×28	5 inner boxes contained Dimensions:mm (external) 355×355×165

Packing method



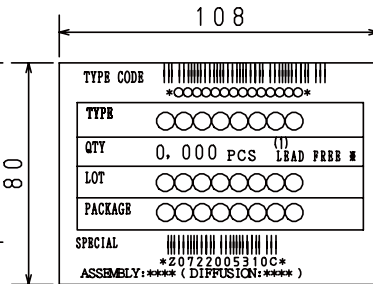
Reel label

Reel label, Inner box label
(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



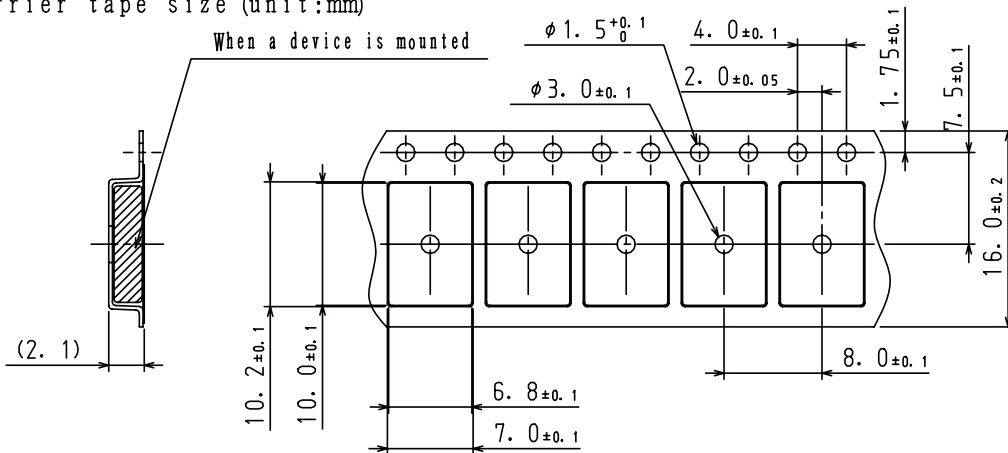
NOTE (1)

The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

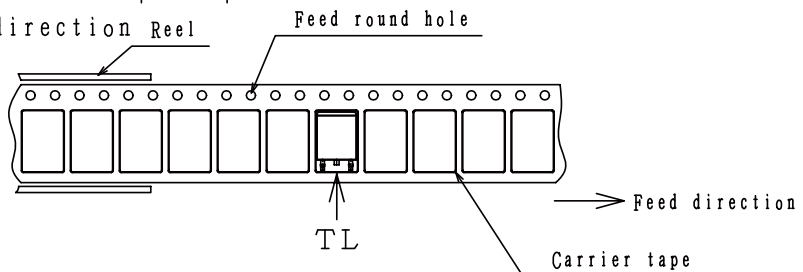
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction Reel



The one electrode terminals on feed hole side...TL

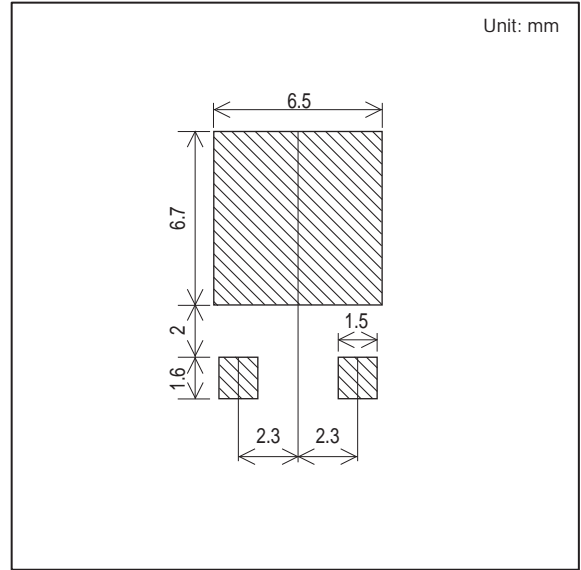
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Outline Drawing

ATP405-TL-H



Land Pattern Example



Note on usage : Since the ATP405 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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