FAIRCHILD SEMICONDUCTOR®

September 2004

RMPA2059

3V WCDMA PowerEdge™ Power Amplifier Module

General Description

The RMPA2059 power amplifier module (PAM) is designed for WCDMA applications. The 2 stage PAM is internally matched to 50Ω to minimize the use of external components and features a low-power mode to reduce standby current and DC power consumption during peak phone usage. High power-added efficiency and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) process.

Features

- Single positive-supply operation and low power and shutdown modes
- 40% CDMA efficiency at +27dBm average output power
- Compact LCC package- 4.0 x 4.0 x 1.5 mm with industry standard pinout
- Internally matched to 50Ω and DC blocked RF input/ output
- Meets WCDMA performance requirements

Device

Absolute Ratings[1]

Symbol	Parameter	Min	Max	Units
Vcc1, Vcc2	Supply Voltages	0	5.0	V
Vref	Reference Voltage	2.7	5.0	V
Vmode	Power Control Voltage	0	3.0	V
Pin	RF Input Power	-	+5	dBm
T_{STG}	Storage Temperature	-55	+150	°C

Note:
1: No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values.

Module Block Diagram

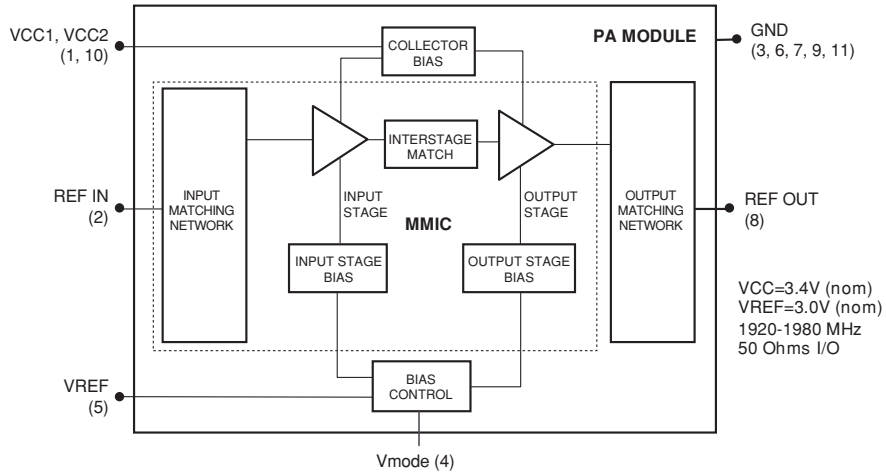


Figure 1. RMPA2059 WCDMA Power Amplifier Module Functional Block Diagram

Electrical Characteristics[1]

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating Frequency			1920		1980	MHz
CDMA MODE						
Gain	G Gp	P_O = 0dBm P_O = +27dBm		26 27		dB dB
Maximum Linear Power Out	P_O		27			dBm
Power-Added Efficiency	PAEd	P_O = +27dBm		40		%
Adjacent Channel Leakage Ratio ±5.0 MHz Offset ±10.0 MHz Offset	 ACLR1 ACLR2	P_O = +27dBm 3GPP 3.2 03-00 DPCCH +1DPDCH		 -38 -48		 dBc dBc
General Characteristics						
Input VSWR	VSWR			2.0:1		
Noise Figure	NF			3		dB
Rx Band Noise Power	No			-139		dBm/Hz
Harmonic Suppression[4]		2fo, 3fo, 4fo			-30	dBc
Spurious Output[4]		5:1 Load VSWR[2]			-60	dBc
Case Operating Temp.	Tc		-30		85	°C
DC Characteristics						
Quiescent Current	Iccq	High Power Mode Low Power Mode		80 40		mA mA
Vref Current	Iref	Vref = 3.0V		5		mA
Power Shutdown Current[3]		Vref = 0V		<1	10	µA

Notes:
1: All parameters met at Tc = +25°C, Vcc = +3.4V, f = 1950 MHz, and load VSWR ≤ 1.2:1.
2: All phase angles.
3: No applied RF signal.
4: Guaranteed by design.

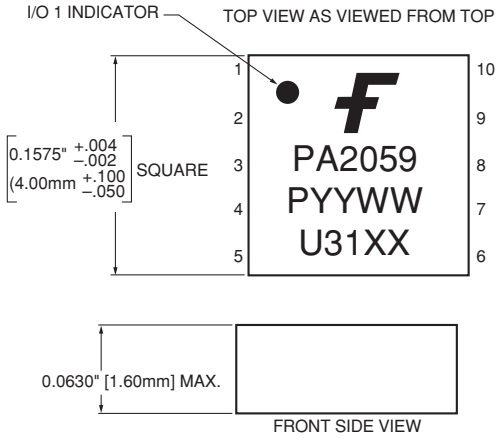
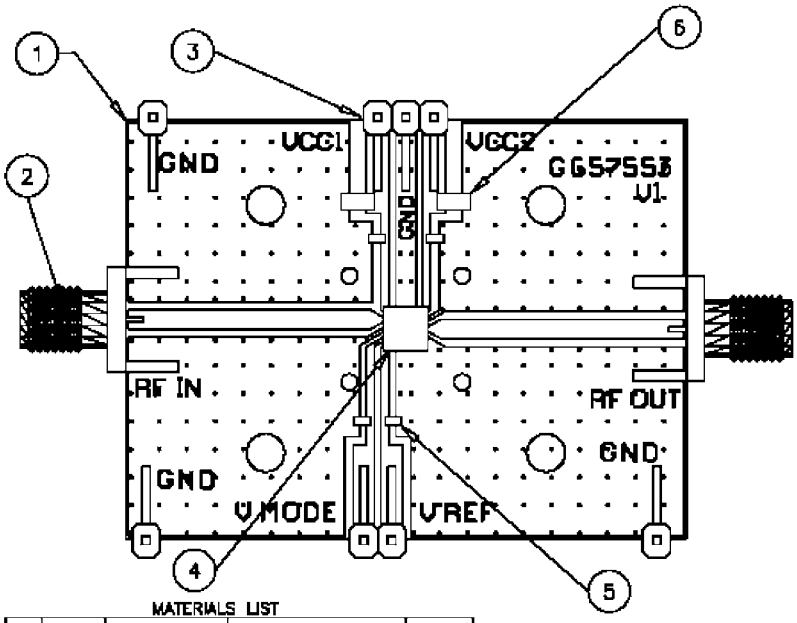


Figure 2. Package Outline

Package Pinout

Parameter	Symbol	Description	Pin#
RF	RF In RF Out	RF Input to PA; DC blocked; 5dBm maximun input RF Output of PA; DC blocked	2 8
DC Power	Vcc1, Vcc2	DC Supplies of PA	1, 10
Ground	Gnd	Signal Ground	3, 6, 7, 9, 11
Control	Vmode Vref	High Power/Low Power Control Reference Voltage	4 5



MATERIALS LIST

QTY	ITEM NO.	PART NUMBER	DESCRIPTION	VENDOR
1	1	[illegible]	PC, BOARD	
2	2	[illegible]	SMA CONNECTOR	JOHNSON
4	3	[illegible]	TERMINALS	3M
REF	4	[illegible]	ASSEMBLY, RMPA2059	
4	5 (C1)	[illegible]	1000 pF CAPACITOR (0603)	MURATA
	5 (ALT)	[illegible]	1000 pF CAPACITOR (0603)	PANASONIC
2	6 (C2)	[illegible]	3.3 nF CAPACITOR (1206)	TDK
A/R	7	SN63	SOLDER PASTE	INDIUM CORP.
A/R	8	SN96	SOLDER PASTE	INDIUM CORP.

Figure 3. Evaluation Board Layout

DC Turn-On Sequence

1) Vcc1 = Vcc2 = 3.4V (typ)
2) Vref = 3.0V (typ)
3) Vmode = 2.0V (Pout < 16dBm), 0V (Pout > 16dBm)

Recommended Operating Conditions[1]

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	Vcc1, Vcc2	3.1	3.4	4.5	V
RF Input Power	Pin		0	+3	dBm
WCDMA Output Power Range	Pout	-55		+27	dBm
Reference Voltage	Vref	2.95	3.0	3.05	V

Note:
1: RF input power for WCDMA Pout = +27dBm.

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC & ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
  - A properly grounded static-dissipative surface on which to place devices.
  - Static-dissipative floor or mat.
  - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, & ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

Device Usage:
Fairchild recommends the following procedures prior to assembly.

- Dry-bake devices at 125°C for 24 hours minimum. Note: The shipping trays cannot withstand 125°C baking temperature.
- Assemble the dry-baked devices within 7 days of removal from the oven.
- During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
- If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure must be repeated.

Solder Materials & Temperature Profile: Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

- **Reflow Profile**
  - Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A typical heating rate is 1- 2°C/sec.
  - Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 120-150 seconds at 150°C.
  - Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 10 seconds. Maximum soldering temperatures should be in the range 215-220°C, with a maximum limit of 225°C.
  - Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

Solder Joint Characteristics:
Proper operation of this device depends on a reliable void-free attachment of the heatsink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

Rework Considerations:
Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should not be subjected to more than 225°C and reflow solder in the molten state for more than 5 seconds. No more than 2 rework operations should be performed.

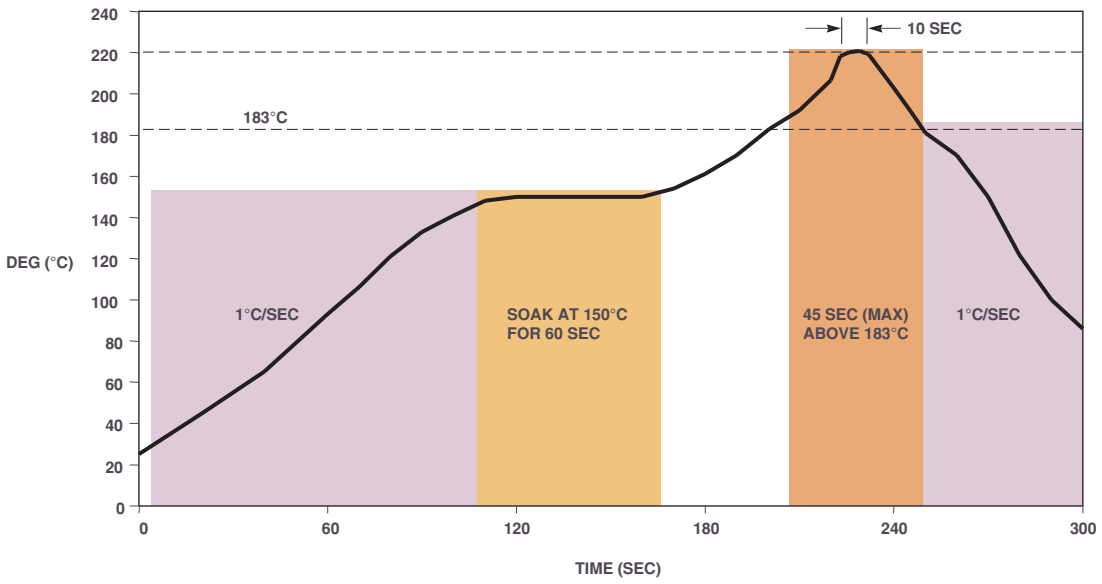


Figure 4. Recommended Solder Reflow Profile

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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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