3.5MHz, 500mA Synchronous Dual Step-Down DC-DC Regulator

Features

- Input Voltage — 2.9V to 5.5V
- Output Voltage — 0.8V to 3.3V
- Output current capability — 500mA per regulator
- Efficiency up to 94%
- Programmable output voltages — 15
- High light-load efficiency via automatic PSAVE mode
- Fast transient response
- Oscillator frequency — 3.5MHz
- 100% duty cycle capability
- Quiescent current — 38µA typical per regulator
- Shutdown current — 0.1µA typical per regulator
- Internal soft-start
- Over-voltage protection
- Current limit and short circuit protection
- Over-temperature protection
- Under-voltage lockout
- Floating control pin protection
- MLPQ-UT18 2.0 x 3.0 x 0.6 (mm) package
- Lead-free, halogen-free, and RoHS/WEEE compliant

Applications

- Smart phones and cellular phones
- MP3/Personal media players
- Personal navigation devices
- Digital cameras
- Single Li-ion cell or 3 NiMH/NiCd cell devices
- Devices with 3.3V or 5V internal power rails

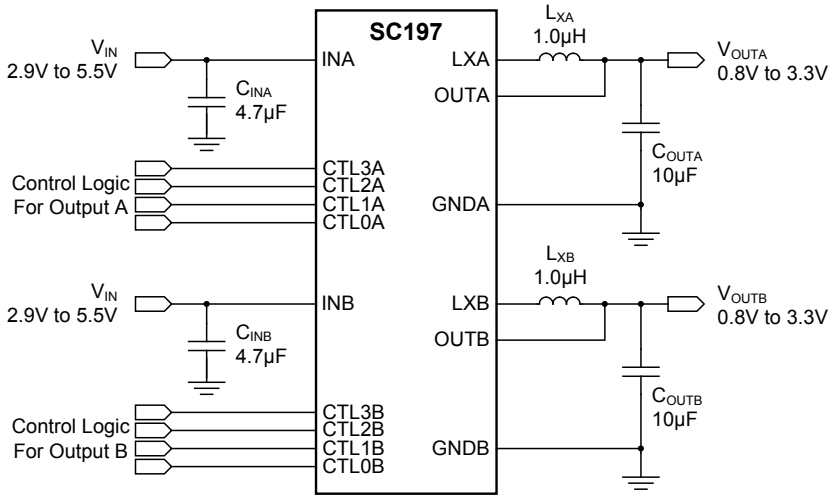
Description

The SC197 contains two identical high efficiency 500mA step-down regulators designed for use in battery-powered applications. Each regulator includes 15 programmable output voltage settings that can be selected using the four control pins, eliminating the need for external feedback resistors. The output voltage can be fixed to a single setting or dynamically switched between different levels. Pulling all four control pins low disables the output.

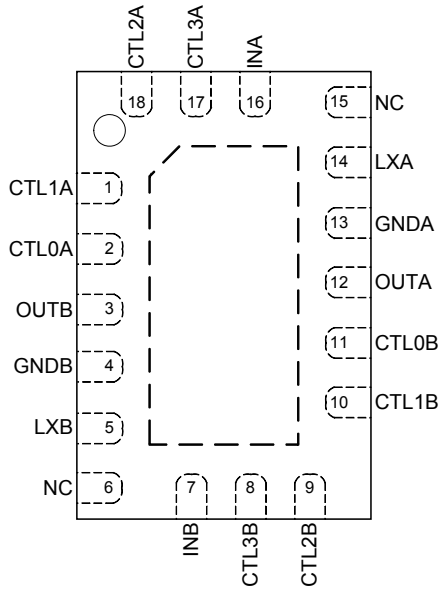
The SC197 operates at a fixed 3.5MHz switching frequency in normal PWM (Pulse-Width Modulation) mode. A variable frequency PSAVE (Power Save) mode is used to optimize efficiency at light loads for each output setting. Built-in hysteresis prevents chattering between the two modes.

The SC197 provides several protection features to safeguard the device under stressed conditions. These include short circuit protection, over-temperature protection, under-voltage lockout, and soft-start to control in-rush current. These features, coupled with the small 2.0 x 3.0 x 0.6 (mm) package make the SC197 a versatile device ideal for step-down regulation in products needing high efficiency and a small PCB footprint.

Typical Application Circuit



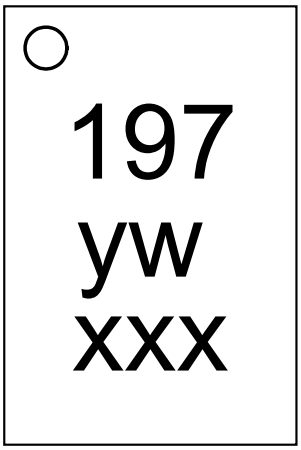
Pin Configuration



MLPQ-UT18; 2 x 3, 18 LEAD

θ_{JA} = 77°C/W

Marking Information



197 = SC197

yw = Date code

xxx = lot number

Ordering Information

Device	Package
SC197ULTRT[1][2]	MLPQ-UT18 2 x 3
SC197EVB	Evaluation Board

Notes:

(1) Available in tape and reel only. A reel contains 3,000 devices.

(2) Lead-free packaging only. Device is WEEE and RoHS compliant and halogen-free.

Table 1 – Output Voltage Settings

CTL3A/B	CTL2A/B	CTL1A/B	CTL0A/B	$V_{OUTA/B}$
0	0	0	0	Shutdown
0	0	0	1	0.80
0	0	1	0	1.00
0	0	1	1	1.20
0	1	0	0	1.40
0	1	0	1	1.50
0	1	1	0	1.60
0	1	1	1	1.80
1	0	0	0	1.85
1	0	0	1	1.90
1	0	1	0	2.00
1	0	1	1	2.20
1	1	0	0	2.50
1	1	0	1	2.80
1	1	1	0	3.00
1	1	1	1	3.30

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Absolute Maximum Ratings

INA, INB (V) ..... -0.3 to +6.0
LXA, LXB Voltage (V) ..... -1.0 to (V_{IN} +0.5)
Other Pins (V) ..... -0.3 to (V_{IN} +0.3)
Output Short Circuit to GND ..... Continuous
ESD Protection Level[1] (kV) 2.5

Recommended Operating Conditions

Ambient Temperature Range (°C) ..... $-40 \le T_A \le +85$
Input Voltage (V) ..... $2.9 \le V_{IN} \le 5.5$

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) 77
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB per JESD51 standards.

Electrical Characteristics

Unless otherwise specified: V_{IN} = 3.6V, C_{IN} = 4.7µF, C_{OUT} =10µF, L_X =1µH, V_{OUT} =1.8V, $T_{J(MAX)}$ =125°C, T_A = -40 to +85 °C. Typical values are T_A =+25 °C.
All specifications are identical for converters A and B.

Parameter	Symbol[1]	Condition	Min	Typ	Max	Units
Output Voltage Range	V_{OUT}		0.8		3.3 [2]	V
Output Voltage Tolerance	V_{OUT_TOL}	I_{OUT} = 200mA	-2.0		2.0	%
		PSAVE mode		1.5		
Line Regulation	$\Delta V_{LINEREG}$	$2.9 \le V_{IN} \le 5.5V$, I_{OUT} = 200mA		0.3		%/V
Load Regulation	$\Delta V_{LOADREG}$	$200mA \le I_{OUT} \le 500mA$		-0.4		%
Output Current Capability	I_{OUT}		500			mA
Current Limit Threshold	I_{LIMIT}		800		1300	mA
Foldback Current Limit	I_{FB_LIM}	$I_{LOAD} > I_{LIMIT}$		150		mA
Under-Voltage Lockout	V_{UVLO}	Rising V_{IN}			2.9	V
		Hysteresis		200		mV
Quiescent Current	I_Q	No switching, I_{OUT} = 0mA		38	60	µA
Shutdown Current	I_{SD}	$V_{CTL\ 0-3}$ = 0V		0.1	1.0	µA
LX Leakage Current	I_{LX}	Into LX pin		0.1	1.0	µA
High Side Switch Resistance[3]	R_{DSON_P}	I_{OUT} = 100mA		250		mΩ
Low Side Switch Resistance[4]	R_{DSON_N}	I_{OUT} = 100mA		350		

Electrical Characteristics (continued)

Parameter	Symbol[1]	Condition	Min	Typ	Max	Units
Switching Frequency	f_{SW}		2.8	3.5	4.2	MHz
Soft-Start	t_{SS}	V_{OUT} = 90% of final value		100	500	µs
Thermal Shutdown	T_{OT}	Rising temperature		160		°C
Thermal Shutdown Hysteresis	T_{HYST}			20		°C
Logic Inputs - CTL0A, CTL1A, CTL2A, CTL3A, CTL0B, CTL1B, CTL2B, and CTL3B						
Input High Voltage	V_{IH}		1.2			V
Input Low Voltage	V_{IL}				0.4	V
Input High Current	I_{IH}	$V_{CTL\ 0\text{-}3}$= V_{IN}	-2.0		5.0	µA
Input Low Current	I_{IL}	$V_{CTL\ 0\text{-}3}$= GND	-2.0		2.0	µA

Notes

(1) All symbol references apply equally to A and B devices.

(2) Maximum output voltage is limited to VIN if the input is less than 3.3V.

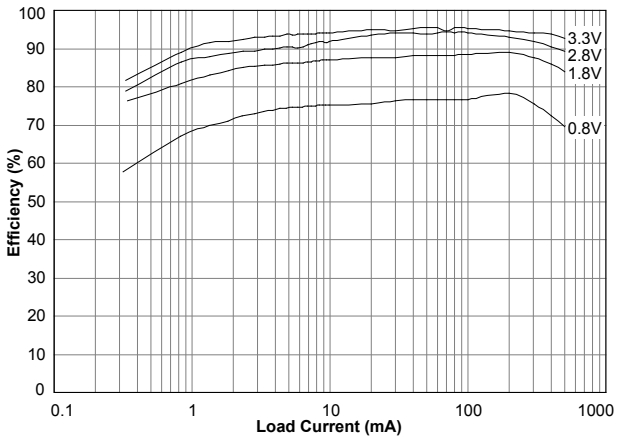
(3) Measured from INA to LXA or from INB to LXB.

(4) Measured from LXA to GNDA or from LXB to GNDB.

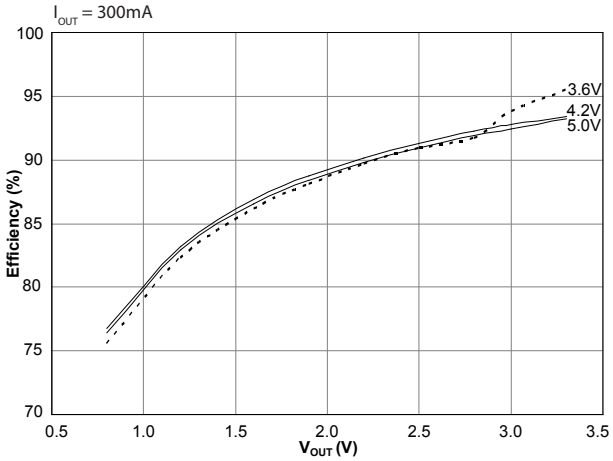
Typical Characteristics

V_{IN} = 4.0V for V_{OUT} = 3.3V, V_{IN} = 3.6V for all others. C_{IN} = 4.7µF, C_{OUT} = 10µF, L_X = 1µH, T_A = 25°C unless otherwise noted.

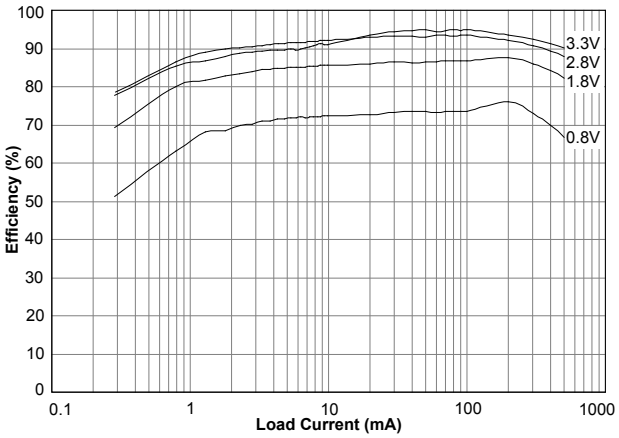
Efficiency vs. I_{OUT} (T_A = -40°C)



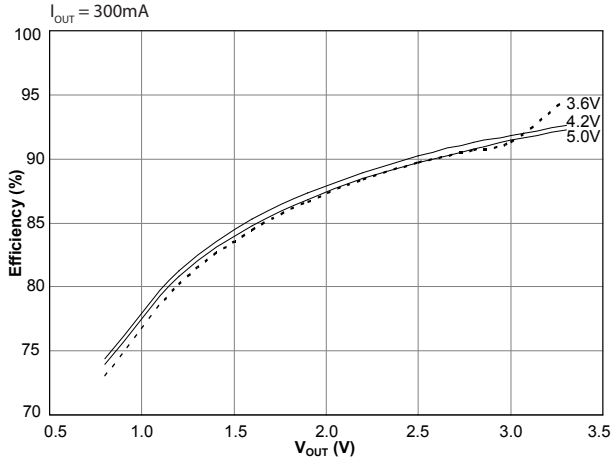
Efficiency vs. V_{OUT} (T_A = -40°C)



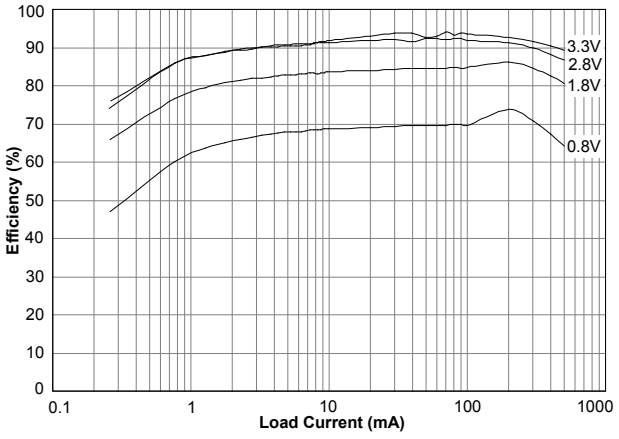
Efficiency vs. I_{OUT} (T_A = 25°C)



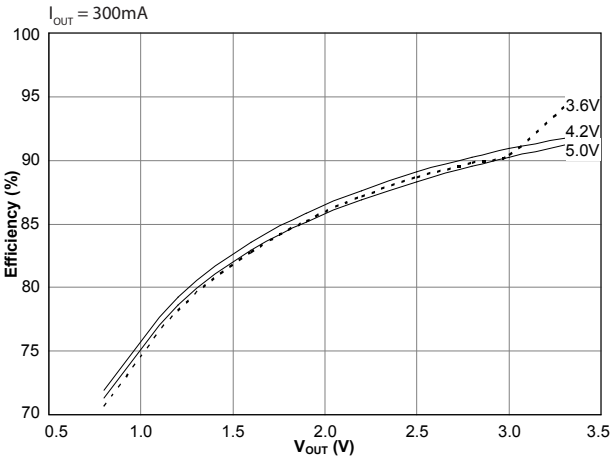
Efficiency vs. V_{OUT} (T_A = 25°C)



Efficiency vs. I_{OUT} (T_A = 85°C)



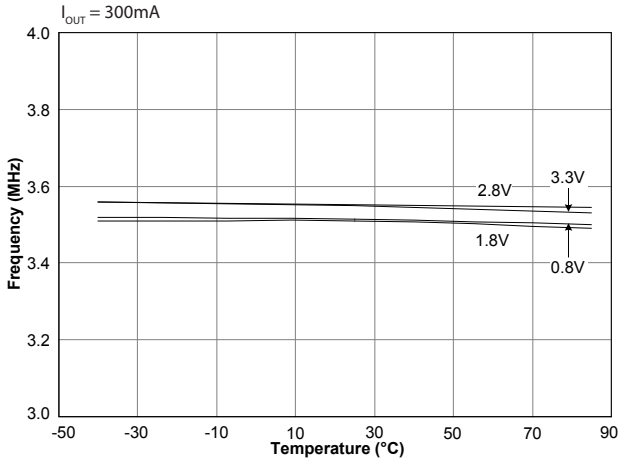
Efficiency vs. V_{OUT} (T_A = 85°C)



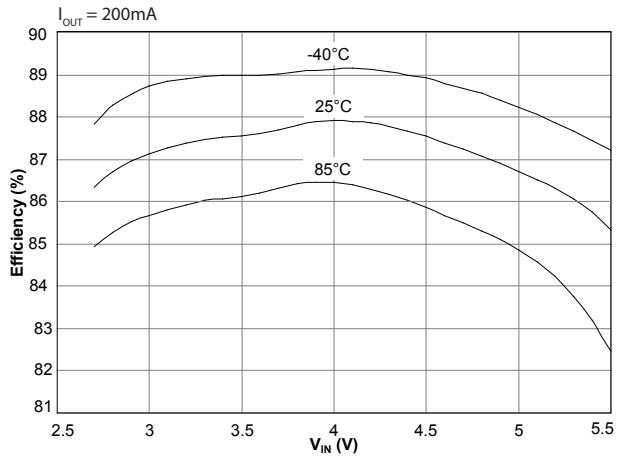
Typical Characteristics (continued)

V_{IN} = 4.0V for V_{OUT} = 3.3V, V_{IN} = 3.6V for all others. C_{IN} = 4.7µF, C_{OUT} = 10µF, L_X = 1µH, T_A = 25°C unless otherwise noted.

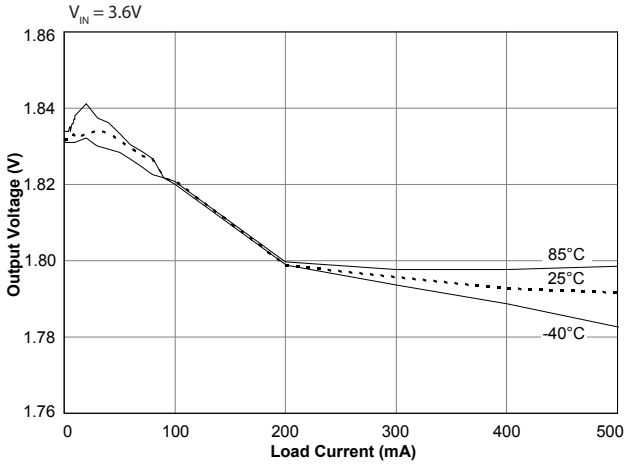
Frequency vs. Temperature



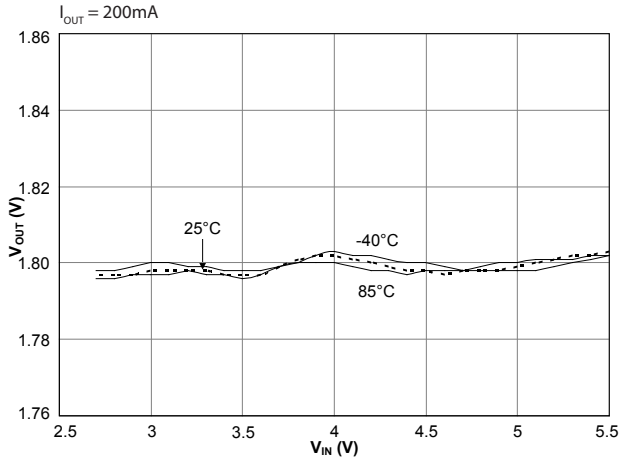
Efficiency vs. V_{IN} (V_{OUT}=1.8V)



Load Regulation (V_{OUT} = 1.8V)

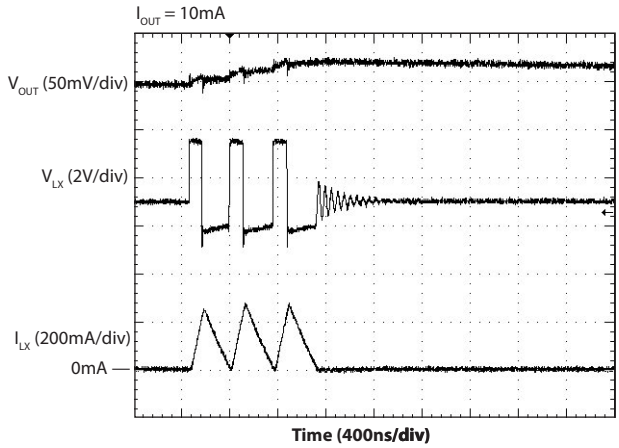


Line Regulation (V_{OUT}=1.8V)

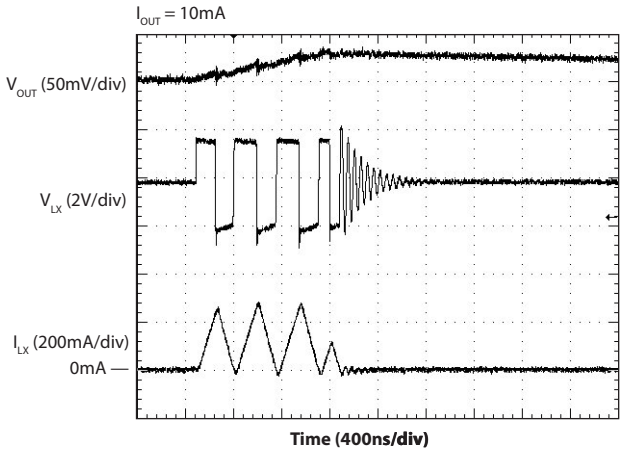


Typical Characteristics (continued)

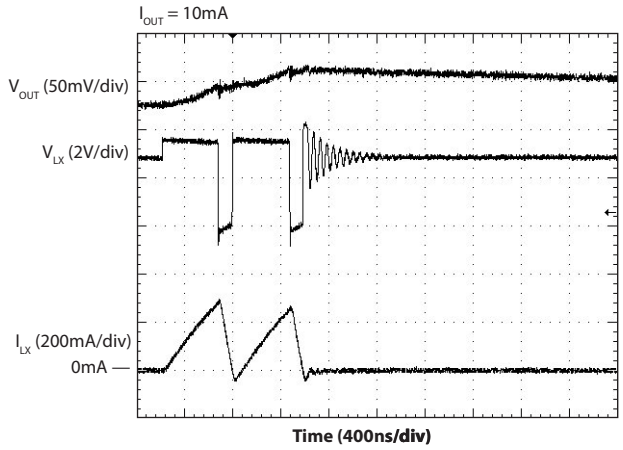
Light Load Switching — V_{OUT} = 1.0V



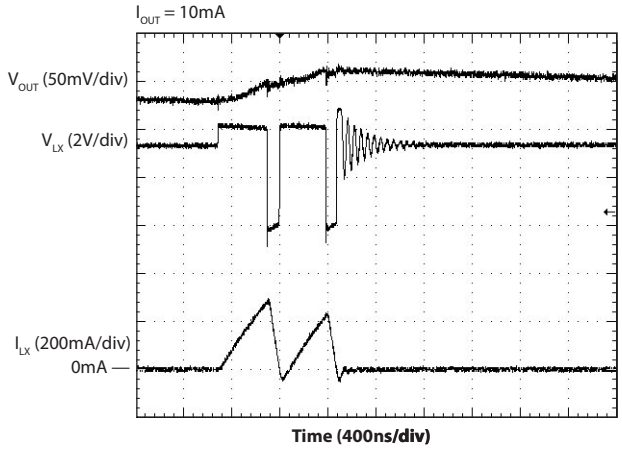
Light Load Switching — V_{OUT} = 1.8V



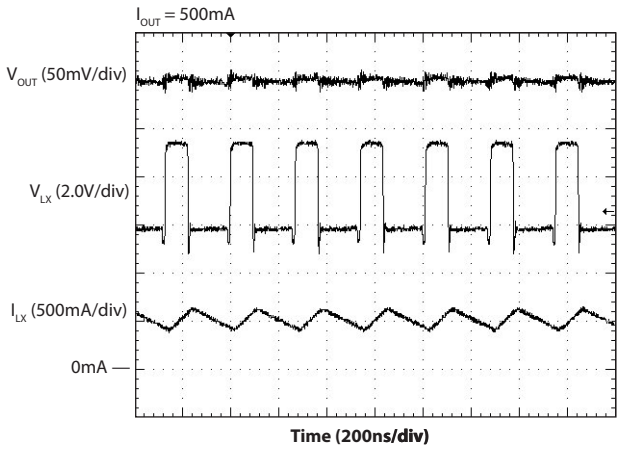
Light Load Switching — V_{OUT} = 2.8V



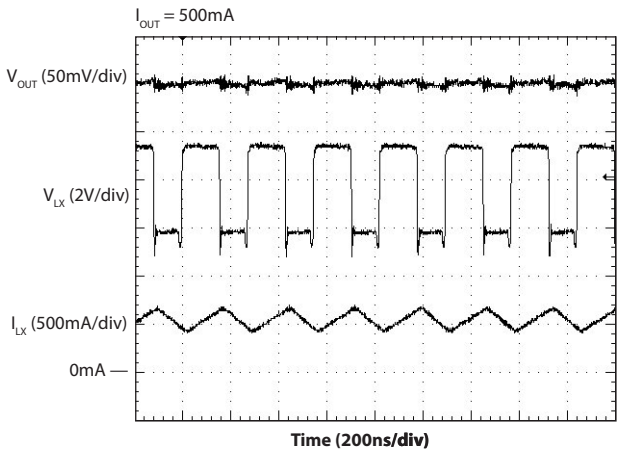
Light Load Switching — V_{OUT} = 3.3V



Heavy Load Switching — V_{OUT} = 1.0V

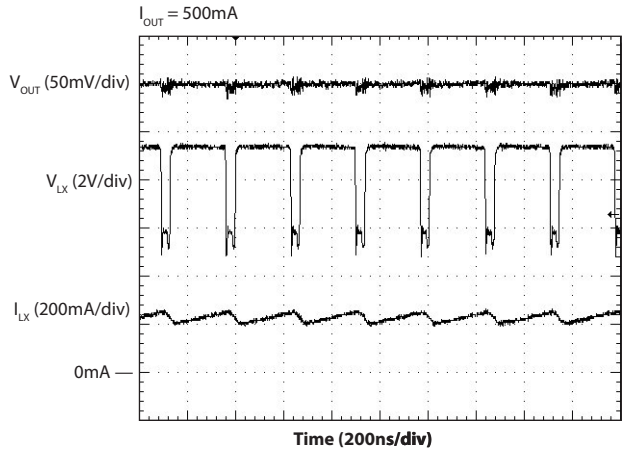


Heavy Load Switching — V_{OUT} = 1.8V

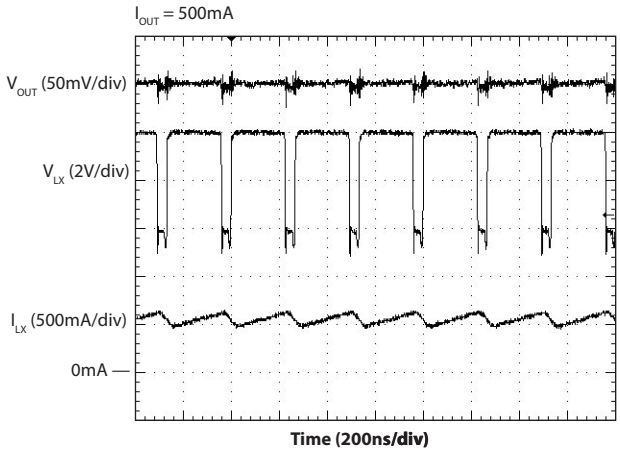


Typical Characteristics (continued)

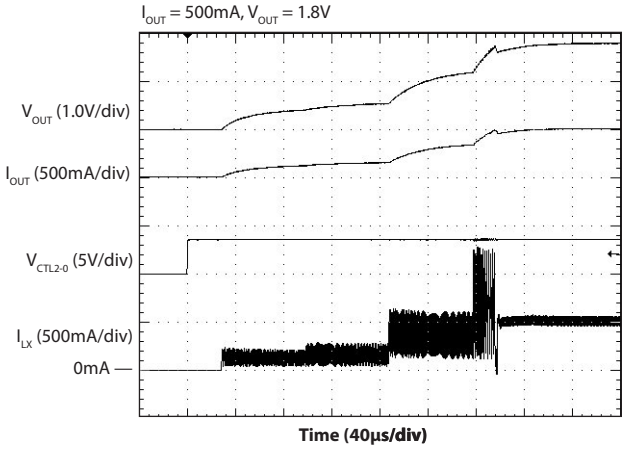
Heavy Load Switching — V_{OUT} = 2.8V



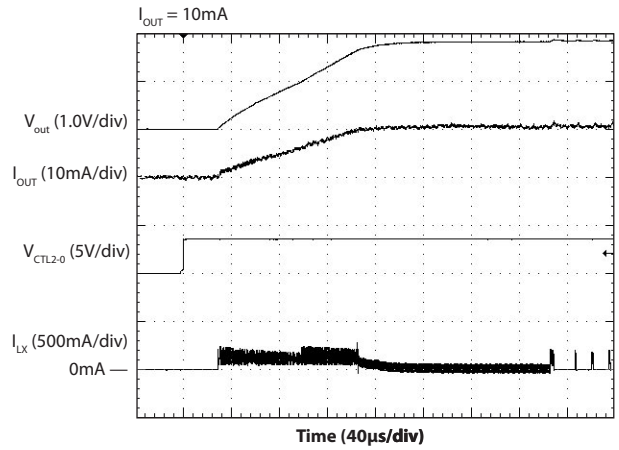
Heavy Load Switching — V_{OUT} = 3.3V



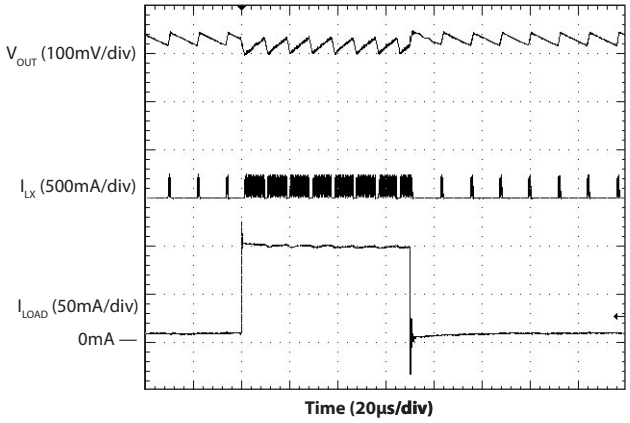
Heavy Load Soft-start



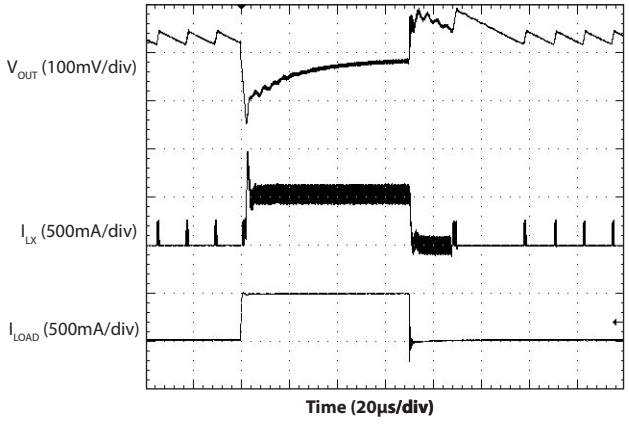
Light Load Soft-start



Load Transient Response — 10 to 100mA

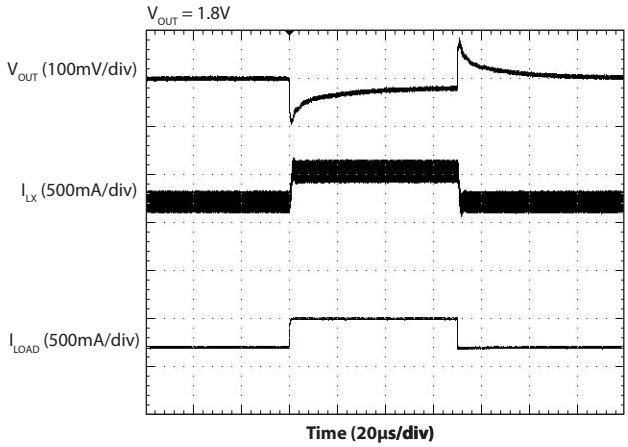


Load Transient Response — 10 to 500mA

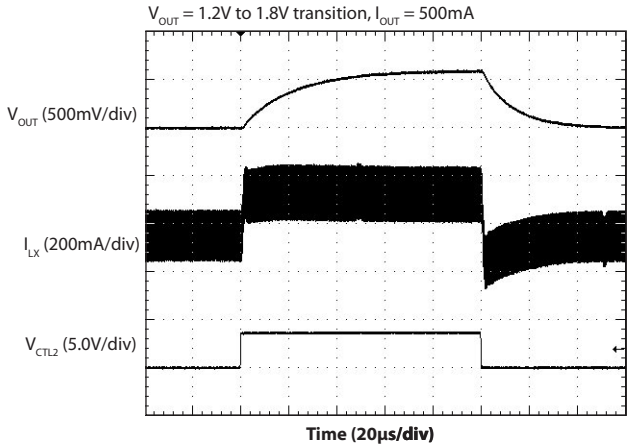


Typical Characteristics (continued)

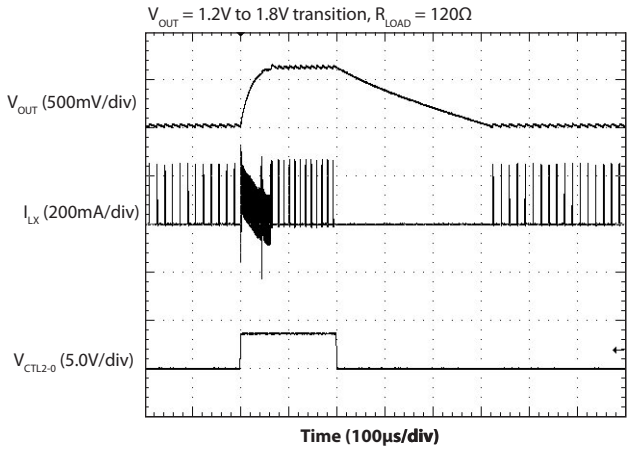
Load Transient Response — 200 to 500mA



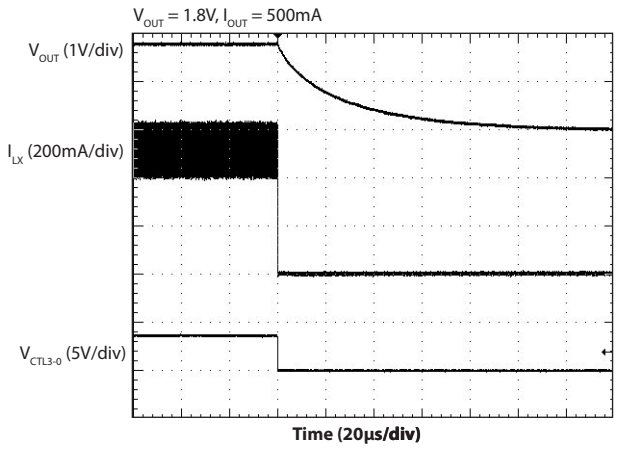
VID Transient Response — PWM



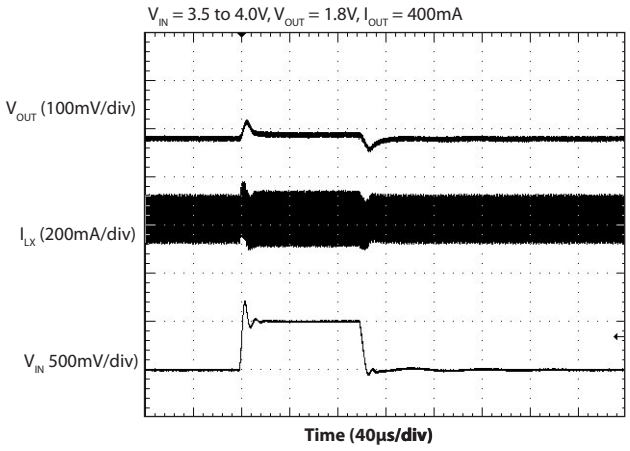
VID Transient Response — PSAVE



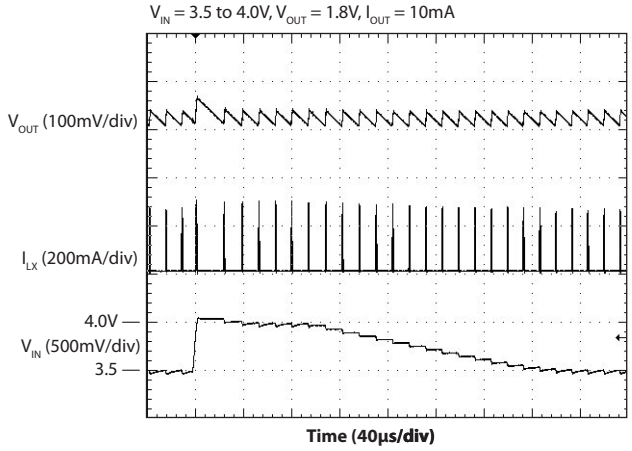
Shutdown Transient Response



Line Transient Response — PWM



Line Transient Response — PSAVE



Pin Descriptions

Pin	Pin Name	Pin Function
1	CTL1A	Control bit 1A — see Table 1, page 2, for output voltage selection. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL1 is pulled above the logic high threshold.
2	CTL0A	Control bit 0A — see Table 1, page 2, for output voltage selection. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL0 is pulled above the logic high threshold.
3	OUTB	Output voltage sense B — output voltage regulation point (connection node of inductor and output capacitor).
4	GNDB	Ground B — reference and power ground for the SC197.
5	LXB	Switching output B — connect an inductor between this pin and the load to filter the pulsed output current.
6	NC	No connection
7	INB	Input power supply B — connect a bypass capacitor from this pin to GND.
8	CTL3B	Control bit 3B — see Table 1, page 2, for output voltage selection. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL3 is pulled above the logic high threshold.
9	CTL2B	Control bit 2B — see Table 1, page 2, for output voltage selection. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL2 is pulled above the logic high threshold.
10	CTL1B	Control bit 1B — see Table 1, page 2, for output voltage selection. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL1 is pulled above the logic high threshold.
11	CTL0B	Control bit 0B — see Table 1, page 2, for output voltage selection. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL0 is pulled above the logic high threshold.
12	OUTA	Output voltage sense A — output voltage regulation point (connection node of inductor and output capacitor).
13	GNDA	Ground A — reference and power ground for the SC197.
14	LXA	Switching output A — connect an inductor between this pin and the load to filter the pulsed output current.
15	NC	No connection
16	INA	Input power supply A — connect a bypass capacitor from this pin to GND.
17	CTL3A	Control bit 3A— see Table 1, page 2, for output voltage selection. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL3 is pulled above the logic high threshold.
18	CTL2A	Control bit 2A — see Table 1, page 2, for output voltage selection. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL2 is pulled above the logic high threshold.

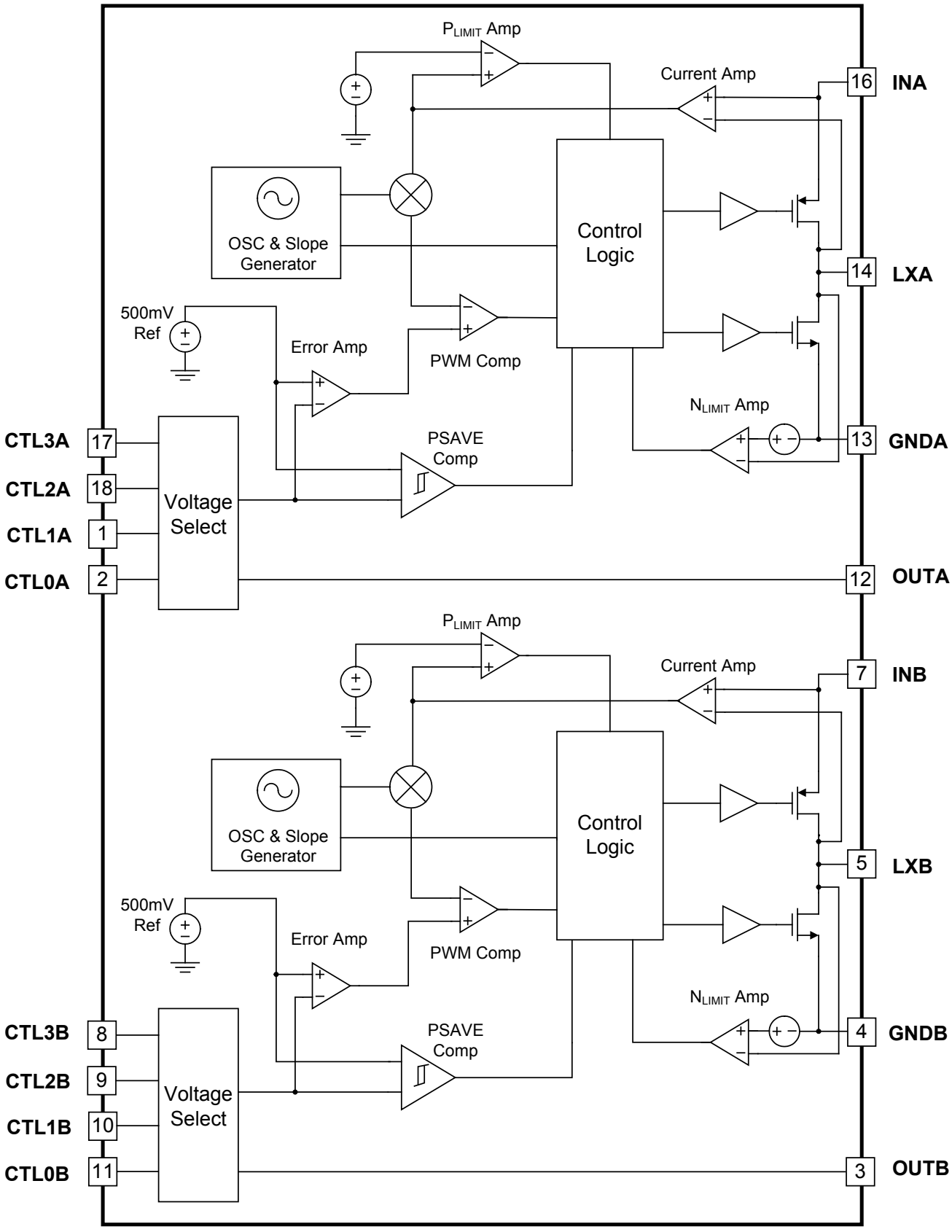
Notes

(1) Any of pins CTL3A, CTL2A, CTL1A, and CTL0A may be connected together to function as a single input for enable and disable.

(2) Any of pins CTL3B, CTL2B, CTL1B, and CTL0B may be connected together to function as a single input for enable and disable.

(3) A and B devices are electrically isolated and share no common connections internally. CTLxA and CTLxB pins may only be connected together when A and B devices share the same power source, INA and INB are connected together, and GNDA and GNDB are connected together. Note that connecting any CTLxA and CTLxB pins together will force both A and B devices to make output voltage changes simultaneously.

Block Diagram



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Applications Information

General Description

The SC197 contains two identical synchronous step-down PWM (Pulse Width Modulated) DC-DC regulators. Each regulator utilizes a 3.5MHz fixed-frequency voltage mode architecture. Each is designed to operate in fixed-frequency PWM mode and enter PSAVE (Power Save) mode utilizing pulse frequency modulation under light load conditions to maximize efficiency. Each regulator requires only two capacitors and a single inductor to be implemented in most systems. The switching frequency has been chosen to minimize the size of the inductor and capacitors while maintaining high efficiency. Output voltage is programmable, eliminating the need for external programming resistors. Loop compensation is also internal, eliminating the need for external components to control stability.

Programmable Output Voltage

The SC197 has 15 fixed output voltage levels which can be individually selected by programming the CTLx(A/B) control pins (see Table 1 on page 2 for settings). Control pins with an "A" suffix refer to the A output, and the "B" suffix refers to the B output. "A" and "B" devices are electrically isolated and share no connections internal to the package. The "A" or "B" device is disabled whenever all four CTLxA or all four CTLxB pins are pulled low. The "A" or "B" device is enabled whenever at least one of the CTLxA or CTLxB pins is pulled high. This configuration eliminates the need for a dedicated enable pin. Each CTLx(A/B) pin is internally pulled down via 1MΩ if V_{IN} is below 1.5V or if the voltage on the control pin is below the input high voltage. This ensures that the output is disabled when power is applied if there are no inputs to the CTLx(A/B) pins. Each weak pull-down is disabled whenever its pin is pulled high and remains disabled until all CTLx(A/B) pins are pulled low.

The output voltage can be set using different methods. If a static output voltage is required, the CTLx(A/B) pins can be tied to either IN or GND to set the desired voltage whenever power is applied at IN. If enable control is required, each CTLx(A/B) pin can be tied to either GND or to a microprocessor I/O line to create the desired control code whenever the control signal is forced high. This approach is equivalent to using the CTLx(A/B) pins collectively as a single enable pin. A third option is to connect each of the four CTLx(A/B) pins to individual microprocessor I/O lines. Any of the 15 output voltages can be programmed using this approach. If only two output voltages are needed, the CTLx(A/B) pins can be combined in a way that will reduce the number of I/O lines to 1, 2, or 3, depending on the control code for each desired voltage. Other CTLx(A/B) pins could be hard wired to GND or IN. This option allows dynamic voltage adjustment for systems that reduce the supply voltage when entering sleep states. Note that applying all zeros to the CTLx(A/B) pins when changing the output voltages will temporarily disable the device, so it is important to avoid this combination when dynamically changing levels.

CTLxA and CTLxB pins may only be connected together when A and B devices share the same power source; i.e., INA and INB pins are connected together, and GNDA and GNDB are connected together. Note that connecting any CTLxA and CTLxB pins together will force both A and B devices to make output voltage changes simultaneously.

Adjustable Output Voltage Selection

If an output voltage other than one of the 15 programmable settings is needed, an external resistor divider network can be added to the SC197 to adjust the output voltage setting. This network scales the output based on the resistor ratio and the programmed output setting. The resistor values can be determined using the equation. Note that V_{OUT} may refer to either the A or B device.

$$V_{OUT} = V_{SET} \times \left[\frac{R_{FB1} + R_{FB2}}{R_{FB2}} \right] + I_{LEAK} \times R_{FB1}$$

where V_{OUT} is the desired output voltage, V_{SET} is the voltage setting selected by the CTLx(A/B) pins, R_{FB1} is the resistor between the output capacitor and the OUT(A/B) pin, R_{FB2} is the resistor between the OUT(A/B) pin and ground, and I_{LEAK} is the leakage current into the OUT(A/B) pin during normal operation. The current into the OUT(A/B) pin is typically 1µA, so the last term of the equation can be neglected if the current through R_{FB2} is much larger than 1µA. Selecting a resistor value of 10kΩ or

Applications Information (continued)

lower will simplify the design. If I_{LEAK} is neglected and R_{FB2} is fixed, R_{FB1} can be determined using the equation.

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - V_{SET}}{V_{SET}}$$

Inserting resistance in the feedback loop will adversely affect the system's transient performance if feed-forward capacitance is not included in the circuit. The circuit in Figure 1 illustrates how the resistor divider and feed-forward capacitor can be added to the SC197 schematic. The value of feed-forward capacitance needed can be determined using the equation.

$$C_{FF} = 4 \times 10^{-6} \times \frac{V_{SET}(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - V_{SET})(V_{SET} - 0.5)}$$

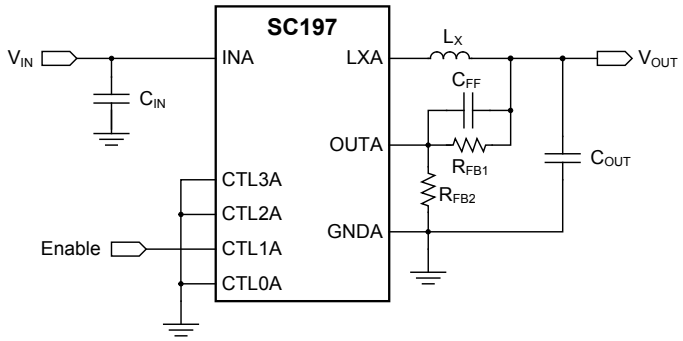

Figure 1 — Application Circuit with External Resistors

To simplify the design, it is recommended to program the output setting to 1.0V, use resistor values smaller than 10kΩ, and include a feed-forward capacitance calculated with the equation above. If the output voltage is set to 1.0V, the previous equation reduces to the following.

$$C_{FF} = 8 \times 10^{-6} \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - 1)}$$

Example:
An output voltage of 1.3V is desired, but this is not a programmable option. What external component values for Figure 1 are needed?

Solution: To keep the circuit simple, set R_{FB2} to 10kΩ so current into the OUT(A/B) pin can be neglected and set the CTL3-0 pins to 0010 (1.0V setting). The necessary component values are as follows:

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - V_{SET}}{V_{SET}} = 3k\Omega$$

$$C_{FF} = 8 \times 10^{-6} \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - 1)} = 5.69nF$$

PWM Operation

Normal PWM operation occurs when the output load current exceeds the PSAVE threshold. In this mode, the PMOS high side switch is activated with the duty cycle required to produce the output voltage programmed by the CTLx(A/B) pins. An internal synchronous NMOS rectifier eliminates the need for an external Schottky diode on the LX(A/B) pin. The duty cycle (percentage of time PMOS is active) increases as V_{IN} decreases to maintain output voltage regulation. As the input voltage approaches the programmed output voltage, the duty cycle approaches 100% (PMOS always on) and the device enters a pass-through mode. This mode remains active until the input voltage increases or the load decreases enough to allow PWM switching to resume.

Power Save Mode Operation

When the load current decreases below the PSAVE threshold, PWM switching stops and the device automatically enters PSAVE mode. This threshold varies depending on the input voltage and output voltage setting, optimizing efficiency for all possible load currents in PWM or PSAVE mode. While in PSAVE mode, output voltage regulation is controlled by a series of switching bursts. During a burst, the inductor current is limited to a peak value which controls the on-time of the PMOS switch. After reaching this peak, the PMOS switch is disabled and the inductor current decreases to near 0mA. Switching bursts continue until the output voltage climbs to V_{OUT} +2.5% or until the PSAVE current limit is reached. Switching is then stopped to eliminate switching losses, enhancing overall efficiency. Switching resumes when the output voltage reaches the lower threshold of V_{OUT} and continues until the upper threshold again is reached. Note that the output voltage is regulated hysteretically while in PSAVE mode between V_{OUT} and V_{OUT} + 2.5%. The

Applications Information (continued)

period and duty cycle while in PSAVE mode are solely determined by V_{IN} and V_{OUT} until PWM mode resumes. This can result in the switching frequency being much lower than the PWM mode frequency.

If the output load current increases enough to cause V_{OUT} to decrease below the PSAVE exit threshold (V_{OUT} -2%), the device automatically exits PSAVE and operates in continuous PWM mode. Note that the PSAVE high and low threshold levels are both set at or above V_{OUT} to minimize undershoot when the SC197 exits PSAVE. Figure 2 illustrates the transitions from PWM mode to PSAVE mode and back to PWM mode.

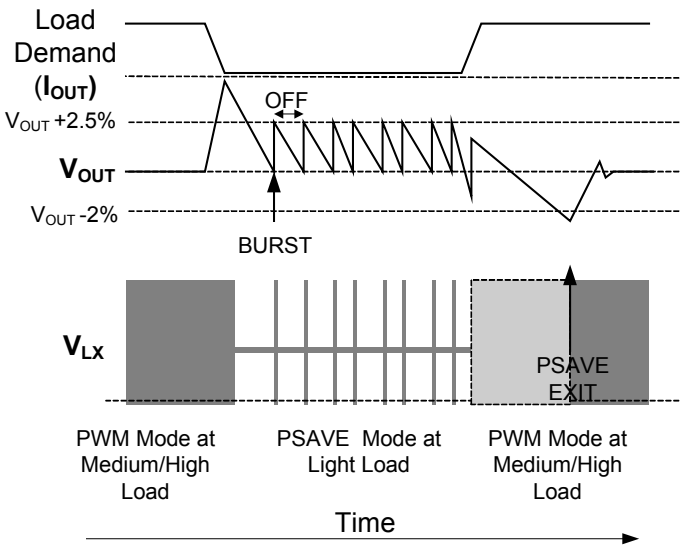

Figure 2 — Transitions Between PWM and PSAVE Modes

Protection Features

The SC197 provides the following protection features:

- Soft-Start Operation
- Over-Voltage Protection
- Current Limit
- Thermal Shutdown
- Under-Voltage Lockout

Soft-Start

The soft-start sequence is activated after a transition from an all zeros CTLx(A/B) code to a non-zero CTLx(A/B) code enables the device. At start-up, the PMOS current limit is stepped through four levels: 25%, 40%, 60%, and 100%. Each step is maintained for 60µs following an internal reference start up of 20µs, resulting in a total nominal start-up period of 260µs. If V_{OUT} reaches 90% of the target within the first 2 steps, the device continues in PSAVE mode at the end of soft-start; otherwise, it goes into PWM mode. Note the V_{OUT} ripple in PSAVE mode can be larger than the ripple in PWM mode.

Over-Voltage Protection

OVP (Over-Voltage Protection) ensures the output voltage does not rise to a level that could damage its load. When V_{OUT} exceeds the regulation voltage by 15%, the PWM drive is disabled. Switching does not resume until V_{OUT} has fallen below the regulation voltage by 2%.

Current Limit

The SC197 switching stage is protected by a current limit function. If the output load exceeds the PMOS current limit for 32 consecutive switching cycles, the device enters fold-back current limit mode and the output current is limited to approximately 150mA. Under these conditions, the output voltage will be the product of I_{FB-LIM} and the load resistance. The load must fall below I_{FB-LIM} for the device to exit fold-back current limit mode. This function makes the device capable of sustaining an indefinite short circuit on its output under fault conditions.

Thermal Shutdown

The SC197 has a thermal shutdown feature to protect the device if the junction temperature exceeds 160°C. During thermal shutdown, the PMOS and NMOS switches are both disabled, tri-stating the LX(A/B) output. When the junction temperature drops by the hysteresis value (20°C), the device goes through the soft-start process and resumes normal operation.

Under-Voltage Lockout

UVLO (Under-Voltage Lockout) activates when the supply voltage drops below the UVLO threshold. This prevents the device from entering an ambiguous state in which regulation cannot be maintained. Hysteresis of approximately 200mV is included to prevent chattering near the threshold.

Inductor Selection

The SC197 is designed to operate with a 1µH inductor between the LX(A/B) pin and the OUT(A/B) pin. Other values may lead to instability, malfunction, or out-of-specification performance. The specified current levels

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Applications Information (continued)

for PSAVE entry, PSAVE exit, and current limit are dependent on the inductor value.

The SC197 converter has internal loop compensation. The compensation is designed to work with a specific single-pole output filter corner frequency defined by the equation.

$$f_C = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

where L = 1µH and C_{OUT} = 10µF.

When selecting output filter components, the LC product should not vary over a wide range. Selection of smaller inductor and capacitor values will move the corner frequency, potentially impacting system stability.

It is also important to consider the change in inductance with DC bias current when choosing an inductor. The inductor saturation current is specified as the current at which the inductance drops a specific percentage from the nominal value (approximately 30%). Except for short-circuit or other fault conditions, the peak current must always be less than the saturation current specified by the manufacturer. The peak current is the maximum load current plus one half of the inductor ripple current at the maximum input voltage. Load and/or line transients can cause the peak current to exceed this level for short durations. Maintaining the peak current below the inductor saturation specification keeps the inductor ripple current and the output voltage ripple at acceptable levels. Manufacturers often provide graphs of actual inductance and saturation characteristics versus applied inductor current. The saturation characteristics of the inductor can vary significantly with core temperature. Core and ambient temperatures should be considered when examining the core saturation characteristics.

When the inductor value has been determined, the DC resistance (DCR) must be examined. Efficiency can be optimized by lowering the inductor's DCR as much as possible. Low DCR in an inductor requires either more surface area for the increased wire diameter or fewer turns to reduce the length of the copper winding. Fewer turns requires an inductor core with a larger cross-sectional area in order to maintain the same saturation characteristics. The inductor size must always be considered when examining the inductor DCR to determine the best compromise between DCR and component area on a PCB. Note that the ripple component of the inductor is a small percentage of the DC load. AC losses in the inductor core and winding do not contribute significantly to the total losses.

Magnetic fields associated with the output inductor can interfere with nearby circuitry. This can be minimized by the use of low-noise shielded inductors which use the minimum gap possible to limit the distance that magnetic fields can radiate from the inductor. Shielded inductors, however, typically have a higher DCR and are, therefore, less efficient than a similar sized non-shielded inductor.

Final inductor selection depends on various design considerations such as efficiency, EMI, size, and cost. Table 2 lists the manufacturers of recommended inductor options. The inductors with larger packages tend to provide better overall efficiency, while the smaller package inductors provide decent efficiency with reduced footprint or height. The saturation current ratings and DC characteristics are also shown.

Table 2 — Recommended Inductors

Manufacturer Part Number	L (µH)	DCR (Ω)	Saturation Current (mA)	L at 400mA (µH)	Dimensions LxWxH (mm)
Murata LQM21PN1R0MC0	1.0±20%	0.19	800	0.75	2.0x1.25x0.55
Murata LQM2HPN1R0MJ0	1.0±20%	0.09	1500	0.95	2.5x2.0x1.1
Murata LQM31PN1R0M00	1.0±20%	0.12	1200	0.95	3.2x1.6x0.85
Taiyo Yuden CKP25201R0M-T	1.0±20%	0.08	800	0.88	2.5x2.0x1.0
Toko MDT2012-CR1R0N	1.0±30%	0.08	1350	1.00	2.0x1.25x1.0
FDK MIPSZ2012D1R0	1.0±30%	0.09	1100	1.00	2.0x1.25x1.0
FDK MIPSU2520D1R0	1.0±30%	0.08	1300	0.78	2.5x2.0x0.5
FDK MIPSA2520D1R0	1.3±30%	0.09	1200	1.20	2.5x2.0x1.2
Taiyo Yuden BRC1608T1R0M	1.0±20%	0.18	850	0.90	1.6x0.8x0.8

Applications Information (continued)

C_{OUT} Selection

The internal voltage loop compensation in the SC197 limits the minimum output capacitor value to 10µF. This is due to its influence on the the loop crossover frequency, phase margin, and gain margin. Increasing the output capacitor above this minimum value will reduce the crossover frequency and provide greater phase margin.

The output capacitor determines the output voltage ripple and contributes load current during large step load transitions. A capacitor between 10µF and 22µF will usually be adequate in stabilizing the output during large load transitions.

Capacitors with X7R or X5R ceramic dielectric are recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

In addition to ensuring stability, the output capacitor serves other important functions. This capacitor determines the output voltage ripple — as capacitance increases, ripple voltage decreases. It also supplies current during a large load step for a few switching cycles until the control loop responds (typically 3 switching cycles). Once the loop responds, regulation is restored and the desired output is reached. During the period prior to PWM operation resuming, the relationship between output voltage and output capacitance can be approximated using the following equation.

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f}$$

This equation can be used to approximate the minimum output capacitance needed to ensure voltage does not droop below an acceptable level. For example, a load step from 50mA to 400mA requiring droop less than 50mV would require the minimum output capacitance to be as follows.

$$C_{OUT} = \frac{3 \times 0.4}{0.05 \times 4 \times 10^{6}} = 6.0\mu F$$

In this example, using a standard 10µF capacitor would be adequate to keep voltage droop less than the desired limit. Note that if the voltage droop limit were decreased from 50mV to 25mV, the output capacitance would need to be increased to at least 12µF (twice as much capacitance for half the droop). Capacitance will decrease from the nominal value when a ceramic capacitor is biased with a DC current, so it is important to select a capacitor whose value exceeds the necessary capacitance value at the programmed output voltage. Check the manufacturer's capacitance vs. DC voltage graphs when selecting an output capacitor to ensure the capacitance will be adequate.

Table 3 lists the manufacturers of recommended output capacitor options.

Table 3 — Recommended Output Capacitors

Manufacturer Part Nunber	Value (µF)	Type	Rated Voltage (VDC)	Dimensions LxWxH (mm) Case Size
Murata GRM188R60J106ME47D	10±20%	X5R	6.3	1.6x0.8x0.8 0603
Murata GRM21BR60J106K	10±10%	X5R	6.3	2.0x1.25x1.25 0805
Taiyo Yuden JMK107BJ106MA-T	10±20%	X5R	6.3	1.6x0.8x0.8 0603
TDK C1608X5R0J106MT	10±20%	X5R	6.3	1.6x0.8x0.8 0603

C_{IN} Selection

The SC197 input source current will appear as a DC supply current with a triangular ripple imposed on it. To prevent large input voltage ripple, a low ESR ceramic capacitor is required. A minimum value of 4.7µF should be used. It is important to consider the DC voltage coefficient characteristics when determining the actual required value. For example, a 10µF, 6.3V, X5R ceramic capacitor with 5V DC applied may exhibit a capacitance as low as 4.5µF. The value of required input capacitance is estimated by determining the acceptable input ripple voltage and calculating the minimum value required for C_{IN} using the equation

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{\Delta V}{I_{OUT}} - ESR\right) f}$$

Applications Information (continued)

The input voltage ripple is at maximum level when the input voltage is twice the output voltage (50% duty cycle scenario).

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the PMOS switch. Low ESR/ESL X5R ceramic capacitors are recommended for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IN and GND pins of the SC197. Table 4 lists the recommended input capacitor options from different manufacturers.

Table 4 — Recommended Input Capacitors

Manufacturer Part Nunber	Value (µF)	Type	Rated Voltage (VDC)	Dimensions LxWxH (mm) Case Size
Murata GRM188R60J475K	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603
Murata GRM188R60J106K	10±10%	X5R	6.3	1.6x0.8x0.8 0603
Taiyo Yuden JMK107BJ475KA	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603
TDK C1608X5R0J475KT	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603

PCB Layout Considerations

The layout diagram in Figure 3 shows a recommended PCB top-layer for the SC197 and supporting components. Specified layout rules must be followed since the layout is critical for achieving the performance specified in the Electrical Characteristics table. Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following guidelines are recommended for designing a PCB layout:

1. C_{INA} and C_{INB} should be placed as close to the IN and NC pins as possible. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to minimize trace impedance. This will also minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Keep the LXA and LXB pin traces as short as possible to minimize pickup of high frequency switching edges to other parts of the circuit.
3. Route a trace from the OUTA pin and connect it directly to the terminal of C_{OUTA}. Repeat by adding a trace between the OUTB pin and the C_{OUTB} capactor. Provide space between the OUTA trace and L_{XA} to minimize noise and magnetic interference. Also provide space between OUTB and L_{XA}.
4. C_{OUTA} and C_{OUTB} should have a direct return to ground with minimized trace length.
5. Use a ground plane referenced to ground pins GNDA and GNDB. Use multiple vias to connect to ground to further reduce noise and interference on sensitive circuit nodes.
6. Minimize the resistance from the output and ground pins to the load. This will reduce errors in DC regulation due to voltage drops in the traces.

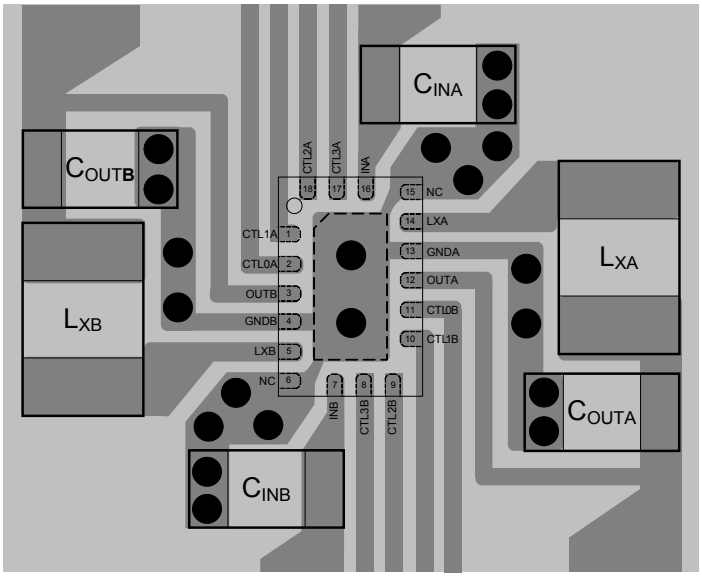
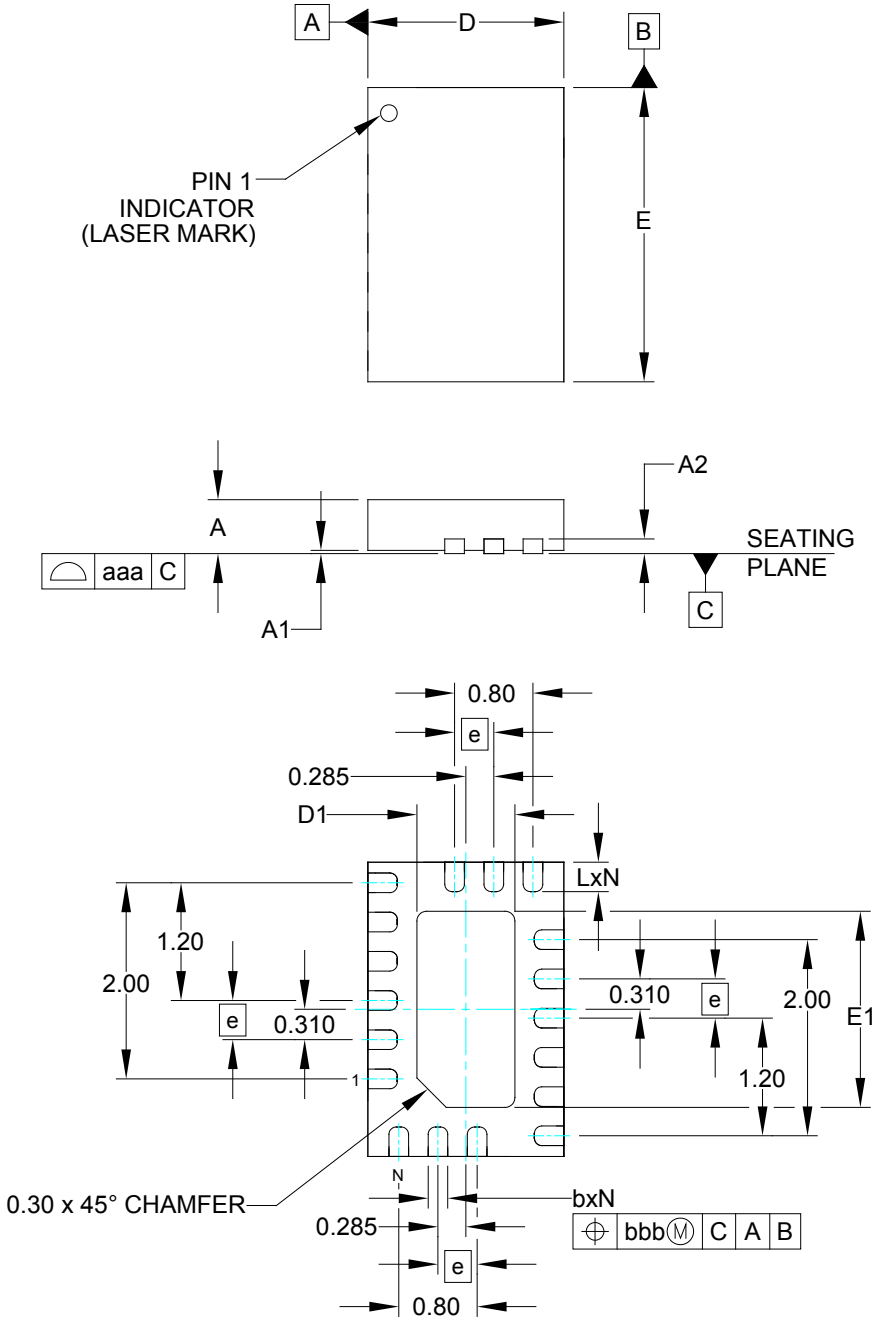


Figure 3 — Recommended PCB Layout

Outline Drawing — MLPQ-UT18

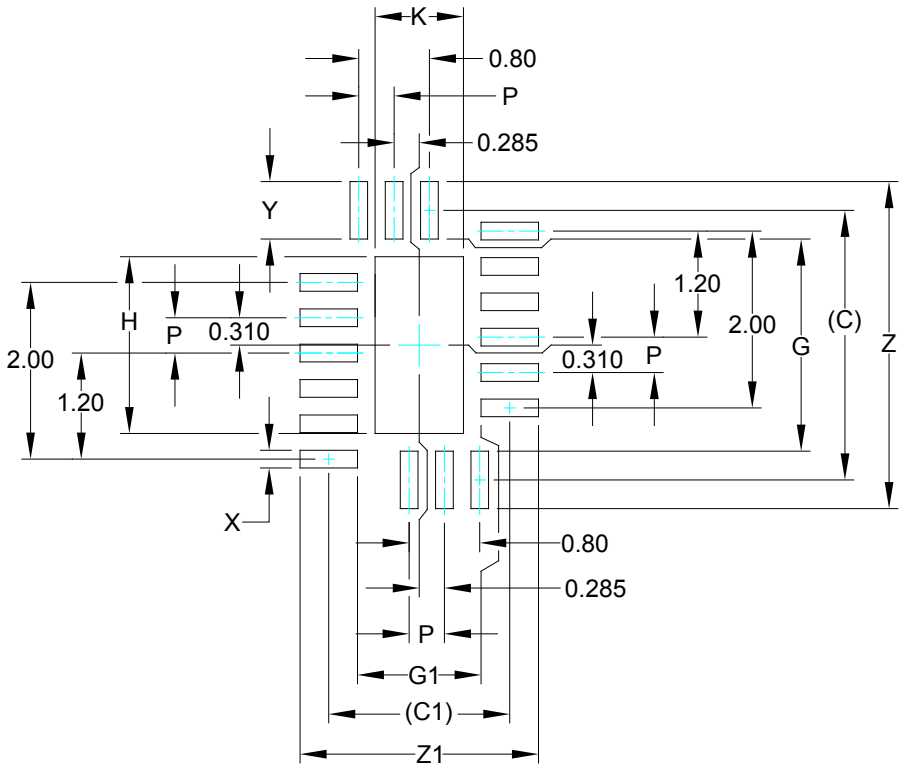


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.50	-	0.60
A1	0.00	-	0.05
A2		(0.152)	
b	0.15	0.20	0.25
D	1.90	2.00	2.10
D1	0.85	1.00	1.10
E	2.90	3.00	3.10
E1	1.85	2.00	2.10
e		0.40 BSC	
L	0.25	0.30	0.35
N		18	
aaa		0.08	
bbb		0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ-UT18



DIMENSIONS	
DIM	MILLIMETERS
C	(3.05)
C1	(2.05)
G	2.40
G1	1.40
H	2.00
K	1.00
P	0.40
X	0.20
Y	0.65
Z	3.70
Z1	2.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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