ITG-3400
Product Specification
Revision 1.0

TABLE OF CONTENTS

TABLE OF FIGURES 4

TABLE OF TABLES 5

1 DOCUMENT INFORMATION 6

1.1 REVISION HISTORY 6

1.2 PURPOSE AND SCOPE 7

1.3 PRODUCT OVERVIEW 7

1.4 APPLICATIONS 7

2 FEATURES 8

2.1 GYROSCOPE FEATURES 8

2.2 ADDITIONAL FEATURES 8

3 ELECTRICAL CHARACTERISTICS 9

3.1 GYROSCOPE SPECIFICATIONS 9

3.2 ELECTRICAL SPECIFICATIONS 10

3.3 I2C TIMING CHARACTERIZATION 13

3.4 SPI TIMING CHARACTERIZATION 14

3.5 ABSOLUTE MAXIMUM RATINGS 15

4 APPLICATIONS INFORMATION 16

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION 16

4.2 TYPICAL OPERATING CIRCUIT 17

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS 17

4.4 BLOCK DIAGRAM 18

4.5 OVERVIEW 18

4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING 18

4.7 I2C AND SPI SERIAL COMMUNICATIONS INTERFACES 19

4.8 CLOCKING 20

4.9 SENSOR DATA REGISTERS 20

4.10 FIFO 21

4.11 INTERRUPTS 21

4.12 DIGITAL-OUTPUT TEMPERATURE SENSOR 21

4.13 BIAS AND LDOS 21

4.14 CHARGE PUMP 21

4.15 STANDARD POWER MODES 21

5 PROGRAMMABLE INTERRUPTS 23

6 DIGITAL INTERFACE 24

6.1 I2C AND SPI SERIAL INTERFACES 24

6.2 I2C INTERFACE..24

6.3 I2C COMMUNICATIONS PROTOCOL 24

6.4 I^2C TERMS 27

6.5 SPI INTERFACE 28

7 SERIAL INTERFACE CONSIDERATIONS...29

7.1 ITG-3400 SUPPORTED INTERFACES...29

8 ASSEMBLY 30

8.1 ORIENTATION OF AXES 30

8.2 PACKAGE DIMENSIONS 31

8.3 PCB DESIGN GUIDELINES..32

8.4 ASSEMBLY PRECAUTIONS 33

8.5 STORAGE SPECIFICATIONS...36

8.6 PACKAGE MARKING SPECIFICATION...36

8.7 TAPE & REEL SPECIFICATION 37

8.8 LABEL 38

8.9 PACKAGING...39

8.10 REPRESENTATIVE SHIPPING CARTON LABEL 40

9 ENVIRONMENTAL COMPLIANCE...41

Table of Figures

Figure 1 I2C Bus Timing Diagram 13
Figure 2 SPI Bus Timing Diagram 14
Figure 3 Pin out Diagram for ITG-3400 3.0x3.0x0.9mm QFN 16
Figure 4 ITG-3400 QFN Application Schematic. (a) I2C operation, (b) SPI operation. 17
Figure 5 ITG-3400 Block Diagram 18
Figure 6 ITG-3400 Solution Using I^2C Interface 19
Figure 7 ITG-3400 Solution Using SPI Interface 20

Table of Tables

Table 1 Gyroscope Specifications 9
Table 2 D.C. Electrical Characteristics 10
Table 3 A.C. Electrical Characteristics 12
Table 4 I^2C Timing Characteristics 13
Table 5 SPI Timing Characteristics 14
Table 6 fCLK = 20MHz 15
Table 7 Absolute Maximum Ratings 15
Table 8 Signal Descriptions 16
Table 9 Bill of Materials 17
Table 10 Standard Power Modes for ITG-3400 22
Table 11 Table of Interrupt Sources 23
Table 12 Serial Interface 24
Table 13 I^2C Terms 27

1 Document Information

1.1 Revision History

Revision Date	Revision	Description
12/24/2013	1.0	Initial Release

1.2 Purpose and Scope

This document is a preliminary product specification, providing a description, specifications, and design related information on the ITG-3400™ gyroscope device. The device is housed in a small 3x3x0.9mm 24-pin QFN package.

Specifications are subject to change without notice. Final specifications will be updated based upon characterization of production silicon. For references to register map and descriptions of individual registers, please refer to the ITG-3400 Register Map and Register Descriptions document.

1.3 Product Overview

The ITG-3400 is a 3-axis gyroscope that is housed in a small 3x3x0.9mm (24-pin QFN) package. It also features a 4096-byte FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. With its dedicated I^2C sensor bus, the ITG-3400 directly accepts inputs from external I^2C devices.

The gyroscope has a programmable full-scale range of ±250, ±500, ±1000, and ±2000 degrees/sec. Factory-calibrated initial sensitivity of the sensor reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, a precision clock with 1% drift from -40°C to 85°C, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71 to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

Communication with all registers of the device is performed using either I^2C at 400kHz or SPI at 1MHz. For applications requiring faster communications, the sensor and interrupt registers may be read using SPI at 20MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 3x3x0.9mm (24-pin QFN), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

1.4 Applications

- Motion UI
- Handset gaming
- Location based services, points of interest, and dead reckoning
- Health and sports monitoring
- Power management

2 Features

2.1 Gyroscope Features

The triple-axis MEMS gyroscope in the ITG-3400 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±250, ±500, ±1000, and ±2000°/sec and integrated 16-bit ADCs
- Digitally-programmable low-pass filter
- Gyroscope operating current: 3.2mA
- Factory calibrated sensitivity scale factor

2.2 Additional Features

The ITG-3400 includes the following additional features:

- VDD supply voltage range of 1.8 – 3.3V ± 5%
- Smallest and thinnest QFN package for portable devices: 3x3x0.9mm (24-pin QFN)
- 4096 byte FIFO buffer enables the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope and temp sensor
- 10,000 *g* shock tolerant
- 400kHz Fast Mode I^2C for communicating with all registers
- 1MHz SPI serial interface for communicating with all registers
- 20MHz SPI serial interface for reading sensor and interrupt registers
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 Electrical Characteristics

3.1 Gyroscope Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	FS_SEL=0		±250		º/s	
	FS_SEL=1		±500		º/s	
	FS_SEL=2		±1000		º/s	
	FS_SEL=3		±2000		º/s	
Gyroscope ADC Word Length			16		bits	
Sensitivity Scale Factor	FS_SEL=0		131		LSB/(º/s)	
	FS_SEL=1		65.5		LSB/(º/s)	
	FS_SEL=2		32.8		LSB/(º/s)	
	FS_SEL=3		16.4		LSB/(º/s)	
Sensitivity Scale Factor Tolerance	25°C		±4		%	1
Sensitivity Scale Factor Variation Over Temperature	0°C to +55°C		±10		%	1
Nonlinearity	Best fit straight line; 25°C		0.2		%	1
Cross-Axis Sensitivity			±2		%	
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±60		º/s	1
ZRO Variation Over Temperature	0°C to +55°C		±60		º/s	
GYROSCOPE NOISE PERFORMANCE (FS_SEL=0)						
Total RMS Noise	DLPFCFG=2 (92 Hz)		0.7		º/s-rms	1
GYROSCOPE MECHANICAL FREQUENCIES		25	27	29	KHz	1
LOW PASS FILTER RESPONSE	Programmable Range	5		250	Hz	
GYROSCOPE START-UP TIME	From Sleep mode		35		ms	1
OUTPUT DATA RATE	Programmable, Normal (Filtered) mode	4		8000	Hz	1

Table 1 Gyroscope Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.2 Electrical Specifications

3.2.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	Units	Notes
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.45	V	
VDDIO		1.71	1.8	3.45	V	
SUPPLY CURRENTS						
Normal Mode	3-axis Gyroscope		3.2		mA	1
Standby Mode			1.6		mA	1
Full-Chip Sleep Mode			6		µA	1
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	

Table 2 D.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.2.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameter	Conditions	MIN	TYP	MAX	Units	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.1		100	ms	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
Sensitivity	Untrimmed		333.87		LSB/°C	
Room Temp Offset	21°C		0		LSB	
Power-On RESET						
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01	20	100	ms	1
Start-up time for register read/write	From power-up		11	100	ms	1
I²C ADDRESS	AD0 = 0 AD0 = 1		1101000 1101001			
DIGITAL INPUTS (SYNC, AD0, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1MΩ;			0.1*VDDIO	V	
$V_{OL.INT1}$, INT Low-Level Output Voltage	OPEN=1, 0.3mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	
I2C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4V V_{OL}=0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		250	ns	
INTERNAL CLOCK SOURCE						
Sample Rate	Fchoice=0,1,2 SMPLRT_DIV=0		32		kHz	
	Fchoice=3; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	

Parameter	Conditions	MIN	TYP	MAX	Units	NOTES
	Fchoice=3; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	
Clock Frequency Initial Tolerance	CLK_SEL=0, 6; 25°C	-5		+5	%	1
	CLK_SEL=1,2,3,4,5; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=0,6	-10		+10	%	1
	CLK_SEL=1,2,3,4,5		±1		%	1
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low Speed Characterization		100 ±10%		kHz	
	High Speed Characterization		1 ±10%		MHz	
SPI Operating Frequency, Sensor and Interrupt Registers Read Only			20 ±10%		MHz	
I^2C Operating Frequency	All registers, Fast-mode			400	kHz	
	All registers, Standard-mode			100	kHz	

Table 3 A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.3 I2C Timing Characterization

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency				400	kHz	
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	
t_{LOW}, SCL Low Period		1.3			µs	
t_{HIGH}, SCL High Period		0.6			µs	
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	
C_b, Capacitive Load for each Bus Line			< 400		pF	
$t_{VD.DAT}$, Data Valid Time				0.9	µs	
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	

Table 4 I²C Timing Characteristics

Notes:

1. Timing Characteristics apply to both Primary and Auxiliary I2C Bus
2. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

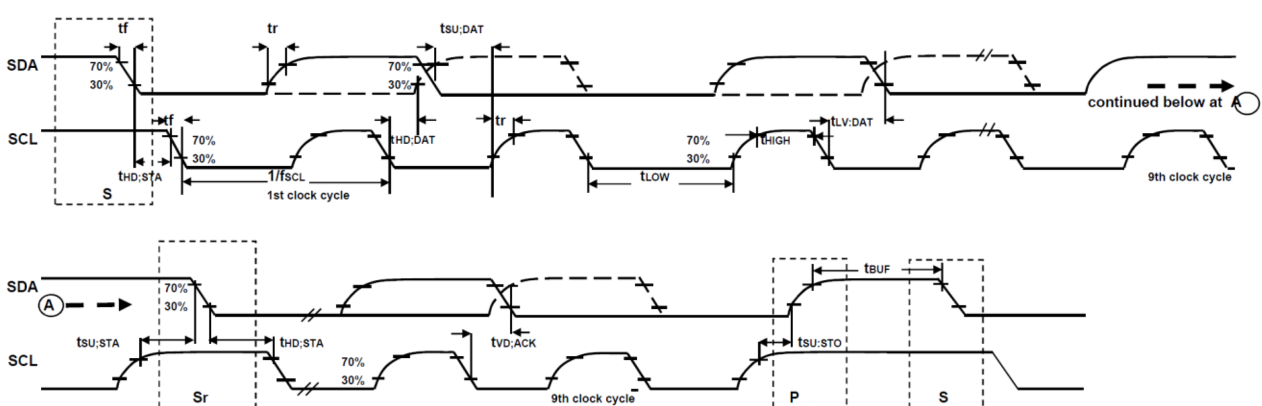


Figure 1 I2C Bus Timing Diagram

3.4 SPI Timing Characterization

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
SPI TIMING						
f_{SCLK}, SCLK Clock Frequency				1	MHz	
t_{LOW}, SCLK Low Period		400			ns	
t_{HIGH}, SCLK High Period		400			ns	
$t_{SU.CS}$, CS Setup Time		8			ns	
$t_{HD.CS}$, CS Hold Time		500			ns	
$t_{SU.SDI}$, SDI Setup Time		11			ns	
$t_{HD.SDI}$, SDI Hold Time		7			ns	
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF			100	ns	
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20pF	4			ns	
$t_{DIS.SDO}$, SDO Output Disable Time				50	ns	

Table 5 SPI Timing Characteristics

Notes:

3. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

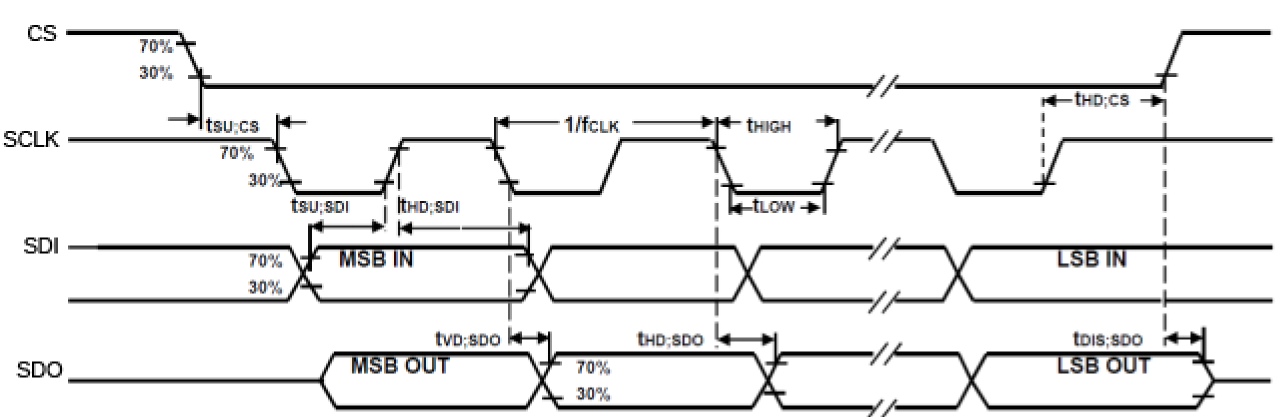


Figure 2 SPI Bus Timing Diagram

3.4.1 fSCLK = 20MHz

Parameters	Conditions	Min	Typical	Max	Units
SPI TIMING					
f_{SCLK}, SCLK Clock Frequency		0.9		20	MHz
t_{LOW}, SCLK Low Period		-		-	ns
t_{HIGH}, SCLK High Period		-		-	ns
$t_{SU.CS}$, CS Setup Time		1			ns
$t_{HD.CS}$, CS Hold Time		1			ns

$t_{SU.SDI}$, SDI Setup Time		0			ns
$t_{HD.SDI}$, SDI Hold Time		1			ns
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF		25		ns
$t_{DIS.SDO}$, SDO Output Disable Time				25	ns

Table 6 fCLK = 20MHz

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

3.5 Absolute Maximum Ratings

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5V to +4V
Supply Voltage, VDDIO	-0.5V to +4V
PLLFILT	-0.5V to 2V
Input Voltage Level (AD0, SYNC, INT, SCL, SDA)	-0.5V to VDD + 0.5V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2kV (HBM); 250V (MM)
Latch-up	JEDEC Class II (2),125°C ±100mA

Table 7 Absolute Maximum Ratings

4 Applications Information

4.1 Pin Out Diagram and Signal Description

Pin Number	Pin Name	Pin Description
8	VDDIO	Digital I/O supply voltage
9	AD0 / SDO	I^2C Slave Address LSB (AD0); SPI serial data output (SDO)
10	REGOUT	Regulator filter capacitor connection
11	FSYNC	Frame synchronization digital input. Connect to GND if unused.
12	INT	Interrupt digital output (totem pole or open-drain)
13	VDD	Power supply voltage and Digital I/O supply voltage
18	GND	Power supply ground
19	RESV	Reserved. Do not connect.
20	RESV	Reserved. Connect to GND.
22	nCS	Chip select (SPI mode only)
23	SCL / SCLK	I^2C serial clock (SCL); SPI serial clock (SCLK)
24	SDA / SDI	I^2C serial data (SDA); SPI serial data input (SDI)
1 – 7, 14 – 17, 21	NC	No Connect pins. Do not connect.

Table 8 Signal Descriptions

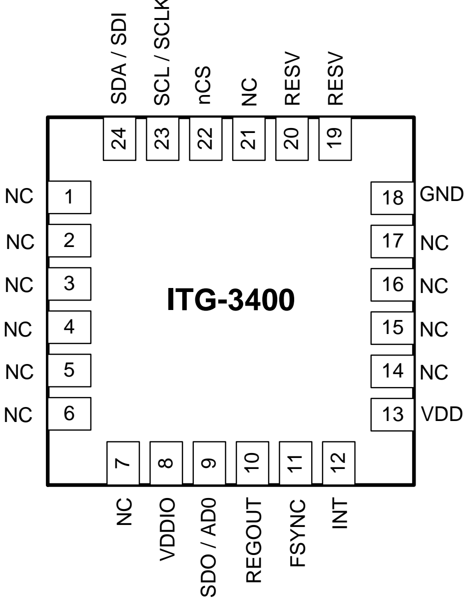


Figure 3 Pin out Diagram for ITG-3400 3.0x3.0x0.9mm QFN

4.2 Typical Operating Circuit

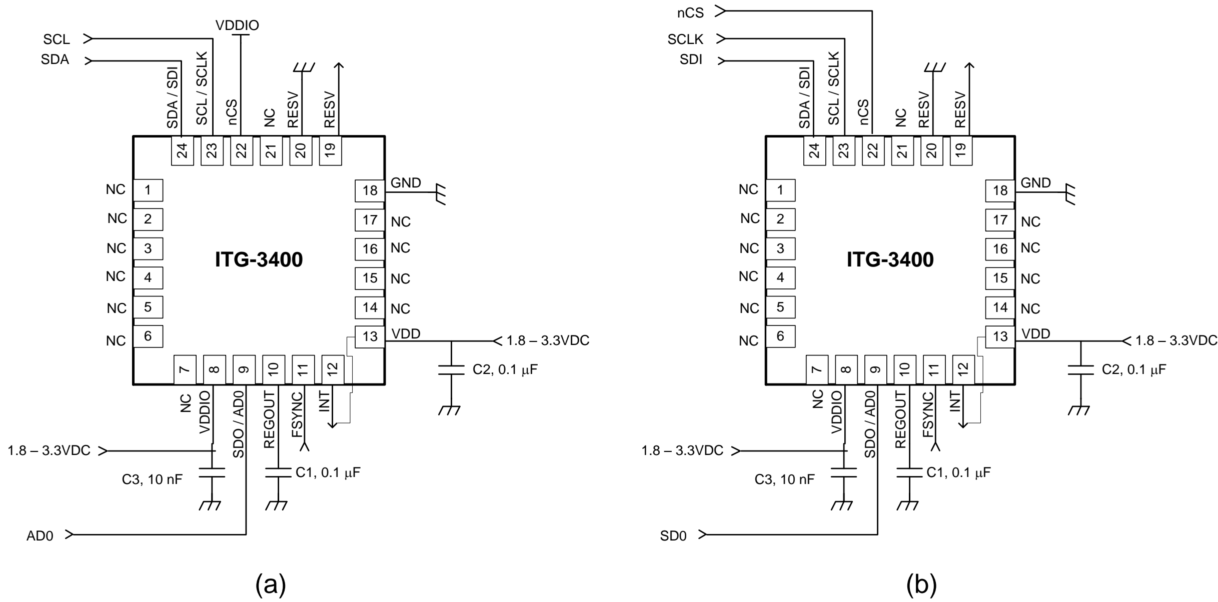


Figure 4 ITG-3400 QFN Application Schematic. (a) I2C operation, (b) SPI operation.

4.3 Bill of Materials for External Components

Component	Label	Specification	Quantity
PLL Filter Capacitor	C1	Ceramic, X7R, 0.1µF ±10%, 2V	1
VDD Bypass Capacitor	C2	Ceramic, X7R, 0.1µF ±10%, 4V	1
VDDIO Bypass Capacitor	C3	Ceramic, X7R, 10nF ±10%, 4V	1

Table 9 Bill of Materials

4.4 Block Diagram

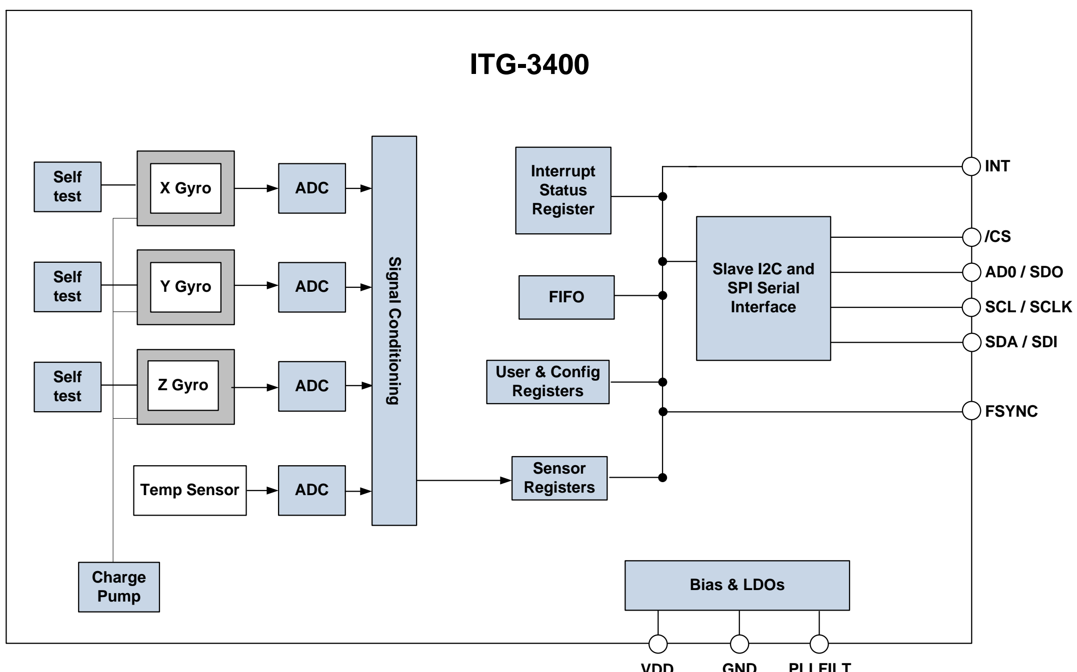


Figure 5 ITG-3400 Block Diagram

4.5 Overview

The ITG-3400 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Primary I^2C and SPI serial communications interfaces
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 Three-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning

The ITG-3400 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered

to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

4.7 I2C and SPI Serial Communications Interfaces

The ITG-3400 communicates to a system processor using either a SPI or an I^2C serial interface. The ITG-3400 always acts as a slave when communicating to the system processor. The LSB of the of the I^2C slave address is set by pin 4 (AD0).

4.7.1 ITG-3400 Solution Using I2C Interface

In the figure below, the system processor is an I^2C master to the ITG-3400.

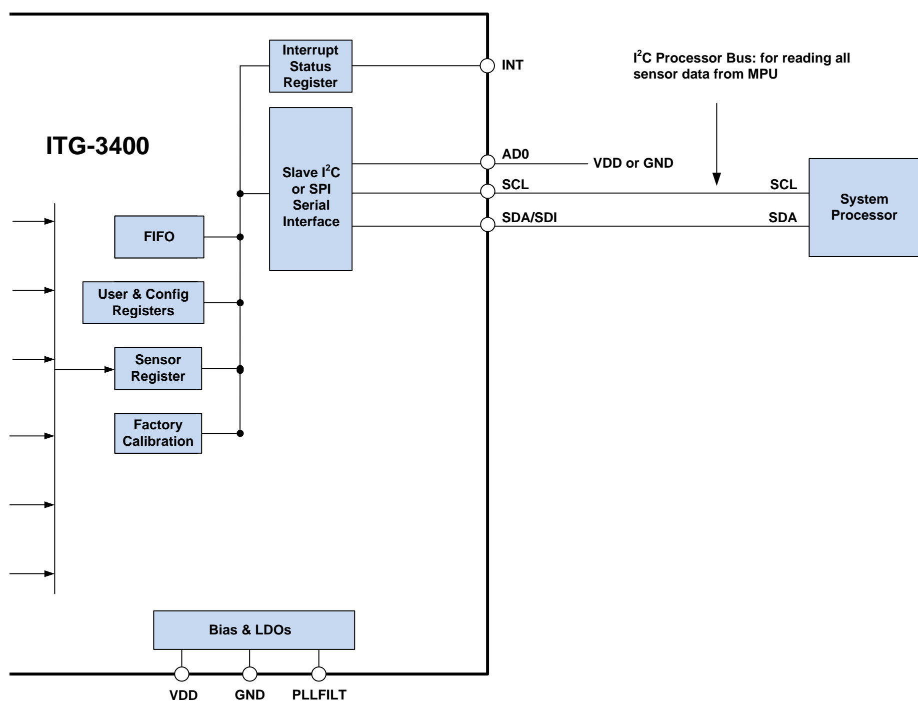


Figure 6 ITG-3400 Solution Using I^2C Interface

4.7.2 ITG-3400 Solution Using SPI Interface

In the figure below, the system processor is an SPI master to the ITG-3400. Pins 2, 3, 4, and 5 are used to support the SCLK, SDI, SDO, and CS signals for SPI communications.

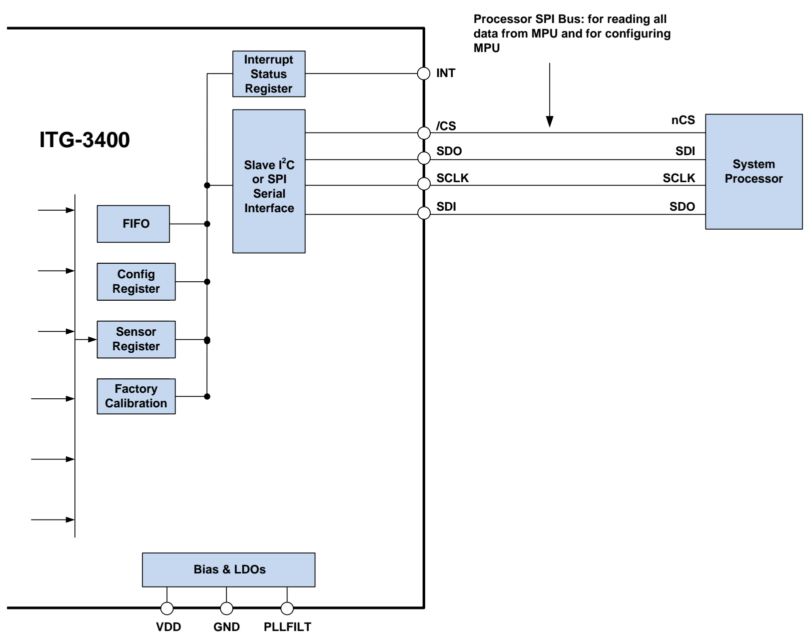


Figure 7 ITG-3400 Solution Using SPI Interface

4.8 Clocking

The ITG-3400 has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

- An internal relaxation oscillator
- Any of the X, Y, or Z gyros (MEMS oscillators with a variation of ±1% over temperature)

Selection of the source for generating the internal synchronous clock depends on the requirements for power consumption and clock accuracy. These requirements will most likely vary by mode of operation.

There are also start-up conditions to consider. When the ITG-3400 first starts up, the device uses its internal clock until programmed to operate from another source. This allows the user, for example, to wait for the MEMS oscillators to stabilize before they are selected as the clock source.

4.9 Sensor Data Registers

The sensor data registers contain the latest gyro, auxiliary sensor, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.10 FIFO

The ITG-3400 contains a 4096-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, temperature readings, auxiliary sensor readings, and SYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

For further information regarding the FIFO, please refer to the ITG-3400 Register Map and Register Descriptions document.

4.11 Interrupts

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); and (2) new data is available to be read (from the FIFO and Data registers). The interrupt status can be read from the Interrupt Status register.

For further information regarding interrupts, please refer to the ITG-3400 Register Map and Register Descriptions document.

4.12 Digital-Output Temperature Sensor

An on-chip temperature sensor and ADC are used to measure the ITG-3400 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.13 Bias and LDOs

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ITG-3400. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at PLLFILT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.14 Charge Pump

An on-chip charge pump generates the high voltage required for the MEMS oscillators.

4.15 Standard Power Modes

The following table lists the user-accessible power modes for ITG-3400.

Mode	Name	Gyro
1	Sleep Mode	Off
2	Standby Mode	Drive On
5	Gyroscope Mode	On

Table 10 Standard Power Modes for ITG-3400

Notes:

1. Power consumption for individual modes can be found in section 3.2.1.

5 Programmable Interrupts

The ITG-3400 has a programmable interrupt system which can generate an interrupt signal on the INT pin. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

Interrupt Name	Module
FIFO Overflow	FIFO
Data Ready	Sensor Registers
I^2C Master errors: Lost Arbitration, NACKs	I^2C Master
I^2C Slave 4	I^2C Master

Table 11 Table of Interrupt Sources

For information regarding the interrupt enable/disable registers and flag registers, please refer to the ITG-3400 Register Map and Register Descriptions document. Some interrupt sources are explained below.

6 Digital Interface

6.1 I2C and SPI Serial Interfaces

The internal registers and memory of the ITG-3400 can be accessed using either I^{2}C at 400 kHz or SPI at 1MHz. SPI operates in four-wire mode.

Pin Number	Pin Name	Pin Description
8	VDDIO	Digital I/O supply voltage.
9	AD0 / SDO	I^{2}C Slave Address LSB (AD0); SPI serial data output (SDO)
23	SCL / SCLK	I^{2}C serial clock (SCL); SPI serial clock (SCLK)
24	SDA / SDI	I^{2}C serial data (SDA); SPI serial data input (SDI)

Table 12 Serial Interface

Note:

To prevent switching into I^{2}C mode when using SPI, the I^{2}C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in Section 6.3.

For further information regarding the *I2C_IF_DIS* bit, please refer to the ITG-3400 Register Map and Register Descriptions document.

6.2 I2C Interface

I^{2}C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I^{2}C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ITG-3400 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the ITG-3400 is b110111X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin AD0. This allows two ITG-3400s to be connected to the same I^{2}C bus. When used in this configuration, the address of the one of the devices should be b1101110 (pin AD0 is logic low) and the address of the other should be b1101111 (pin AD0 is logic high).

6.3 I2C Communications Protocol

START (S) and STOP (P) Conditions

Communication on the I^{2}C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

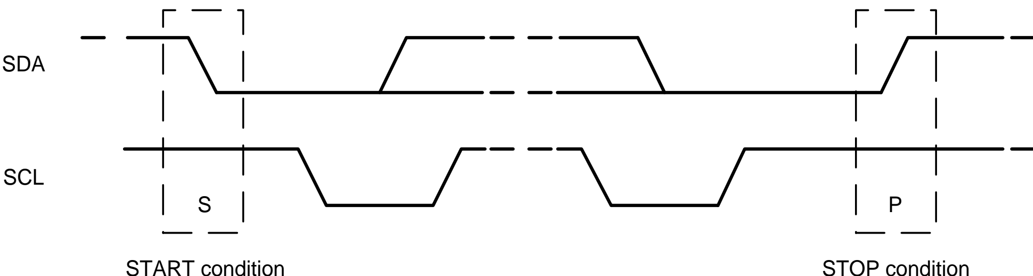


Figure 9 START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

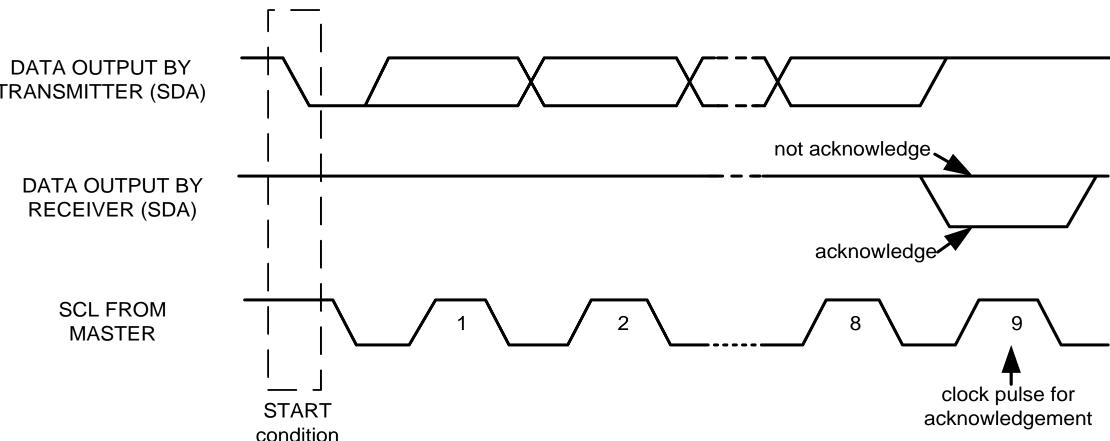


Figure 10 Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

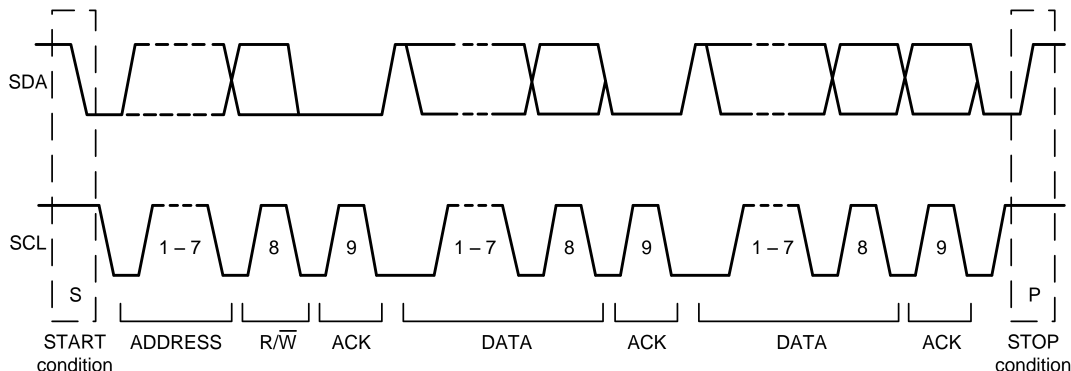


Figure 11 Complete I²C Data Transfer

To write the internal ITG-3400 registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ITG-3400 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ITG-3400 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ITG-3400 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ITG-3400 registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ITG-3400, the master transmits a start signal followed by the slave address and read bit. As a result, the ITG-3400 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

6.4 I²C Terms

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	ITG-3400 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 13 I²C Terms

6.5 SPI Interface

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The ITG-3400 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO) and the Serial Data Input (SDI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 1MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

SPI Address format

MSB							LSB
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

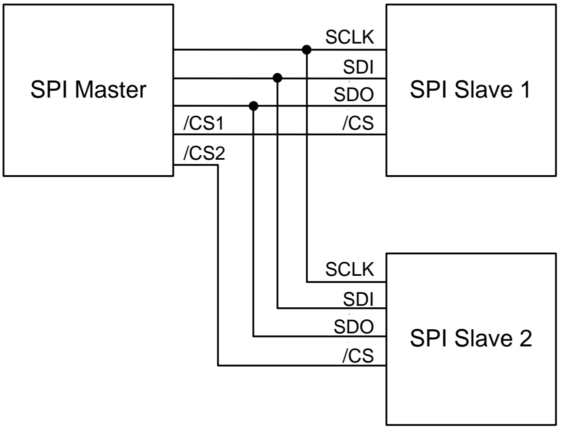


Figure 12 Typical SPI Master / Slave Configuration

7 Serial Interface Considerations

7.1 ITG-3400 Supported Interfaces

The ITG-3400 supports I^{2}C communications on its serial interface.

The ITG-3400's I/O logic levels are set to be VDDIO.

The figure below depicts a sample circuit of ITG-3400. It shows the relevant logic levels and voltage connections.

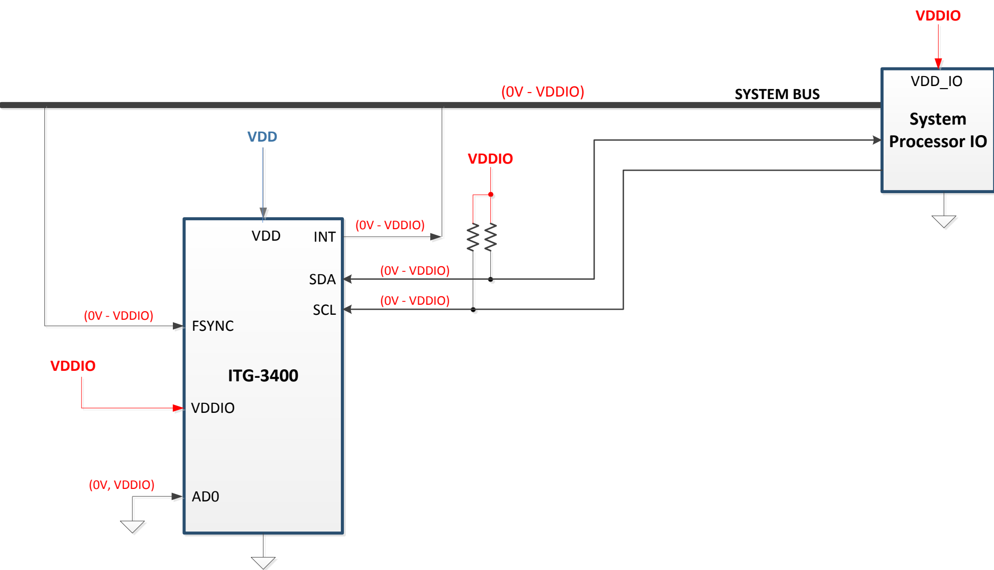


Figure 13 I/O Levels and Connections

8 Assembly

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in QFN package.

8.1 Orientation of Axes

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

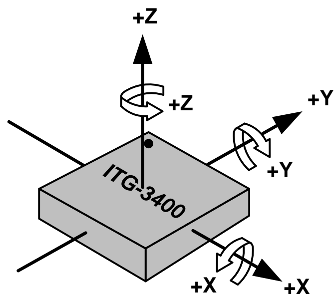
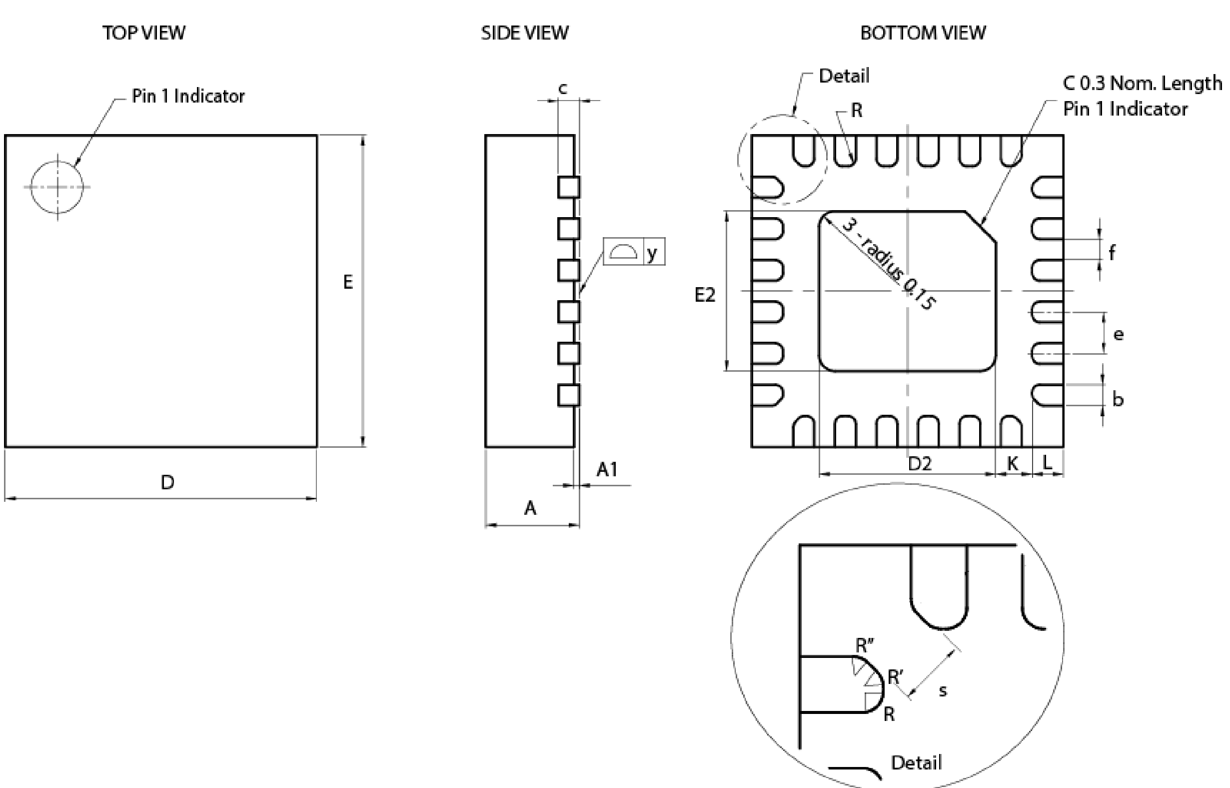


Figure 14 Orientation of Axes of Sensitivity and Polarity of Rotation

8.2 Package Dimensions

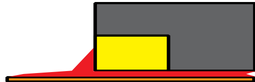
24 Lead QFN (3x3x0.9) mm NiPdAu Lead-frame finish



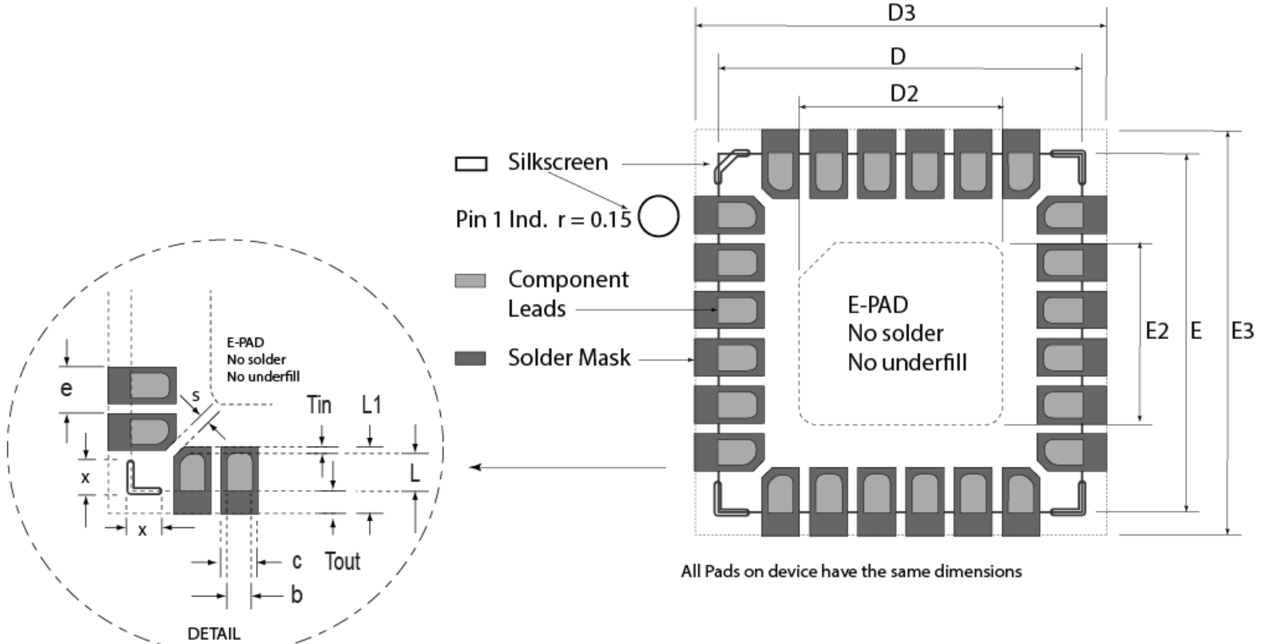
SYMBOLS	DESCRIPTION	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
A	Package thickness	0.85	0.90	0.95
A1	Lead finger (pad) seating height	0.00	0.02	0.05
b	Lead finger (pad) width	0.15	0.20	0.25
c	Lead frame (pad) height	---	0.20 REF	---
D	Package width	2.90	3.00	3.10
D2	Exposed pad width	1.65	1.70	1.75
E	Package length	2.90	3.00	3.10
E2	Exposed pad length	1.49	1.54	1.59
e	Lead finger-finger (pad-pad) pitch	---	0.40	---
f (e-b)	Lead-lead (Pad-Pad) space	0.15	0.20	0.25
K	Lead (pad) to Exposed Pad Space	---	0.35 REF	---
L	Lead (pad) length	0.25	0.30	0.35
R	Lead (pad) corner radius	0.075	REF	---
R'	Corner lead (pad) outer radius	0.10	0.11	0.12
R''	Corner lead (pad) inner radius	0.10	0.11	0.12
s	Corner lead-lead (pad-pad) spacing	---	0.25 REF	---
y	Lead conformality	0.00	---	0.075

8.3 PCB Design Guidelines

The PCB Diagram using a JEDEC type extension with solder rising on the outer edge is shown below. The PCB Dimensions Table shows pad sizing (nominal dimensions) recommended for the ITG-3400 product.



JEDEC type extension with solder rising on outer edge



SYMBOLS	DIMENSIONS IN MILLIMETERS	NOM
	Nominal Package I/O Pad (Land) Dimensions	
e	Lead (pad) pitch, land pitch	0.40
b	Lead (pad) width	0.20
L	Lead (pad) length	0.30
D	Package width	3.00
E	Package length	3.00
D2	Exposed pad finger width	1.70
E2	Exposed pad finger length	1.54
	I/O Land Design Dimensions (Guidelines)	
D3	I/O land finger extent width	3.80
E3	I/O land finger extent length	3.80
c	Land width	0.30
Tout	Outward extension (land beyond pad)	0.40
Tin	Inward extension (land beyond pad)	0.05
L1	Land length	0.70
s	Corner land spacing	0.15
x	Silkscreen corner marker length	0.30

PCB Dimensions Table (for PCB Lay-out Diagram)

Note: The symbols used in the two tables above do not necessarily refer to the same physical dimension. For example the symbols “c” and “s” represent different parameters in the two tables.

8.4 Assembly Precautions

8.4.1 Gyroscope Surface Mount Guidelines

InvenSense MEMS Gyros sense rate of rotation. In addition, gyroscopes sense mechanical stress coming from the printed circuit board (PCB). This PCB stress can be minimized by adhering to certain design rules:

When using MEMS gyroscope components in plastic packages, PCB mounting and assembly can cause package stress. This package stress in turn can affect the output offset and its value over a wide range of temperatures. This stress is caused by the mismatch between the Coefficient of Linear Thermal Expansion (CTE) of the package material and the PCB. Care must be taken to avoid package stress due to mounting.

Traces connected to pads should be as symmetric as possible. Maximizing symmetry and balance for pad connection will help component self alignment and will lead to better control of solder paste reduction after reflow.

Any material used in the surface mount assembly process of the MEMS gyroscope should be free of restricted RoHS elements or compounds. Pb-free solders should be used for assembly.

8.4.2 Exposed Die Pad Precautions

The ITG-3400 has very low active and standby current consumption. There is no electrical connection between the exposed die pad and the internal CMOS circuits. The exposed die pad is not required for heat-sinking, and should not be soldered to the PCB. Underfill is also not recommended. Soldering or adding underfill to the e-pad can induce performance changes due to package thermo-mechanical stress.

8.4.3 Trace Routing

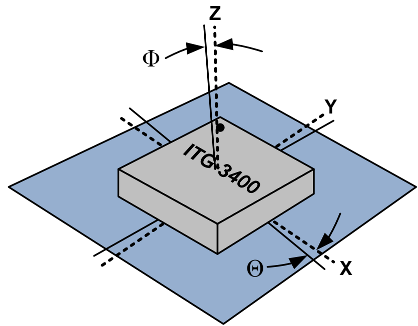
Routing traces or vias under the gyro package such that they run under the exposed die pad is prohibited. Routed active signals may harmonically couple with the gyro MEMS devices, compromising gyro response. The gyro drive frequency is 25 – 29 KHz. To avoid harmonic coupling don't route active signals in non-shielded signal planes directly below, or above the gyro package. Note: For best performance, design a ground plane under the e-pad to reduce PCB signal noise from the board on which the gyro device is mounted. If the gyro device is stacked under another PCB board, design a ground plane directly above the gyro device to shield active signals from the PCB board mounted above.

8.4.4 Component Placement

Do not place large insertion components such as keyboard or similar buttons, connectors, or shielding boxes at a distance of less than 6 mm from the MEMS gyro. Maintain generally accepted industry design practices for component placement near the ITG-3400 to prevent noise coupling and thermo-mechanical stress.

8.4.5 PCB Mounting and Cross-Axis Sensitivity

Orientation errors of the gyroscope mounted to the printed circuit board can cause cross-axis sensitivity in which one gyro sense axis responds to rotation about an orthogonal axis. For example, the X-gyro sense axis may respond to rotation about the Y or Z axes. The orientation mounting errors are illustrated in the figure below.



Package Gyro & Accel Axes (– – –) Relative to PCB Axes (——) with Orientation Errors (Θ and Φ)

The table below shows the cross-axis sensitivity as a percentage of the gyroscope's sensitivity for a given orientation error, respectively.

Cross-Axis Sensitivity vs. Orientation Error

Orientation Error (θ or Φ)	Cross-Axis Sensitivity (sinθ or sinΦ)
0º	0%
0.5º	0.87%
1º	1.75%

The specifications for cross-axis sensitivity in Section 3.1 includes the effect of the die orientation error with respect to the package.

8.4.6 MEMS Handling Instructions

MEMS (Micro Electro-Mechanical Systems) are a time-proven, robust technology used in hundreds of millions of consumer, automotive and industrial products. MEMS devices consist of microscopic moving mechanical structures. They differ from conventional IC products, even though they can be found in similar packages. Therefore, MEMS devices require different handling precautions than conventional ICs prior to mounting onto printed circuit boards (PCBs).

The ITG-3400 has been qualified to a shock tolerance of 10,000*g*. InvenSense packages its gyroscopes as it deems proper for protection against normal handling and shipping. It recommends the following handling precautions to prevent potential damage.

- Do not drop individually packaged gyroscopes, or trays of gyroscopes onto hard surfaces. Components placed in trays could be subject to *g*-forces in excess of 10,000*g* if dropped.
- Printed circuit boards that incorporate mounted gyroscopes should not be separated by manually snapping apart. This could also create *g*-forces in excess of 10,000*g.*
- Do not clean MEMS gyroscopes in ultrasonic baths. Ultrasonic baths can induce MEMS damage if the bath energy causes excessive drive motion through resonant frequency coupling.

8.4.7 ESD Considerations

Establish and use ESD-safe handling precautions when unpacking and handling ESD-sensitive devices.

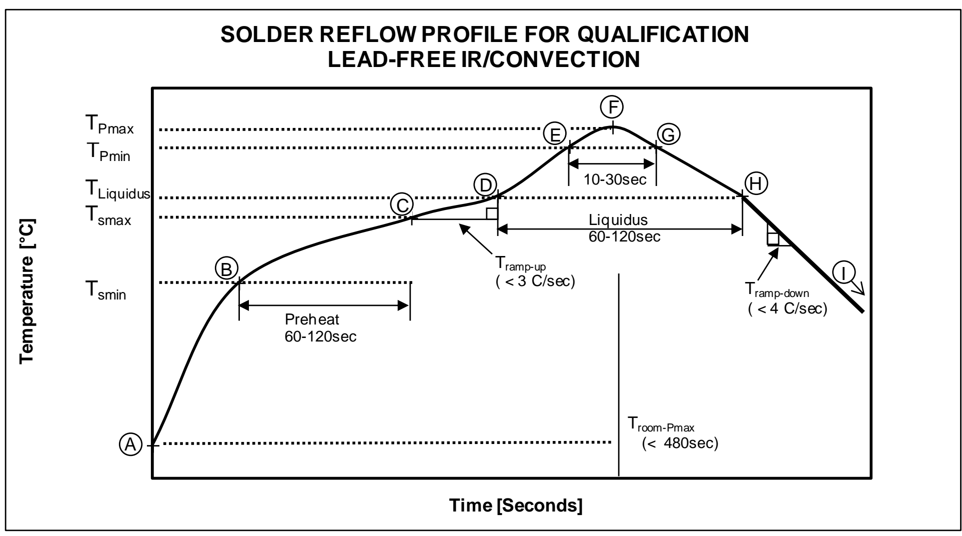
- Store ESD sensitive devices in ESD safe containers until ready for use, such as the original moisture sealed bags, until ready for assembly.
- Restrict all device handling to ESD protected work areas that measure less than 200V static charge. Ensure that all workstations and personnel are properly grounded to prevent ESD.

8.4.8 Reflow Specification

Qualification Reflow: The ITG-3400 was qualified in accordance with IPC/JEDEC J-STD-020D.1. This standard classifies proper packaging, storage and handling in order to avoid subsequent thermal and mechanical damage during the solder reflow attachment phase of PCB assembly.

The qualification preconditioning process specifies a sequence consisting of a bake cycle, a moisture soak cycle (in a temperature humidity oven), and three consecutive solder reflow cycles, followed by functional device testing.

The peak solder reflow classification temperature requirement for package qualification is (260 +5/-0°C) for lead-free soldering of components measuring less than 1.6 mm in thickness. The qualification profile and a table explaining the set-points are shown below:



Temperature Set Points Corresponding to Reflow Profile Above

Step	Setting	CONSTRAINTS		
		Temp (°C)	Time (sec)	Max. Rate (°C/sec)
A	T_{room}	25		
B	T_{Smin}	150		
C	T_{Smax}	200	$60 < t_{BC} < 120$	
D	$T_{Liquidus}$	217		$r_{(TLiquidus-TPmax)} < 3$
E	T_{Pmin} [255°C, 260°C]	255		$r_{(TLiquidus-TPmax)} < 3$
F	T_{Pmax} [260°C, 265°C]	260	$t_{AF} < 480$	$r_{(TLiquidus-TPmax)} < 3$
G	T_{Pmin} [255°C, 260°C]	255	$10 < t_{EG} < 30$	$r_{(TPmax-TLiquidus)} < 4$
H	$T_{Liquidus}$	217	$60 < t_{DH} < 120$	
I	T_{room}	25		

Notes: Customers must never exceed the Classification temperature (T_{Pmax} = 260°C).
All temperatures refer to the topside of the QFN package, as measured on the package body surface.

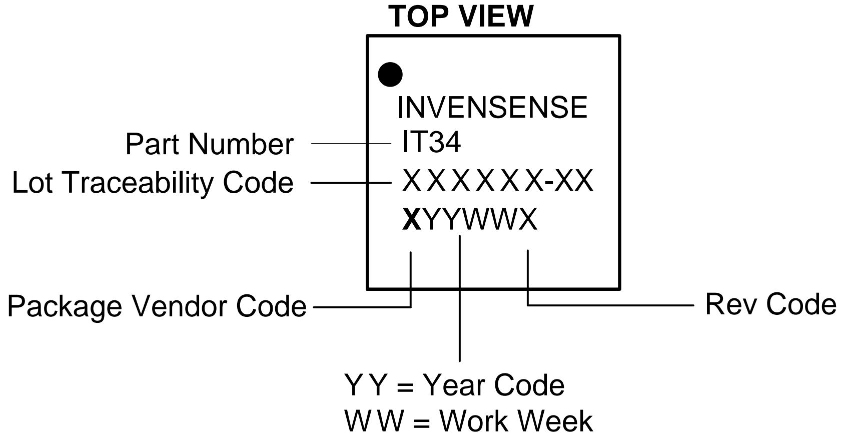
Production Reflow: Check the recommendations of your solder manufacturer. For optimum results, use lead-free solders that have lower specified temperature profiles (Tp_{max} ~ 235°C). Also use lower ramp-up and ramp-down rates than those used in the qualification profile. Never exceed the maximum conditions that we used for qualification, as these represent the maximum tolerable ratings for the device.

8.5 Storage Specifications

The storage specification of the ITG-3400 conforms to IPC/JEDEC J-STD-020D.1 Moisture Sensitivity Level (MSL) 3.

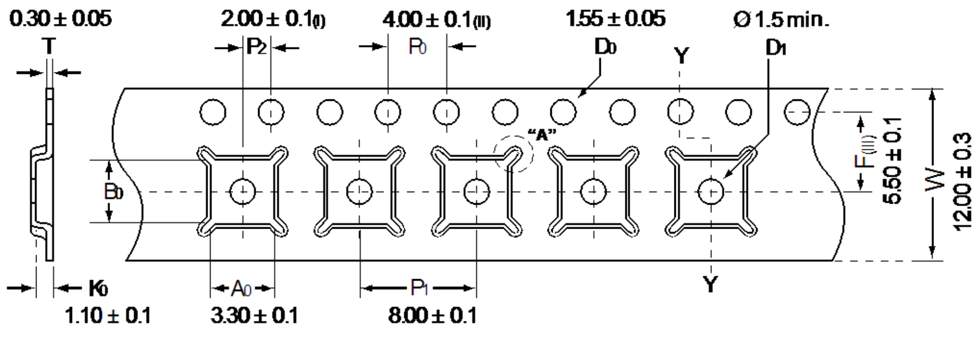
Calculated shelf-life in moisture-sealed bag	12 months -- Storage conditions: <40°C and <90% RH
After opening moisture-sealed bag	168 hours -- Storage conditions: ambient ≤30°C at 60%RH

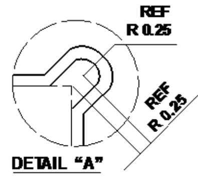
8.6 Package Marking Specification



Package Marking Specification

8.7 Tape & Reel Specification

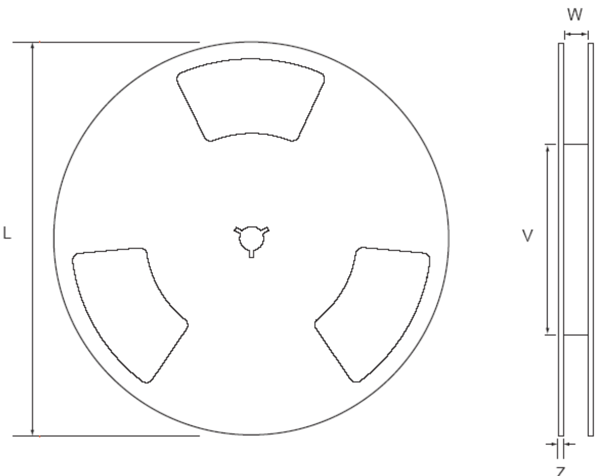




(I) Measured from centerline of sprocket hole to centerline of pocket
(II) Cummulative tolerance of 10 sprocket holes is ± 0.20
(III) Measured from centerline of sprocket hole to centerline of pocket

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

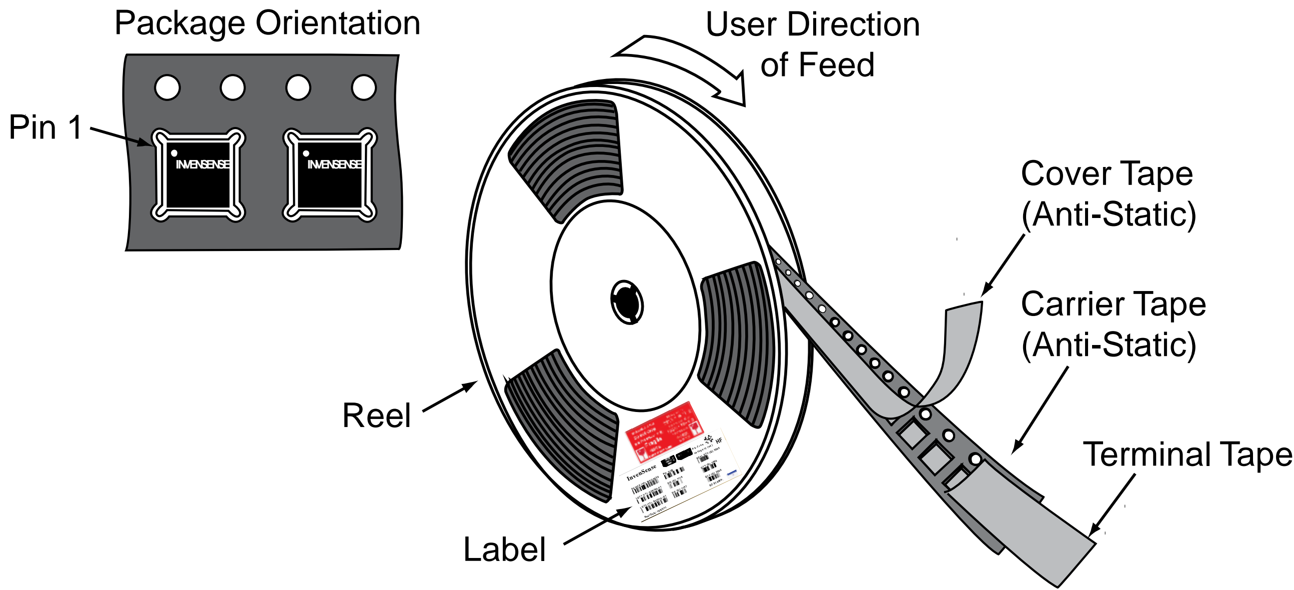
Tape Dimensions



Reel Outline Drawing

Reel Dimensions and Package Size

PACKAGE SIZE	REEL (mm)			
	L	V	W	Z
3x3	330	102	12.8	2.3



Tape and Reel Specification

Reel Specifications

Quantity Per Reel	5,000
Reels per Box	1
Boxes Per Carton (max)	5
Pcs/Carton (max)	25,000

8.8 Label

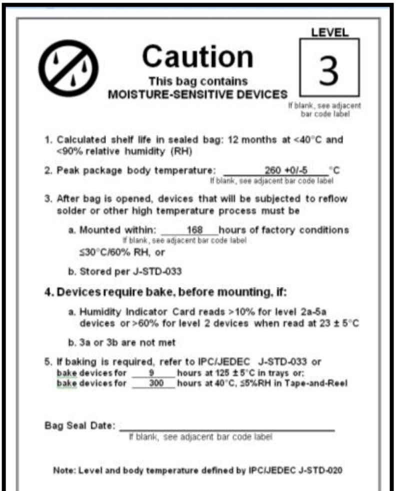
Barcode Label

Location of Label on Reel

8.9 Packaging

REEL – with Barcode & Caution labels

Vacuum-Sealed Moisture Barrier Bag with ESD, MSL3, Caution, and Barcode Labels



MSL3 Label

Caution Label

ESD Label

Inner Bubble Wrap

Pizza Box

Pizza Boxes Placed in Foam-Lined Shipper Box

Outer Shipper Label

8.10 Representative Shipping Carton Label

INV. NO:

111013-99

From:

InvenSense Taiwan, Ltd.
1F, 9 Prosperity 1st Road, Hsinchu Science Park, HsinChu City, 30078, Taiwan
TEL: +886 3 6686999
FAX: +886 3 6686777

Ship To:

Customer Name
Street Address
City, State, Country
ZIP
Attn: Buyer Name
Phone: Buyer Phone Number

SUPP PROD ID: **ITG-3400**

LOT#: Q2R994-F1		LOT#:	
QTY: 5615		QTY:	0
LOT#: Q3X785-G1		LOT#:	
QTY: 4385		QTY:	0
LOT#: Q3Y196-02		LOT#:	
QTY: 5000		QTY:	0
LOT#:		LOT#:	
QTY:	0	QTY:	0

Total Quantity/Carton	Weight: (KG)
15000	4.05

Pb-free Pb

Shipping Carton: 1 OF 3

Category (e4) HF

MSL3

Underfill

QC10

9 Environmental Compliance

The ITG-3400 is RoHS and Green compliant.

The ITG-3400 is in full environmental compliance as evidenced in report HS-ITG-3400A, Materials Declaration Data Sheet.

Environmental Declaration Disclaimer:

InvenSense believes this environmental information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

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