Piezo-Electric Actuator Controller

Preliminary Technical Data

AD5801

FEATURES

Two Efficient Class D-type Amplifiers
Six Integrated Pattern Drivers
Programmable Output Drive Patterns
12-bit ADC Voltage or Current Sensing for Position Feedback
Programmable Shutter Control
On board temperature sensing
Optional Off-board Temperature Sensing
32-lead 5mm X 5mm LFCSP Package

APPLICATIONS

Camera Phones
Piezoelectric Positioning
Piezo Actuators
Lens Auto focus
Lens Zoom
Iris/Exposure
NDF Neutral density Filter
Shutter
Camera Phone
Camera Enabled PDA
Camera/Image Modules
Digital Still Camera DSC
Web Cameras
Security Cameras
Digital Camcorders

GENERAL DESCRIPTION

The AD5801 is a high efficiency ultrasonic motor controller with two Class D-type output drivers. These Class D-type drivers can be used independently or configured as an H-bridge driver, and have full pattern programmability. There are also six integrated drivers which can be operated independently and have programmable output patterns. The AD5801 also has integrated drivers which are programmable from 130mA to 200mA, and may be used for a combination of Shutter and NDF/IRIS control.

The operation modes of the drivers are invoked by the AD5801 using an I2C compatible interface.

The I2C address for the AD5801 is TBD.

FUNCTIONAL BLOCK DIAGRAM

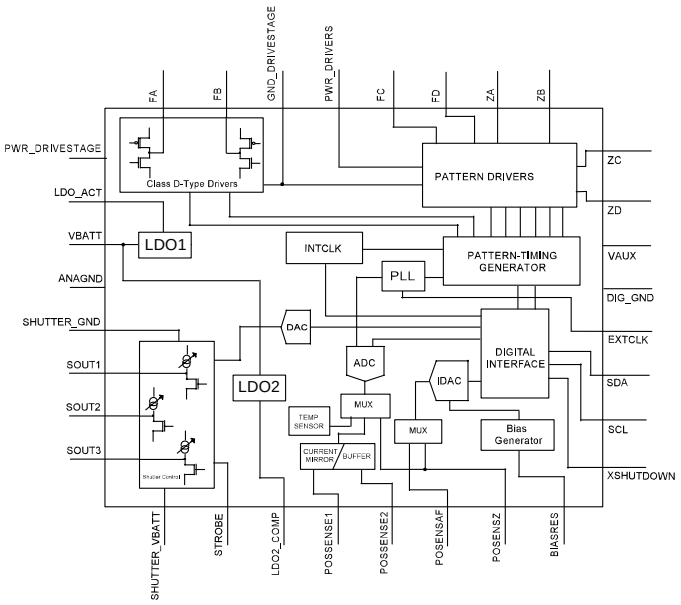

Figure 1. AD5801 Functional Block Diagram.

PRODUCT HIGHLIGHTS

1. Eight independent output drivers.

2. Available in 32-Lead (5mm X 5mm) LFCSP package.

3. Multiplexed input 12-bit resolution ADC for voltage or current measuring.

4. Dual temperature sensing feature, Integrated AD5801 temperature sensing and optional external temperature reading of position sensor.

6. Low Ron in Auto Focus driver switches, 0.5 Ω max.

7. Fully guaranteed in the 2.8 V to 4.5 V supply range.

8. Integrated Shutter/Iris/NDF optional controls

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REVISION HISTORY

June/05—Revision 0.9

SPECIFICATIONS[1]

VCC = 2.8V to4.5 V, VCC>VDD, GND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
Driver Stage[2]	FA, FB					
Switch On Resistance	Ron					
PMOS (high switch)					0.5	Ω
NMOS (low switch)					0.5	Ω
Driver Stage[2]	FC, FD, ZA,-ZD					
Drive Current Capability			8			mA
Output High Voltage	V_{OH}		2.4			V
Output Low Voltage	V_{OL}				0.8	V
Analog to Digial Converter Position Sensing	ADC					
Resolution					12	LSB
INL		12-bit LSB		1		LSB
DNL		12-bit LSB		1		LSB
Conversion Time[3]					160	µs
Input Voltage Range in Current Sense Mode		Max Voltage at SENSE			1.5	V
Current Range		Source Current from SENSE	0		300	µA
Input Voltage Range in Voltage Sense Mode			0		TBD	V
Integrated Temperature Sensor						
Resolution				2		°C
Range			-30		70	°C
Accuracy				+/-4		°C
Conversion Time				320		µs
External Temperature Sensor						
Resolution						°C
Range			-30		70	°C
Input Voltage Range						V
Conversion Time[3]				160		µs
Input Voltage Range		Input Voltage at POSSENS1			1.5	V

BIAS	BIASRES					
Bias reference Voltage				1.275		V
Output Current range		Current to POSSENSAF-Z	4	10	19	mA
Output Current Accuracy				2.5		%
External Resistor[4]	R_{term}			5.1		k Ω
External Resistor Tolerance			-1		1	%
Shutter Controls	SOUT1-SOUT3					
Output Current Range			130		200	mA
Accuracy[5]					±5	%
Step Size				10		mA
Shutter Strobe	STROBE					
Strobe Time			5		35	ms
Input High Voltage	V_{IH}		1.17			V
Input Low Voltage	V_{IL}				0.63	V
Low Drop Out Regulator[6]	LDO_ACT					
Programmable Output Voltage Range			2.8		3.3	V
Output Current Drive Capability					200	mA
Accuracy[5]					±3	%
Programmable Output Voltage Level 1				2.8		V
Programmable Output Voltage Level 2				2.9		V
Programmable Output Voltage Level 3				3.0		V
Programmable Output Voltage Level 4				3.3		V
LDO Compensation Capacitor			10		20	µF
External Clock[7]	EXTCLK					
Clock Frequency Range			4.8		19.44	MHz
Internal Clock[7]	INTCLK					
Clock Frequency					19.44	MHz
I2C Interface[8]						
SDA, SCL Input High Voltage	V_{IH}		1.3	1.8	VAUX	V
SDA, SCL Input Low Voltage	V_{IL}		0		0.4	V
Glitch Rejection					50	ns
ShutDown/Standby/RESET[9]	XSHUTDOWN					
XSD High Level Input voltage			1.17			V
XSD Low Level Input voltage					0.63	V
Minimum Valid Shutdown period			100			ns
Min Time Between Successive XSD Pulses				TBD		ns
Power Supply						
VBATT	Battery Supply		2.8		4.5	V
Currrent Consumption in Active Mode					TBD	mA
Current on VBATT					TBD	mA
VAUX	Digital Supply		2.5		VBATT	V
Current on VAUX					TBD	µA
PWR_DRIVESTAGE	FA-FB Drivers		2.5		5	V
SHUTTER_VBATT	Shutter Supply		2.5		5	V
PWR_DRIVERS	FC, FD, ZA-ZD Drivers		2.5		5	V

[1] Temperature range is as follows: B Version: –40°C to +70°C
[1] See Figure 3 for timing programmability details.
[3] The conversion time of 160µs is due to averaging of four measurements taken by the ADC,. The averaging feature can be disabled and the conversion time is then 40µs.
[4] An external precision resistor is required to establish bias currents and voltages.
[5] This is the accuracy over the entire temperature range.

[6] A minimum 10µF capacitor is required for LDO_ACT. A 4.7 µF is required at the pin LDO2_COMP.
[7] The AD5801 can be programmed for use with an external or internal clock.
[8] See Table 3 and Figure 2 for I2C timing specifications.
[9] Bringing XSHUTDOWN low disables the I2C interface, on a low to high transition there is a reset on the AD5801.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameters	Rating
VCC to GND	TBD
Digital Inputs	−0.3 V to (VDD + 0.3 V)
Voltage on Analog Inputs	−0.3 V to (VCC + 0.3 V)
DRPWR pins to GND	-0.3V to TBD
FOUT pins to GND	-0.3V to TBD
ZOUT pins to GND	-0.3V to TBD
Maximum Voltage between GND pins[1]	±0.3V
Operating Temperature Range	−30°C to +70°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
32-Lead LFCSP	
θ_{JA} Thermal Impedance	32°C/W
Lead Temperature, Soldering (10 s)	300°C

[1]This is the maximum allowable voltage between the various GND pins on the AD5801.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 3. I²C Serial Interface

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Description
F_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU, DAT}$, data setup time
t_6[2]	0.9	µs max	$t_{HD, DAT}$ data hold time
	0	µs min	$t_{HD, DAT}$ data hold time
t_7	0.6	µs min	$t_{SU, STA}$ setup time for repeated start
t_8	0.6	µs min	$t_{SU, STO}$ stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop and a start condition
t_{10}	300	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}	300	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS compatible)
	300	ns max	t_F, fall time of SCL and SDA when receiving
	20 + 0.1 C_B	ns min	t_F, fall time of SCL and SDA when transmitting
C_B[3]	400	pF max	Capacitive load for each bus line

[1] See 2.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} MIN of the SCL signal) to bridge the undefined region of SCL's falling edge.
[3] C_B is the total capacitance of one bus line in pF; t_R and t_F measured between 0.3 V_{DD} and 0.7 V_{DD}.

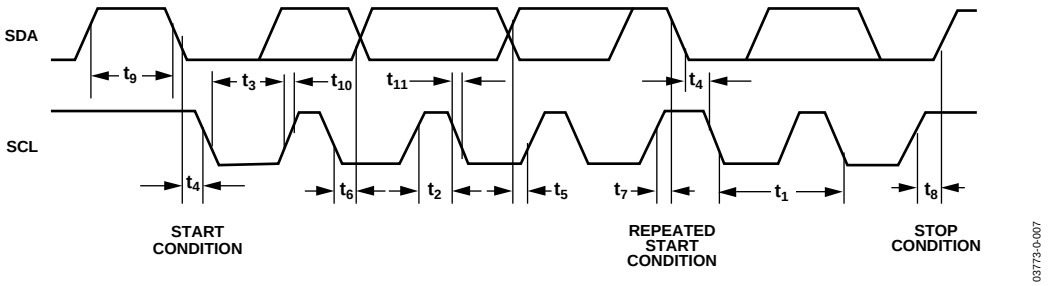

Figure2.. I²C Interface Timing Diagram

Block Diagram

Table 3. Pin Function Descriptions

Pin. No.	Mnemonic	Description
	SHUTTER_VBATT	Power Connection for the Shutter Drivers SOUT1-SOUT3, to be connected to VBATT
	STROBE	Duration of the STROBE signal width sets the duration of current pulsed from SOUT1 to SOUT3. The STROBE function can be disabled and the pulse duration can be programmed over the I"C interface if required.
	LDO2_COMP	This is the compensation pin for the internal Low Drop Out Regulator LDO2. A 4.7µF capacitor should be connected between LDO2_COMP and ANAGND.
	POSSENSE1	Input to ADC, the AD5801 can be used to measure current in an opto-reflective position feedback scheme,or voltage from a Hall sensor or some other voltage output sensor, to determine lens postion.
	POSSENSE2	Input to ADC, the AD5801 can be used to measure current in an opto-reflective position feedback scheme,or voltage from a Hall sensor or some other voltage output sensor, to determine lens postion.
	POSENSAF	Programmable current output.
	POSENSZ	Programmable current output.
	BIASTRES	Connected to external resistor for bias current generator
	XSHUTDOWND	Asynchonous system reset signal
	SCL	I2C Interface Signal
	SDA	I2C Interface Signal
	EXTCLK	Optional External Reference Clock Signal
	DIG_GND	Digital Ground
	VAUX	Digital Supply
	ZD	Pattern programmable output driver which can be used for zoom control.
	ZC	Pattern programmable output driver which can be used for zoom control.
	ZB	Pattern programmable output driver which can be used for zoom control.
	ZA	Pattern programmable output driver which can be used for zoom control.
	FD	Pattern programmable output driver which can be used for auto focus control.
	FC	Pattern programmable output driver which can be used for auto focus control.
	PWR_DRIVERS	Power Supply pin for pattern programmable putput drivers FC, FD, ZA, ZB, ZC, and ZD. This pin can be connected to LDO_ACT or a supply of 5V max.
	GND_DRIVESTAGE	Ground for Focus Actuator/Motor Drivers FA and FB and for pattern drivers FC, FD, ZA, ZB, ZC, and ZD.
	FB	Pattern programmable low Ronoutput driver which can be used for driving auto focus piezo actuator directly.
	FA	Pattern programmable low Ronoutput driver which can be used for driving auto focus piezo actuator directly.
	PWR_DRIVESTAGE	Supply for low Ron Drivers FA and FB, can be connected to LDO_ACT or a supply of 5V max.
	LDO_ACT	Output of integrated Low Drop Out Regulator. A 10µF decoupling capacitor should be connected between LDO_ACT and ANAGND.
	VBATT	Battery supply connection.
	ANAGND	Analog Ground connection.
	SHUTTER_GND	Ground connection for Shutter Drivers SOUT1-SOUT3, this pins should be connected to ANAGND and special care should be exercised to ensure that the ground return path from this pin to ANAGND is kept to a minimum impedance.
	SOUT1	Output for Shutter/Iris/NDF/Lens Cover Drive and control.
	SOUT2	Output for Shutter/Iris/NDF/Lens Cover Drive and control.
	SOUT3	Output for Shutter/Iris/NDF/Lens Cover Drive and control.

General Description

The AD5801 is a high efficiency ultrasonic motor controller with two Class D-type output drivers. These Class D-type drivers can be used independently or configured as an H-bridge driver, and have full pattern programmability. There are also six integrated drivers which can be operated independently and have programmable output patterns. The AD5801 also has integrated drivers which are programmable from 60mA to 200mA, and may be used for a combination of Shutter and NDF/IRIS control.

The operation modes of the drivers are invoked by the AD5801 using an I2C compatible interface.

Driver Stage for Auto Focus

Channel FA sad FB are Class D-type outputs with an on-resistance, Ron, of 0.5Ω maximum over temperature. These outputs have been integrated to eliminate the need to use external FET drivers for the Auto Focus function and can be configured as a PWM source.

The driving frequency of outputs FA and FB is configured in the Registers PWUNIT and PWMPERIOD. The PWUNIT defines the basic time interval from when the counters can derive a count, and is used to set the divide factor used to divide the clock frequency of the master clock derived from the integrated PLL in the AD5801, or the clock applied to EXTCLK. The effective phase difference in the outputs FA and FB can be programmed in the PWMAFATx and PWMAFBTx registers, and the waveforms can be programmed with varying or constant duty cycles (See Figure 3).

The PWM patterns from Channels FA and FA are enabled in the PWMENABLE and PWMPOLARITY Registers. The PWMENABLE register allows the user to enable the drivers channels required, the PWMPOLARITY Register is used to set the polarity of the drive patterns when they are initiated. When the outputs are disabled they can be set configured in a High Impedance, or High or Low state.

To move the motor in reverse the user has the choice of either setting new values to the PWMAFATx and PWMAFBTx registers or setting a direction bit in the ACTIVE Register which interchanges the timing values between the driver outputs FA and FB. The actual duration of the drive operation is defined in the AFSTEPS Register, this allows the user to enter the number of PWMPERIODS required for one move of the lens.

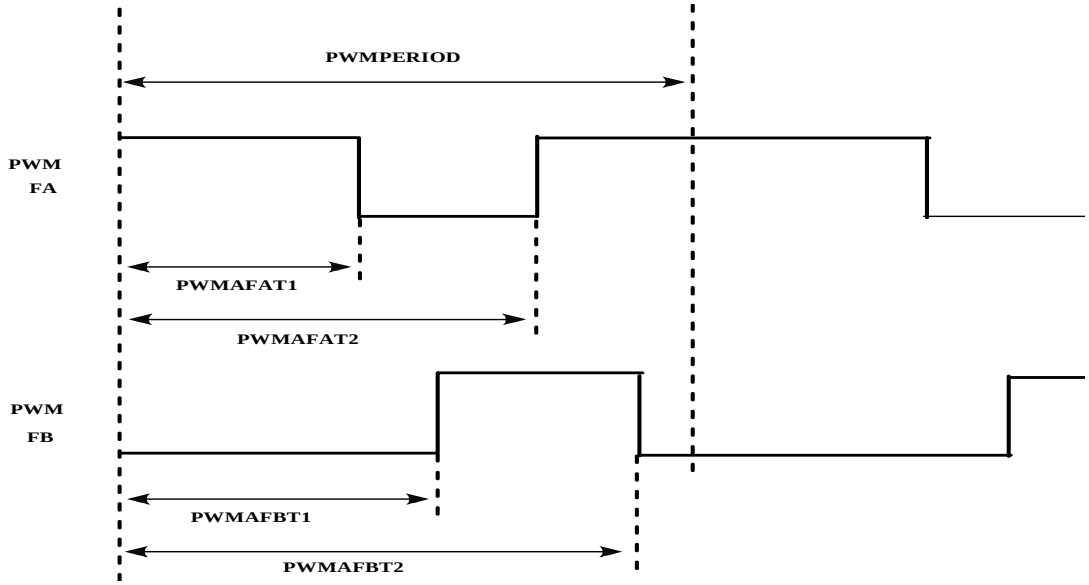

Figure 3. Timing Diagram for Class D-type Driver FA and FB.

Driver Stages FC – ZD

Drivers FC, FD, and ZA – ZD are independent driver channels capable of driving 8mA. These channels can be configured as PWM drivers and used to drive external FETs or Bridges for Zoom control, or for other timing functions.

As with Drivers FA and FB the driving frequency is programmed in the PWMUNIT and PWMPERIOD Registers, and the programmed PWM patterns are enabled by the PWMENABLE and PWMPOLARITY Registers. These driver outputs have four registers (PWMAFCTx, PWMAFDTx, PWMAZATx – PWMAZDTx) which allow the user to

programme up to four transitions within the time set in the PWMPERIOD Register (See Figure 4 for typical timing diagrams, with outputs FC and FD as an example).

The number of PWMPERIOD periods is again set in the AFSTEPS and ZSTEPS Registers. When the outputs are disabled they can be set configured in a High Impedance, or High or Low state.

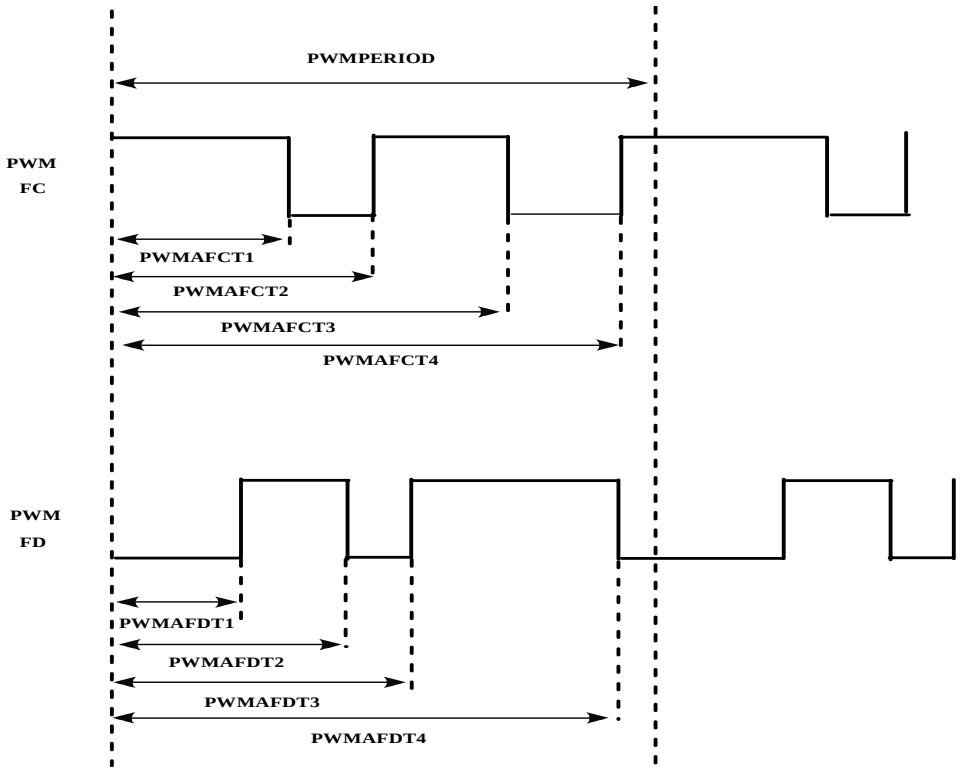

Figure 4. Timing Diagram for PWM Drivers.

Temperature Compensation of Drive Patterns

Because of the high temperature coefficients associated with piezo elements fine tuning of the drive pattern and drive frequencies are required to ensure the device operates over its intended temperature range.

In all drive modes it is possible to specify different timing parameters for three different temperature areas.. If Temperature compensation mode is selected by programming the appropriate bit to the DRIVEMODE register, the PTAT temperature is checked at the beginning of the new ACTIVE move command and depending on the Temperature recorded the timing data for the move is read from the appropriate timing register, HOT, COLD or NOMINAL.

The timing registers for all the driver outputs FA-ZD are duplicated for Hot and Cold operation and the relevant timing information for the Hot and Cold bands of operation are programmed in these Registers.

PWM Slope Mode

A piezo element is a block of ceramic material and is basically a moving capacitor. The electrical energy of the drive patterns are converted into mechanical reaction energy inside the piezo element, and the resulting deformation in the material is used to produce forces to move the lens assembly in an optical module.

Driving a capacitive element with digital patterns may produce large surges in power because power is only consumed during transients and the impedance of the piezo motor can be very small on the rising and falling edges of a pulse.

TheAD5801 has an alternative driving scheme called the PWM Slope Mode which can be employed on Channels FA and FB. The Slope Mode allows the user to control the rise and fall times of the drive waveform by taking advantage of the energy storage properties of the series inductor and the resultant LC

filtering when combined with the piezo element. The AD5801 Slope Mode effectively allows the user to control the rise and fall times of the drive waveform by using predetermined PWM patterns and driving these patterns into an LC load.

The AD5801 have several default patterns, which after filtering by the addition of a suitable inductor in series with the capacitance of the piezo load, produces a rhombic or triangular waveform at the piezo element. The principle on which this mode works is that the pattern density increases linearly and then decreases linearly from:

$$\frac{1}{X} \rightarrow \frac{X}{X}$$

Where: *X* is 8, 9, 10 or 11

The default patterns are register selected and allow the user to effectively control the rise and fall times of the waveforms across the piezo motor. The AD5801 PWM Slope Mode pattern causes the waveform across the piezo element to ramp from GND to an output high level defined by the supply voltage connected to the PWR_DRIVESTAGE pin. The period set in the PWMPERIOD register defines the high and low time within one period. For example:

if selected X value = 10

and PWMPERIOD = 254

Then the number of counter periods, as defined in the PWNUNIT register that are on the top and bottom of the resultant waveform are calculated with the following Formula:

$$\text{Number of Periods} = \frac{PWMPERIOD - \left[X^2 \times 2\right]}{2}$$

In the case where *X* = 10

$$\text{Number of Periods} = \frac{254 - \left[10^2 \times 2\right]}{2} = 26$$

So there are 26 counter periods on top and bottom of the resultant rhombic waveform. Figure 5 illustrates the AD5800 driving a default PWM Slope Mode pattern through a series inductor and into the piezo load, and the resultant waveforms.

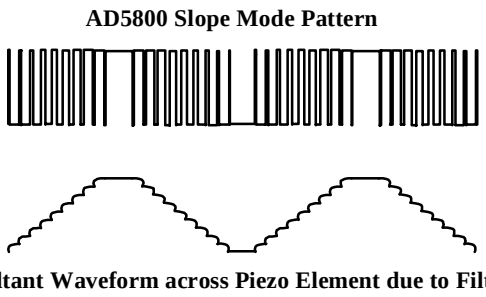

Figure 5. AD5801 Slope Mode Pattern and resulting filtered waveform across the piezo motor.

The primary advantage of using the AD5801 in Slope Mode is that the rise and fall times of the driving waveform are controlled, and therefore the power surges associated when driving the piezo element with a square wave at its resonant frequency are eliminated.

Clock Generation

The AD5801 offers the user the choice of two master clock sources, an internal clock generated from an integrated VCO, or an external clock applied through the EXCLK pin. The external reference clock is provided by the baseband processor in the host system, and can be either a DC coupled square wave or an AC coupled sine wave. In either case the clock may have been RC filtered. The clock may be either a free running system clock or dedicated camera module clock, which may be enabled and disabled by the host. The AD5801 has a highly accurate PLL based clock generator which accepts an accurate and stable multiple of the external clock (4.8MHz or 9.6MHz), and multiplies its frequency to the master clock of 19.44MHz required by the AD5801.

The AD5801 also has the option of using an integrated clock generator. The MCLKCONTROL Register allows the user to select either the external or integrated clock source, select. If an external clock is used then the MCLKCONTROL Register allows the user to set the AD5801 EXTCLK pin to accept an AC-coupled or DC-coupled clock, and also allows the user to select the master clock frequency supplied, or to bypass the PLL if the master clock is 19.44MHz. The internal clock is generated using a 2% accurate VCO.

ADC and Lens Position Sensing

The AD5801 has an integrated on board 12 bit ADC. The ADC contains an on-chip track and hold amplifier, a successive approximation A/D converter. Clocking for the A/D is provided using a divided down ratio of the integrated or host master reference clock.

A programmable safety interval is allowed to elapse before the actual position measurement is made by the ADC. This safety interval duration can be set in a register to be anything from zero to 1000µs. Four consecutive measurements from the lens position signal are made and their average saved to result registers. Each of the lens position measurement results are stored in two 8-bit registers because the ADC is a twelve-bit converter. It is possible to turn-off the averaging feature if required.

The ADC has the ability to accept either current or voltage inputs depending on the position sensing scheme used. A bit in the CONFIG register will set the AD5801 for current or voltage conversion. Figure 6 show a simplified diagram where the ADC measures the output of an optical reflective position sensor.

Depending on whether it is the auto focus lens position or Zoom position you are measuring the IDAC sources a current derived from an integrated Bias circuit and external precision resistor, BIASRES. The Bias circuit consists of bandgap voltage reference and current to voltage generator.

The current sourced is between 4mA and 19mA with 4-bit resolution. In the case of an auto focus lens position measurement the desired current is programmed to LED, D1. The incident light from D1 falls on the photosensitive device Q1 . The output of Q1 is connected to the POSSENSE1 pin and the current flowing in Q1 is then measured by the ADC, and there is a direct current to lens position relationship which indicates the position of the auto focus lens. Because the zoom lens position LED, D2, has no current flowing in it then there is no current flowing in the photosensitive device Q2, and only the position of the auto focus lens is detected and measured. The position sensing for the zoom lens works on exactly the same principles.

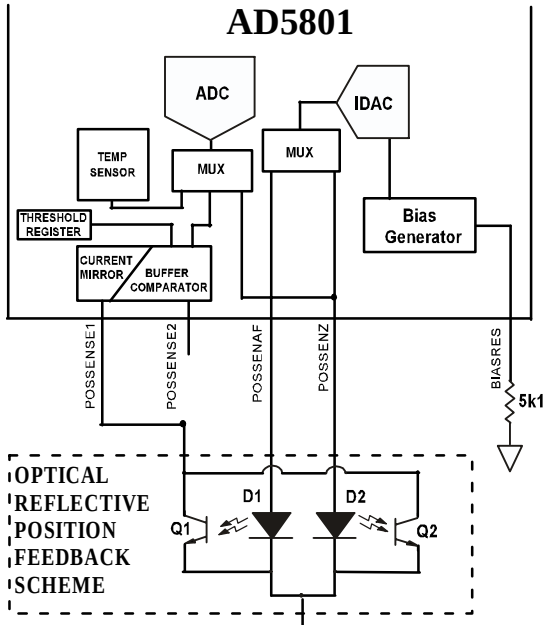

Figure 6. Lens position Sensing using an Optical Reflective Feedback Scheme.

Figure 7 shows the ADC configured to measure in voltage mode. The inputs POSSENSE1 and POSSENSE2 can be connected to the outputs of HALL sensors, or POSSENE1 can be tied to AGND and POSSENSE2 can be used to measure single ended voltages, The AD5801 also has an internal register which may be programmed with a required threshold value, and this value can then be compared to the Hall voltage or single-ended voltage input. The threshold voltage can be used to indicate the ret position of either lens. For example, if the user is driving the lens to the start position the output of the comparator disables the output drivers when the programmed threshold indicating the lens start position is reached. Only one position sense measurement is performed at a time. For a zoom lens position measurement current is source from the POSSENSEZ pin into the Zoom Hall Plate, and the resulting voltage from the output of the Hall sensor is connected through the POSSENSE1 and POSSENSE2 pins to the ADC. Given that only one Hall Sensor is active at one time it is possible to connect the outputs of both sensors together. For single-ended sensor outputs the output voltage is connected to POSSENSE2 and POSSENSE1 is connected to AGND.

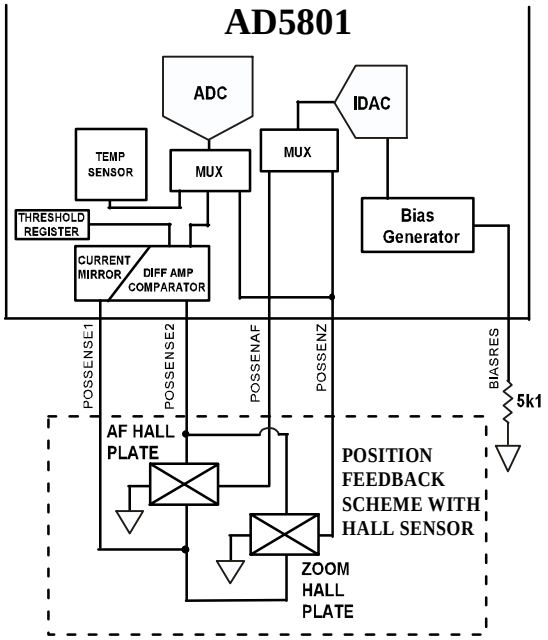

Figure 7. Lens Position Sensing using Hall Sensors.

Outline Package Dimensions