IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

In this document where the previous NXP references remain, please use the new links as shown below.

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Thank you for your cooperation and understanding,

WeEn Semiconductors

founded by NXP

BUJ103AD

Silicon diffused power transistor

Rev. 3 — 18 October 2016 Product data sheet

1. Product profile

1.1 General description

High-voltage, high-speed planar-passivated NPN power switching transistor in a SOT428 (D-PAK) surface mounted package.

1.2 Features and benefits

- Low thermal resistance
- Fast switching

1.3 Applications

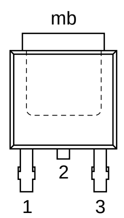
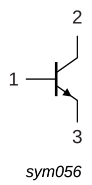
- Electronic lighting ballasts
- Inverters
- DC-to-DC converters
- Motor control systems

1.4 Quick reference data

- $V_{CESM} \leq 700$ V
- $P_{tot} \leq 80$ W
- $I_C \leq 4$ A
- $h_{FEsat} = 12.5$ (typ)

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	base	 SOT428 (D-PAK)	
2	collector [1]		
3	emitter		
mb	mounting base; connected to collector		

[1] It is not possible to make a connection to pin 2 of the SOT428 (D-PAK) package.

3. Ordering information

Table 2. Ordering information

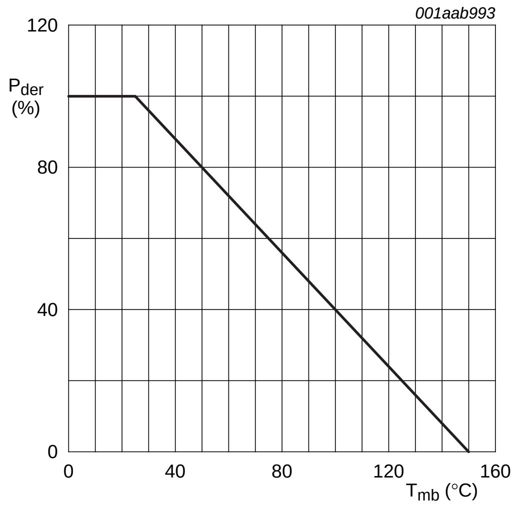
Type number	Package		
	Name	Description	Version
BUJ103AD	D-PAK	plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	peak collector-emitter voltage	V_{BE} = 0 V	-	700	V
V_{CBO}	collector-base voltage	open emitter	-	700	V
V_{CEO}	collector-emitter voltage	open base	-	400	V
I_C	collector current (DC)		-	4	A
I_{CM}	peak collector current		-	8	A
I_B	base current (DC)		-	2	A
I_{BM}	peak base current		-	4	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C; see Figure 1	-	80	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	150	°C



$$P_{der}(\%) = \frac{P_{tot}}{P_{tot(25\,°C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 2		-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	75	-	K/W

[1] Device mounted on a printed-circuit board; minimum footprint.

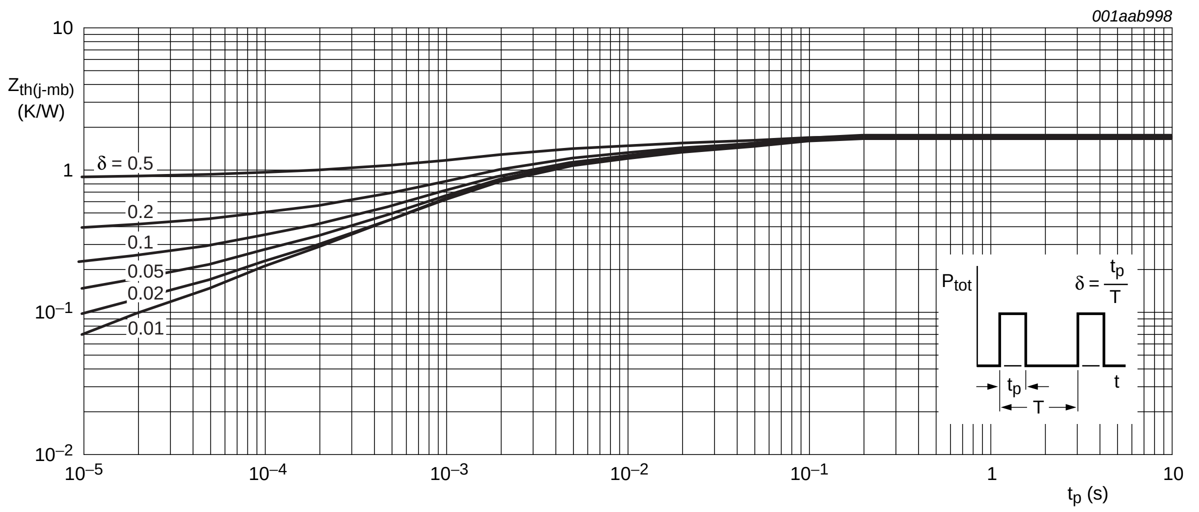


Fig 2. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5. Characteristics

T_{mb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{CES}	collector-emitter cut-off current	V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$	[1]	-	-	1.0	mA
		V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$; T_j = 125 °C	[1]	-	-	2.0	mA
I_{CBO}	collector-base cut-off current	V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$	[1]	-	-	1.0	mA
I_{CEO}	collector-emitter cut-off current	V_{CEO} = $V_{CEOMmax}$ = 400 V	[1]	-	-	0.1	mA
I_{EBO}	emitter-base cut-off current	V_{EB} = 7 V; I_C = 0 A		-	-	0.1	mA
V_{CEOsus}	collector-emitter sustaining voltage	I_B = 0 A; I_C = 10 mA; L = 25 mH; see Figure 3 and 4		400	-	-	V
V_{CEsat}	collector-emitter saturation voltage	I_C = 3.0 A; I_B = 0.6 A; see Figure 10		-	0.25	1.0	V
V_{BEsat}	base-emitter saturation voltage	I_C = 3.0 A; I_B = 0.6 A; see Figure 11		-	0.97	1.5	V
h_{FE}	DC current gain	I_C = 1 mA; V_{CE} = 5 V; see Figure 9		10	17	32	
		I_C = 500 mA; V_{CE} = 5 V		13	22	32	

Table 5. Characteristics *...continued*

T_{mb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
h_{FEsat}	DC saturation current gain	I_C = 2.0 A; V_{CE} = 5 V	11	16	22	
		I_C = 3.0 A; V_{CE} = 5 V	-	12.5	-	
Dynamic characteristics						
Switching times (resistive load); see Figure 5 and 6						
t_{on}	turn-on time	I_{Con} = 2.5 A; I_{Bon} = −I_{Boff} = 0.5 A; R_L = 75 Ω	-	0.52	0.6	µs
t_{stg}	storage time		-	2.7	3.3	µs
t_f	fall time		-	0.3	0.35	µs
Switching times (inductive load); see Figure 7 and 8						
t_{stg}	storage time	I_{Con} = 2 A; I_{Bon} = 0.4 A; L_B = 1 µH; V_{BB} = −5 V	-	1.2	1.4	µs
t_f	fall time		-	30	60	ns
Switching times (inductive load); see Figure 7 and 8						
t_{stg}	storage time	I_{Con} = 2 A; I_{Bon} = 0.4 A; L_B = 1 µH; V_{BB} = −5 V; T_j = 100 °C	-	-	1.8	µs
t_f	fall time		-	-	120	ns

[1] Measured with half sine-wave voltage (curve tracer).

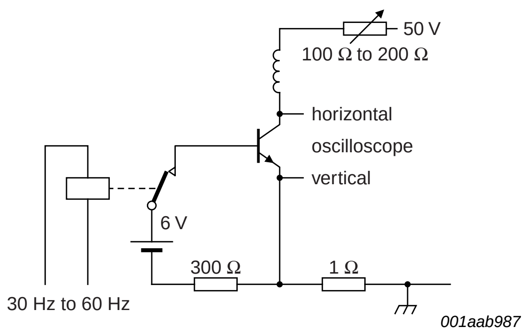


Fig 3. Test circuit for collector-emitter sustaining voltage

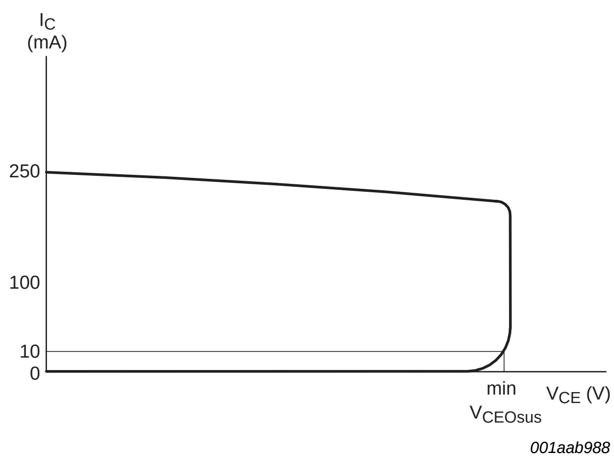
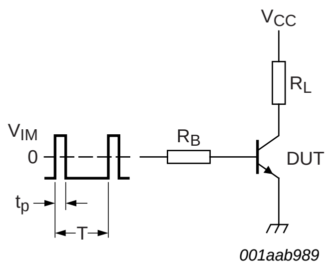


Fig 4. Oscilloscope display for collector-emitter sustaining voltage test waveform



V_{IM} = –6 V to +8 V; V_{CC} = 250 V; t_p = 20 μs;
$\delta = t_p/T$ = 0.01.
R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig 5. Test circuit for resistive load switching

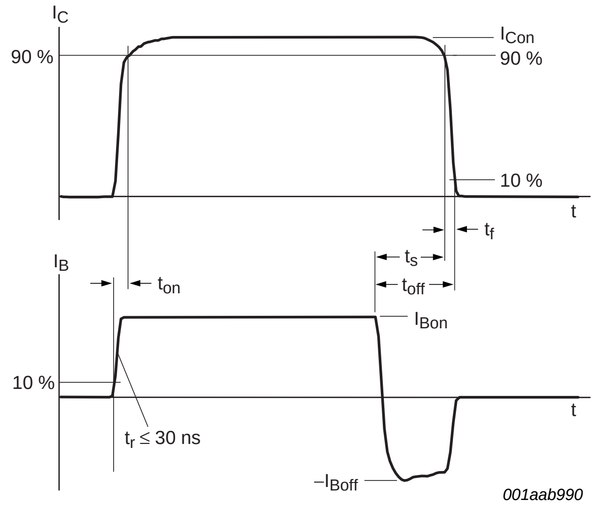
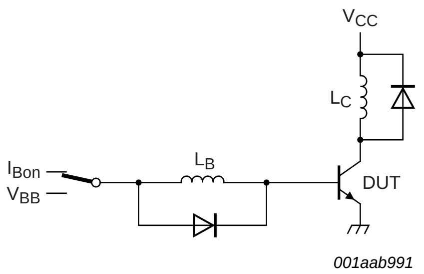


Fig 6. Switching times waveforms for resistive load



V_{CC} = 300 V; V_{BB} = –5 V; L_C = 200 μH; L_B = 1 μH.

Fig 7. Test circuit for inductive load switching

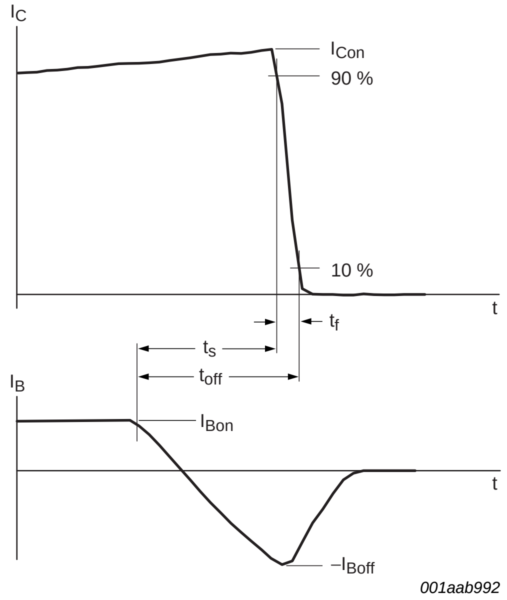


Fig 8. Switching times waveforms for inductive load

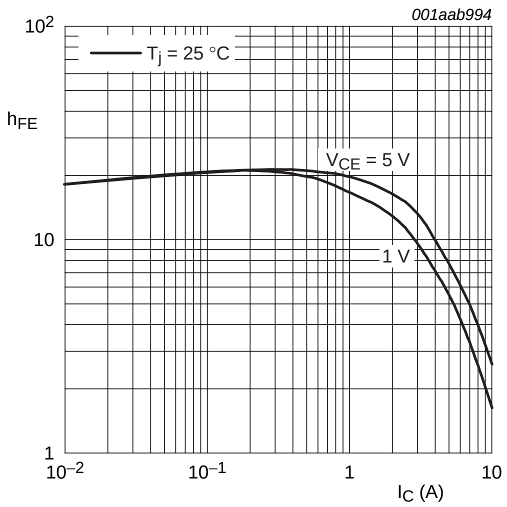
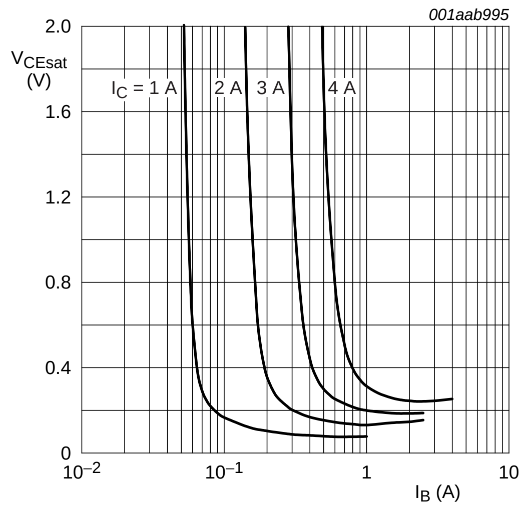
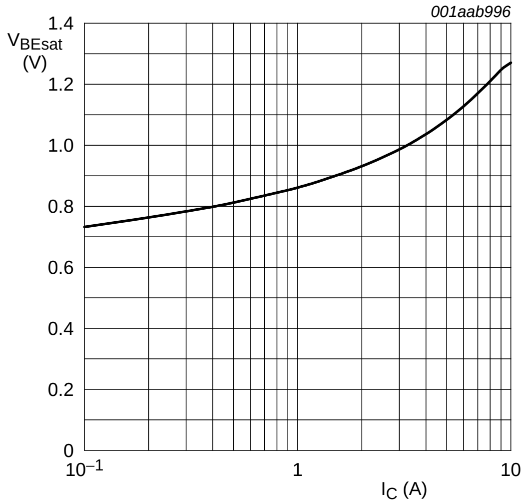


Fig 9. DC current gain as a function of collector current; typical values



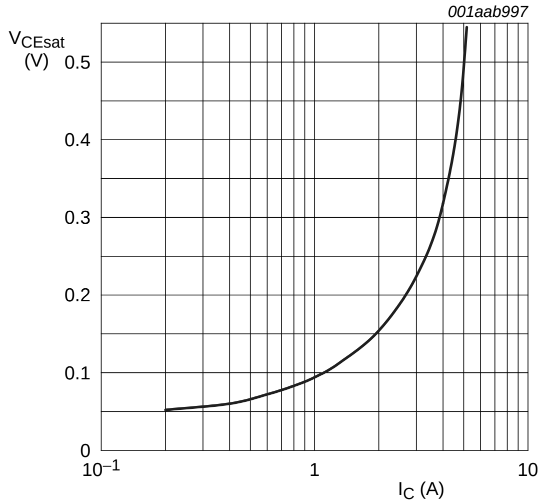
T_j = 25 °C.

Fig 10. Collector-emitter saturation voltage as a function of base current; typical values



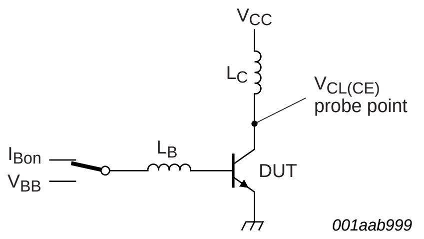
I_C/I_B = 4.

Fig 11. Base-emitter saturation voltage as a function of collector current; typical values



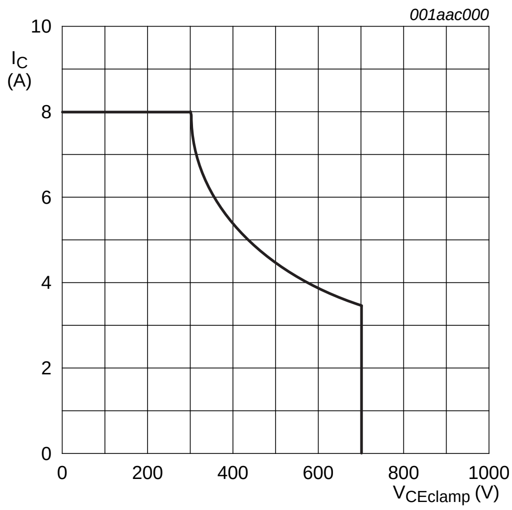
I_C/I_B = 4.

Fig 12. Collector-emitter saturation voltage as a function of collector current; typical values



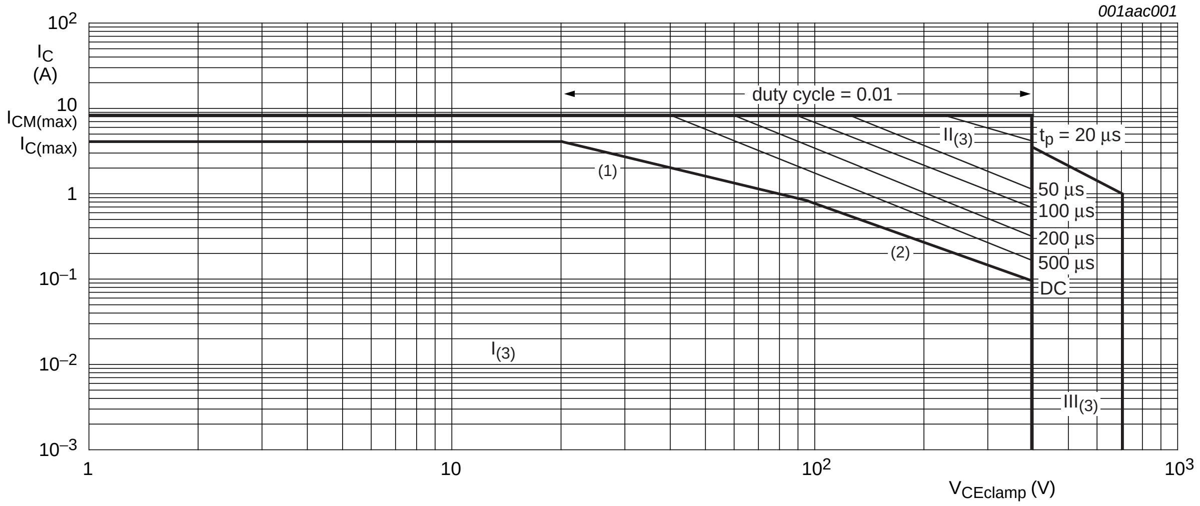
$V_{CEclamp} \leq 1000$ V; $V_{CC} = 150$ V; $V_{BB} = -5$ V; $L_B = 1$ µH; $L_C = 200$ µH.

Fig 13. Test circuit for reverse bias safe operating area



$T_j \leq T_{j(max)}$.

Fig 14. Reverse bias safe operating area



$T_{mb} \leq 25$ °C; Mounted with heatsink compound and 30 ± 5 Newton force on the center of the envelope.

(1) P_{tot} maximum and P_{tot} peak maximum lines.

(2) Second breakdown limits.

(3) I = Region of permissible DC operation.

II = Extension for repetitive pulse operation.

III = Extension during turn-on in single transistor converters provided that $R_{BE} \leq 100$ Ω and $t_p \leq 0.6$ µs.

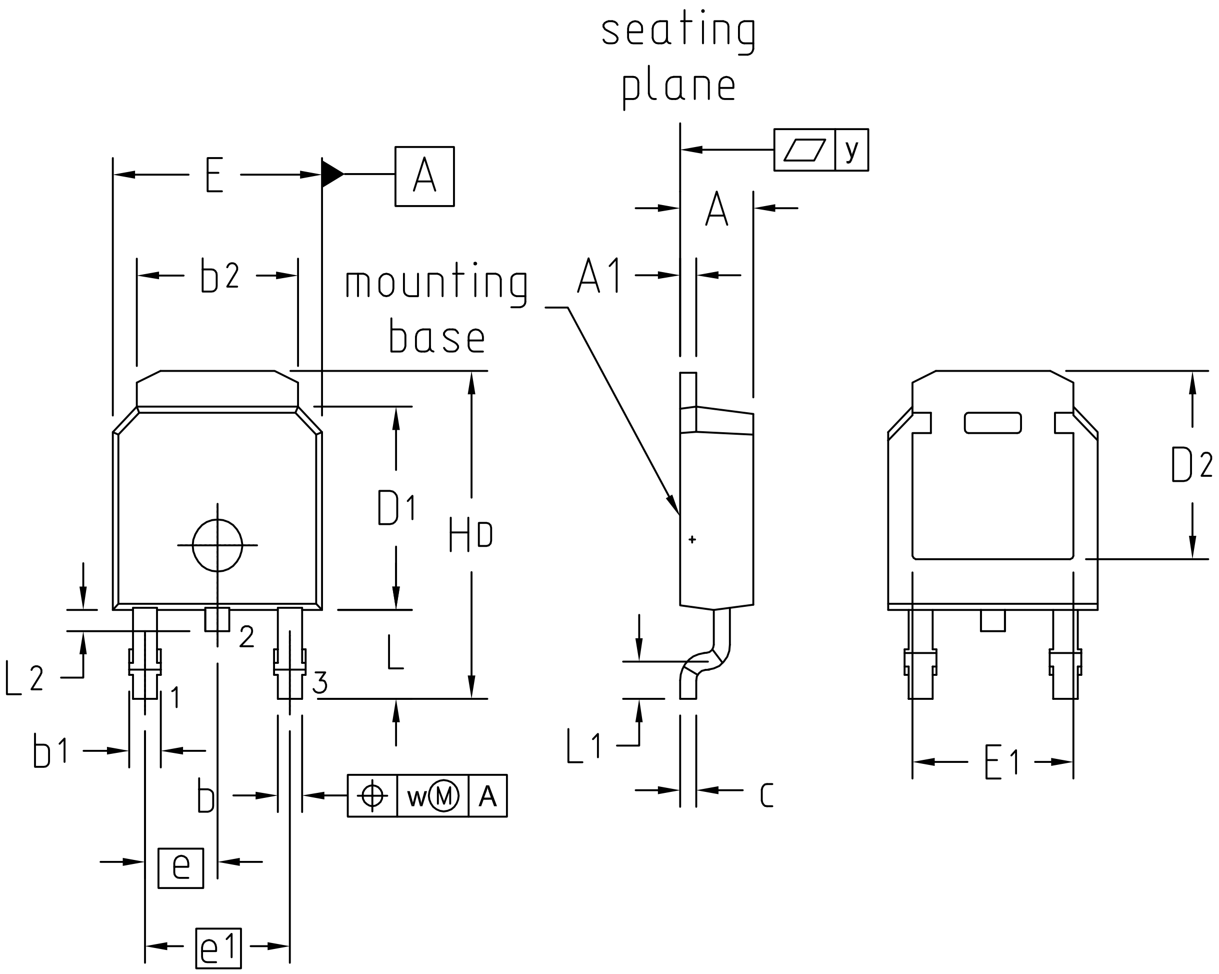
Fig 15. Forward bias safe operating area

7. Package information

Epoxy meets requirements of UL94 V-0 at ⅛ inch.

8. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) SOT428



UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2	E	E_1	e	e_1	H_D	L	L_1	L_2	w	y
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.00 min.	6.73 6.47	4.45 min.	2.285	4.57	10.40 9.60	2.95 2.55	0.5 min.	0.90 0.50	0.2	0.20 max.

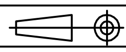
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428		TO-252				

Fig. 2. Package outline DPAK (SOT428)

9. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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