



STY100NM60N

N-channel 600 V, 0.028 Ω typ., 98 A MDmesh™ II
Power MOSFET in a Max247 package

Datasheet — production data

Features

| Type | V _{DSS} @ T _{Jmax} | R _{DS(on)} max | I _D |
|-------------|---|-------------------------|----------------|
| STY100NM60N | 650 V | < 0.029 Ω | 98 A |

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

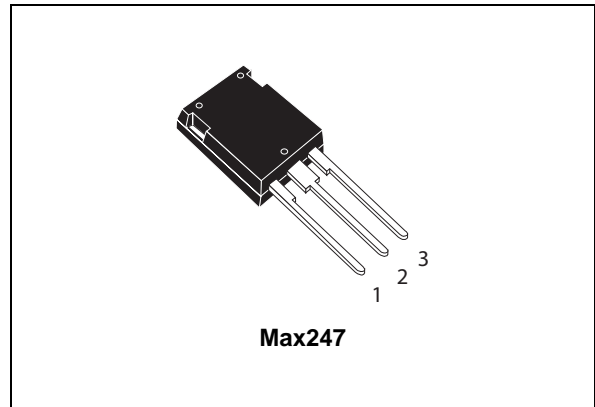


Figure 1. Internal schematic diagram

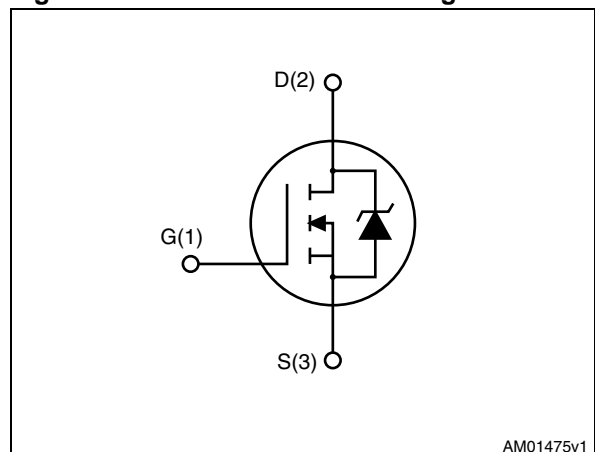


Table 1. Device summary

| Order code | Marking | Package | Packaging |
|-------------|----------|---------|-----------|
| STY100NM60N | 100NM60N | Max247 | Tube |

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|-------------|------|
| V_{GS} | Gate- source voltage | 25 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ °C}$ | 98 | A |
| I_D | Drain current (continuous) at $T_C = 100\text{ °C}$ | 62 | A |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 392 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ °C}$ | 625 | W |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 15 | V/ns |
| T_{stg} | Storage temperature | - 55 to 150 | °C |
| T_j | Max. operating junction temperature | | °C |

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 98\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|--|-------|------|
| $R_{thj-case}$ | Thermal resistance junction-case max | 0.2 | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient max | 30 | °C/W |
| T_j | Maximum lead temperature for soldering purpose | 300 | °C |

Table 4. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|---|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax}) | 15 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j=25\text{ °C}$, $I_D=I_{ar}$, $V_{DD}=50$) | 757 | mJ |

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified).

Table 5. On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|---|------|-------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ($V_{GS} = 0$) | $I_D = 1\text{ mA}$ | 600 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}, T_C = 125\text{ °C}$ | | | 10 150 | μA μA |
| I_{GSS} | Gate-body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 25\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}, I_D = 49\text{ A}$ | | 0.028 | 0.029 | Ω |

Table 6. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------|-------------------------------|---|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 50\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$ | - | 9600 | - | pF |
| C_{oss} | Output capacitance | | | 850 | | pF |
| C_{rss} | Reverse transfer capacitance | | | 50 | | pF |
| $C_{oss(eq)}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0$ | - | 1602 | - | pF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}$ open drain | - | 1.3 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 480\text{ V}, I_D = 98\text{ A},$ $V_{GS} = 10\text{ V}$ (see Figure 15) | - | 330 | - | nC |
| Q_{gs} | Gate-source charge | | | 40 | | nC |
| Q_{gd} | Gate-drain charge | | | 174 | | nC |

1. $C_{oss(eq)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 300\text{ V}, I_D = 49\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 16) and (see Figure 19) | - | 45 | - | ns |
| t_r | Rise time | | | 52 | | ns |
| $t_{d(off)}$ | Turn-off delay time | | | 372 | | ns |
| t_f | Fall time | | | 81 | | ns |

Table 8. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 98 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 392 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 98 \text{ A}, V_{GS} = 0$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 98 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ | - | 622 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 60 \text{ V}$ | - | 16.5 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 16) | - | 52.5 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 98 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ | - | 820 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ | - | 27 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 16) | - | 66 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

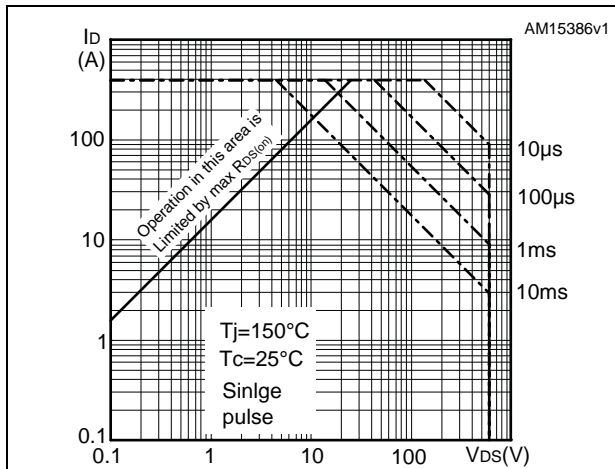


Figure 3. Thermal impedance

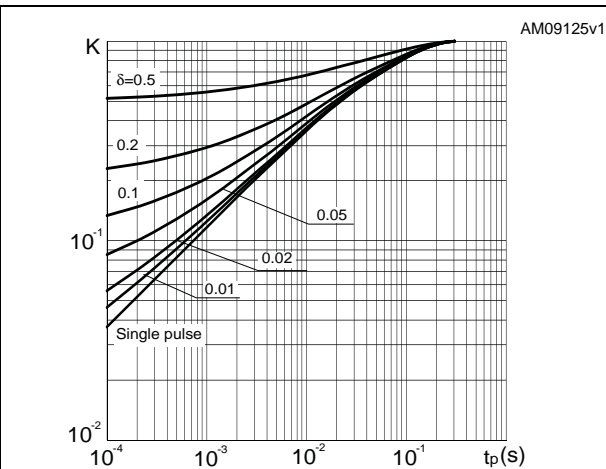


Figure 4. Output characteristics

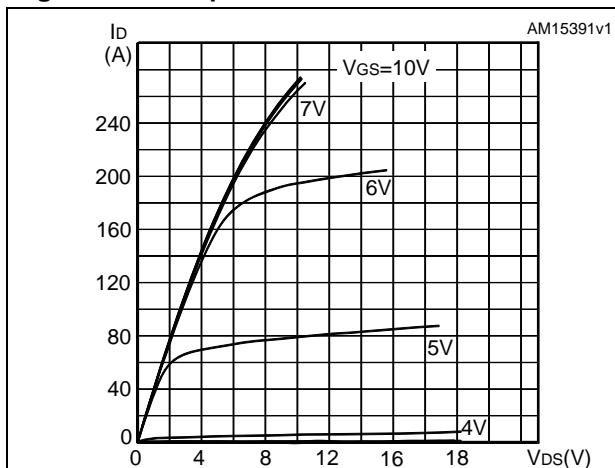


Figure 5. Transfer characteristics

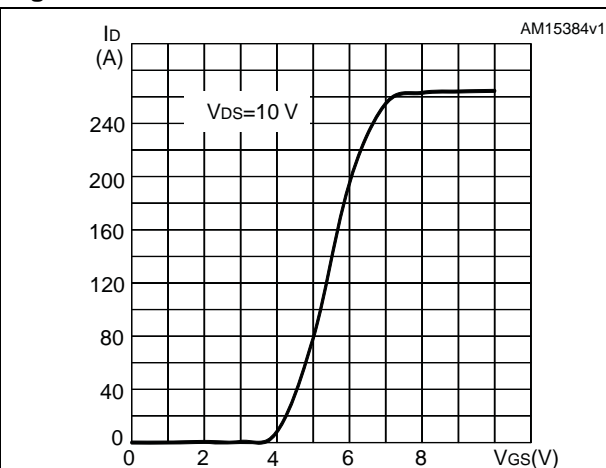


Figure 6. Gate charge vs gate-source voltage

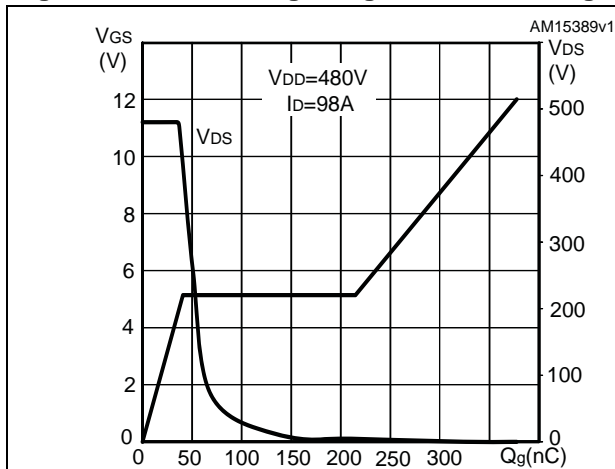


Figure 7. Static drain-source on-resistance

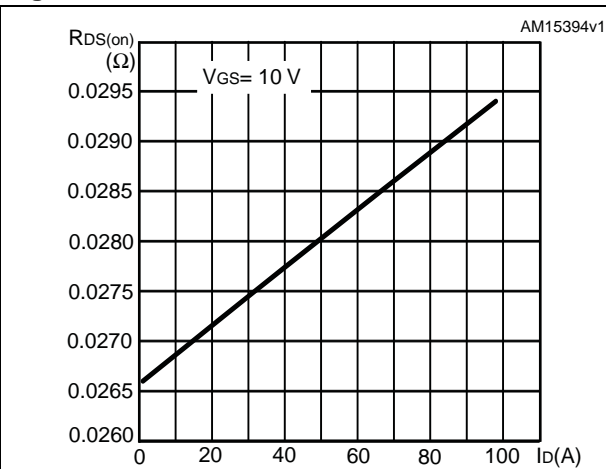


Figure 8. Capacitance variations

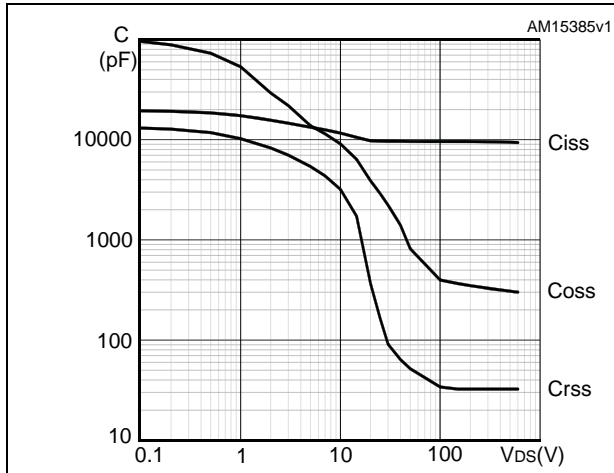


Figure 9. Normalized on-resistance vs temperature

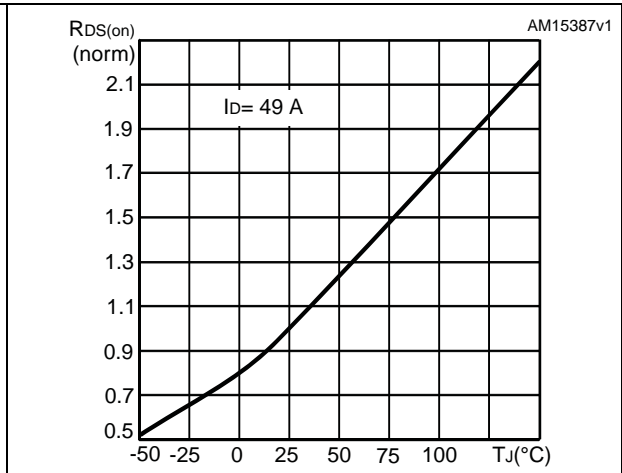


Figure 10. Normalized gate threshold voltage vs temperature

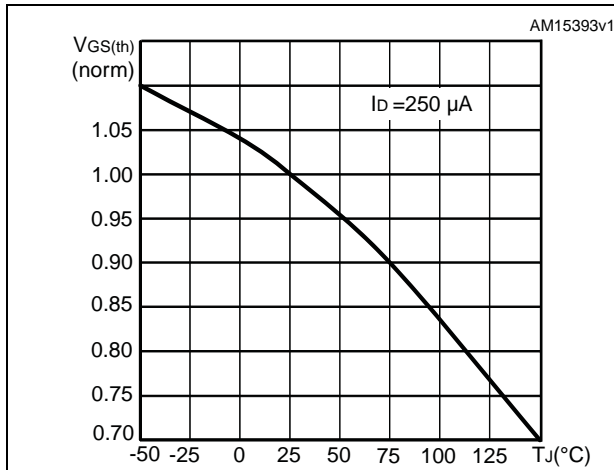


Figure 11. Normalized B_{VDS} vs temperature

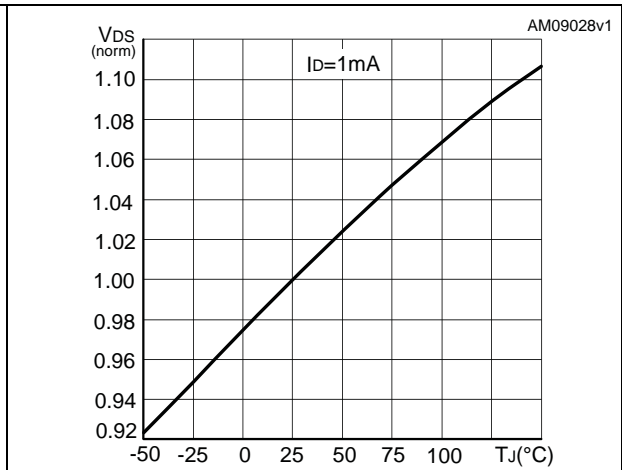


Figure 12. Source-drain diode forward characteristics

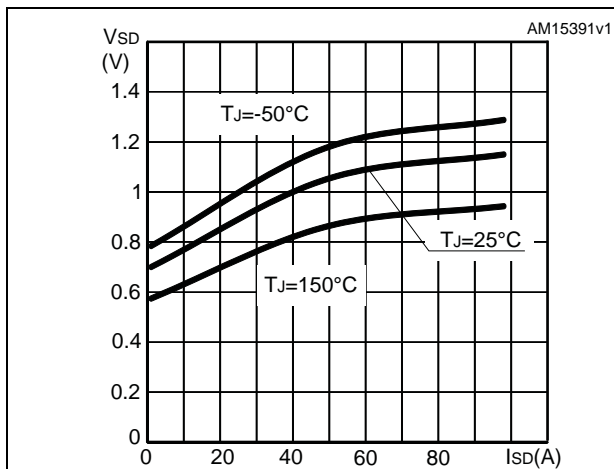
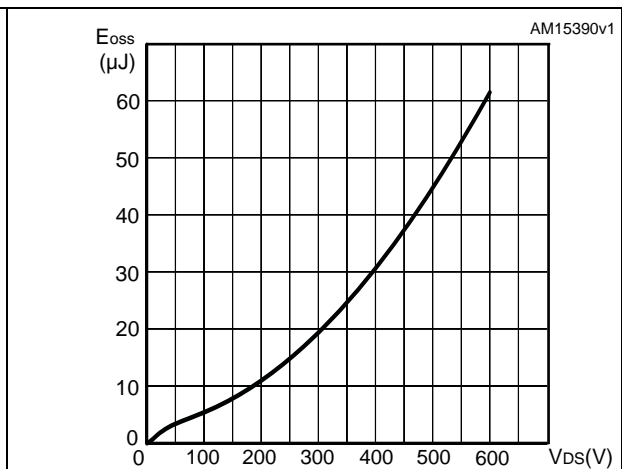
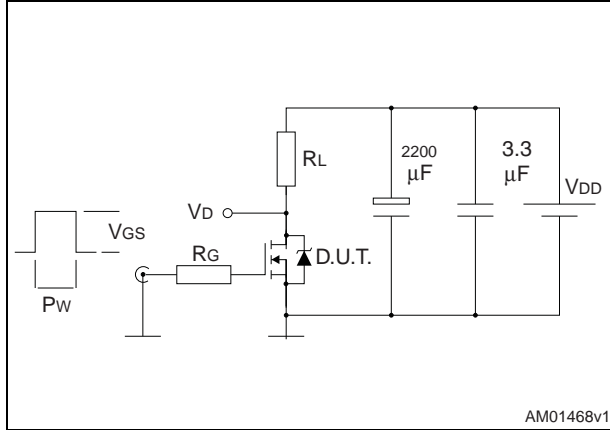


Figure 13. Output capacitance stored energy



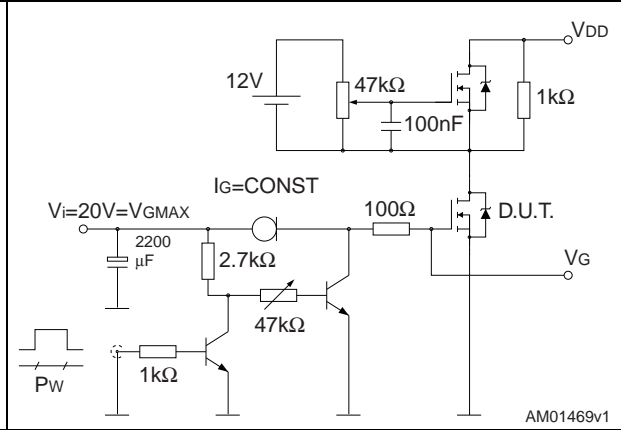
3 Test circuits

Figure 14. Switching times test circuit for resistive load



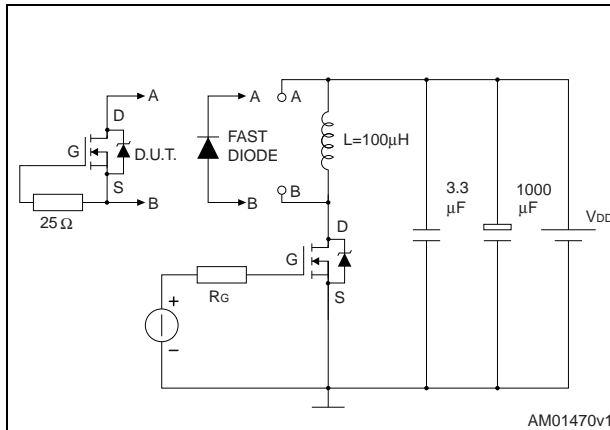
AM01468v1

Figure 15. Gate charge test circuit



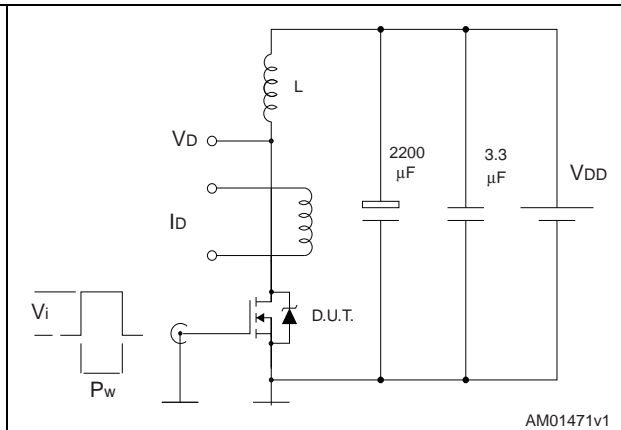
AM01469v1

Figure 16. Test circuit for inductive load switching and diode recovery times



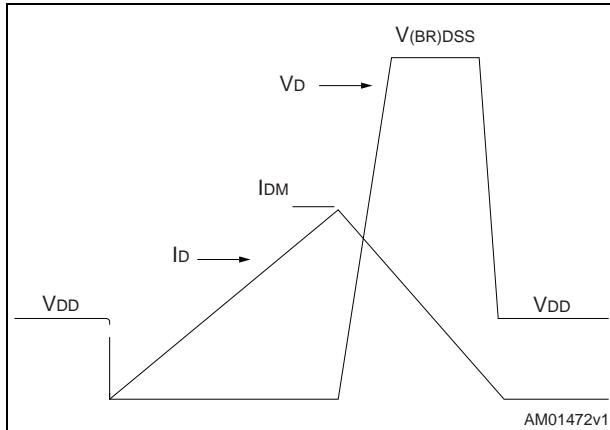
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Figure 17. Unclamped inductive load test circuit



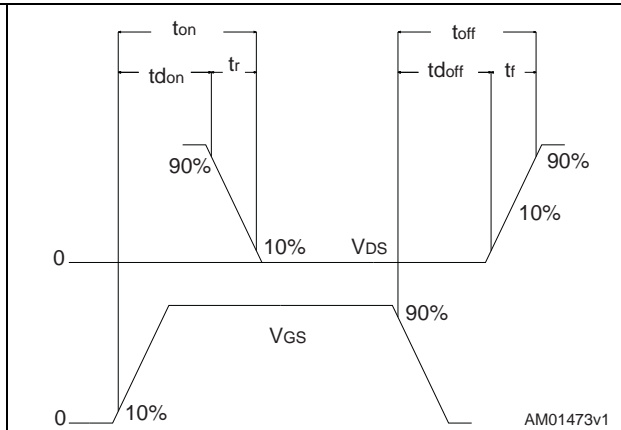
AM01471v1

Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



AM01473v1

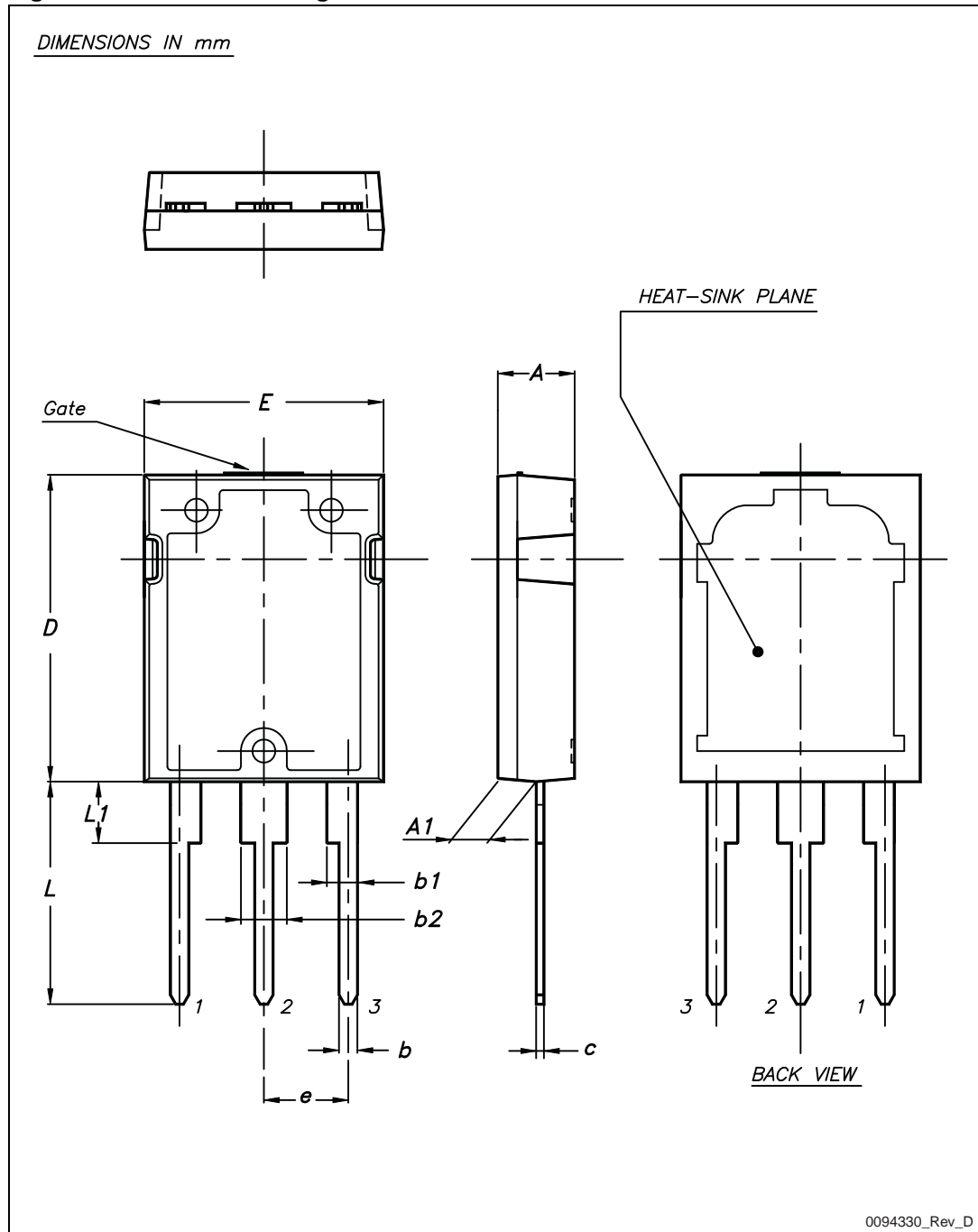
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. Max247 mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 4.70 | | 5.30 |
| A1 | 2.20 | | 2.60 |
| b | 1.00 | | 1.40 |
| b1 | 2.00 | | 2.40 |
| b2 | 3.00 | | 3.40 |
| c | 0.40 | | 0.80 |
| D | 19.70 | | 20.30 |
| e | 5.35 | | 5.55 |
| E | 15.30 | | 15.90 |
| L | 14.20 | | 15.20 |
| L1 | 3.70 | | 4.30 |

Figure 20. Max247 drawing



5 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 14-Sep-2011 | 1 | First release. |
| 05-Nov-2012 | 2 | Document status promoted from preliminary to production data. Added Section 2.1: Electrical characteristics (curves) . Minor text changes. |

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