

MC74LVX126

Quad Bus Buffer

With 5V-Tolerant Inputs

The MC74LVX126 is an advanced high speed CMOS quad bus buffer. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

The MC74LVX126 requires the 3-state control input (OE) to be set Low to place the output into the high impedance state.

Features

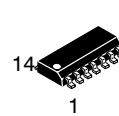
- High Speed: $t_{PD} = 4.4$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25^\circ$ C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.5$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model >2000 V
Machine Model >200 V
- **These devices are available in Pb-free package(s). Specifications herein apply to both standard and Pb-free devices. Please see our website at www.onsemi.com for specific Pb-free orderable part numbers, or contact your local ON Semiconductor sales office or representative.**



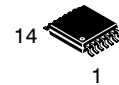
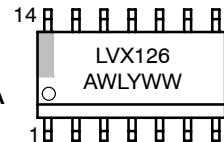
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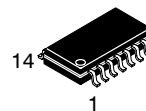
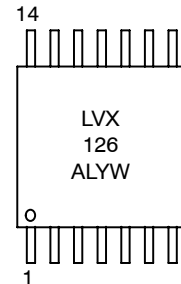
MARKING DIAGRAMS



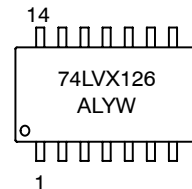
SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



SOEIAJ-14
M SUFFIX
CASE 965



A	=	Assembly
Location		
L, WL	=	Wafer Lot
Y	=	Year
W, WW	=	Work
Week		

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74LVX126

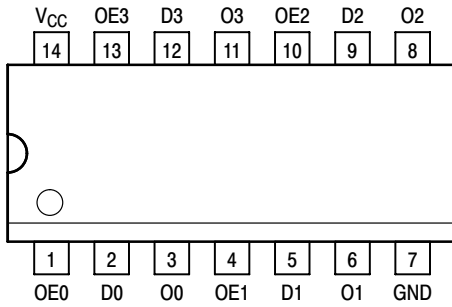


Figure 1. 14-Lead Pinout (Top View)

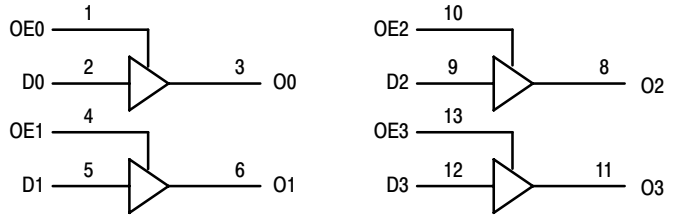


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
OEn	Output Enable Inputs
Dn	Data Inputs
On	3-State Outputs

FUNCTION TABLE

INPUTS		OUTPUTS
OEn	Dn	On
H	L	L
H	H	H
L	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{in}	DC Input Voltage	-0.5 to +7.0	V
V _{out}	DC Output Voltage	-0.5 to V _{CC} +0.5	V
I _{IK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation	180	mW
T _{stg}	Storage Temperature	-65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	3.6	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-40	+125	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = ≤ 85°C		T _A = ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		1.5 2.0 2.4		V
V _{IL}	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8		0.5 0.8 0.8	V
V _{OH}	High-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OH} = -50 μA I _{OH} = -50 μA I _{OH} = -4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48			1.9 2.9 2.34	V
V _{OL}	Low-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44		0.1 0.1 0.52	V
I _{in}	Input Leakage Current	V _{in} = 5.5 V or GND	3.6			±0.1		±1.0		±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	3.6			±0.25		±2.5		±5.0	μA
I _{CC}	Quiescent Supply Current	V _{in} = V _{CC} or GND	3.6			4.0		40		40	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = ≤ 85°C		T _A = ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay Input to Output	V _{CC} = 2.7 V C _L = 15 pF C _L = 50 pF		5.5 7.5	10.1 13.6	1.0 1.0	13.5 17.0	1.0 1.0	15.0 19.0	ns
		V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		3.9 5.9	6.2 9.7	1.0 1.0	8.5 12.0	1.0 1.0	11.0 14.0	
t _{PZL} , t _{PZH}	Output Enable Time OE to O	V _{CC} = 2.7 V C _L = 15 pF R _L = 1 kΩ C _L = 50 pF		5.3 7.8	9.3 12.8	1.0 1.0	12.5 16.0	1.0 1.0	15.5 18.5	ns
		V _{CC} = 3.3 ± 0.3 V C _L = 15 pF R _L = 1 kΩ C _L = 50 pF		4.0 6.5	5.6 9.1	1.0 1.0	7.5 11.0	1.0 1.0	9.5 13.0	
t _{PLZ} , t _{PHZ}	Output Disable Time OE to O	V _{CC} = 2.7 V C _L = 50 pF R _L = 1 kΩ		10.0	15.7	1.0	19.0	1.0	21.0	ns
		V _{CC} = 3.3 ± 0.3 V C _L = 50 pF R _L = 1 kΩ		8.3	11.2	1.0	13.0	1.0	15.0	
t _{OSSL} , t _{OSLH}	Output-to-Output Skew (Note 1)	V _{CC} = 2.7 V C _L = 50 pF V _{CC} = 3.3 ± 0.3 V C _L = 50 pF			1.5 1.5		1.5 1.5		1.5 1.5	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	T _A = 25°C			T _A = ≤ 85°C		T _A = ≤ 125°C		Unit
		Min	Typ	Max	Min	Max	Min	Max	
C _{in}	Input Capacitance		4	10		10		10	pF
C _{out}	Maximum Three-State Output Capacitance		6						pF
C _{PD}	Power Dissipation Capacitance (Note 2)		14						pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per bit). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.3	-0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX126D	SOIC-14	55 Units / Rail
MC74LVX126M	SOEIAJ-14	50 Units / Rail
MC74LVX126MEL	SOEIAJ-14	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SWITCHING WAVEFORMS

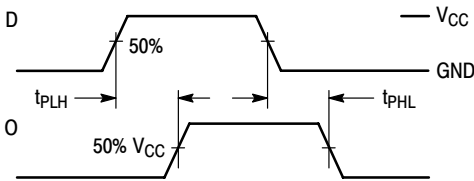


Figure 3.

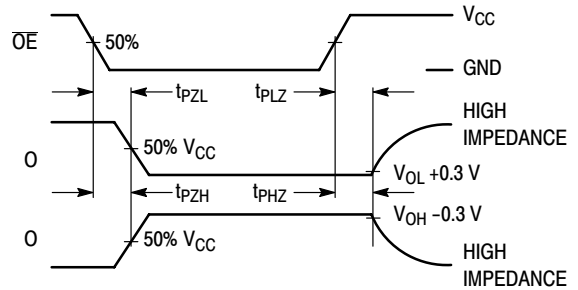
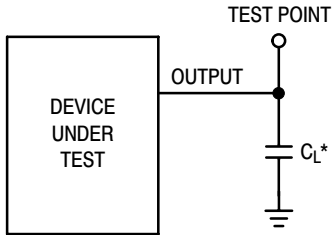


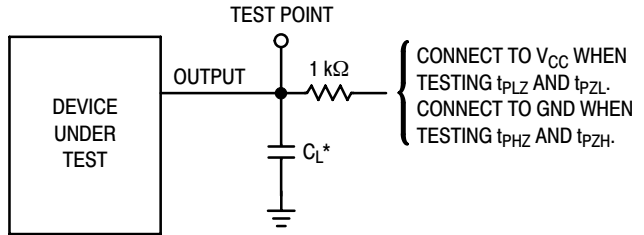
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit



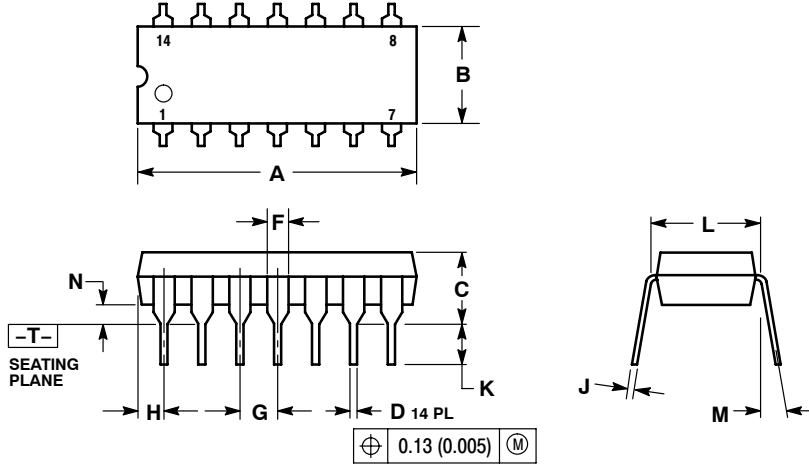
*Includes all probe and jig capacitance

Figure 6. Three-State Test Circuit

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PACKAGE DIMENSIONS

PDIP-14
P SUFFIX
CASE 646-06
ISSUE N

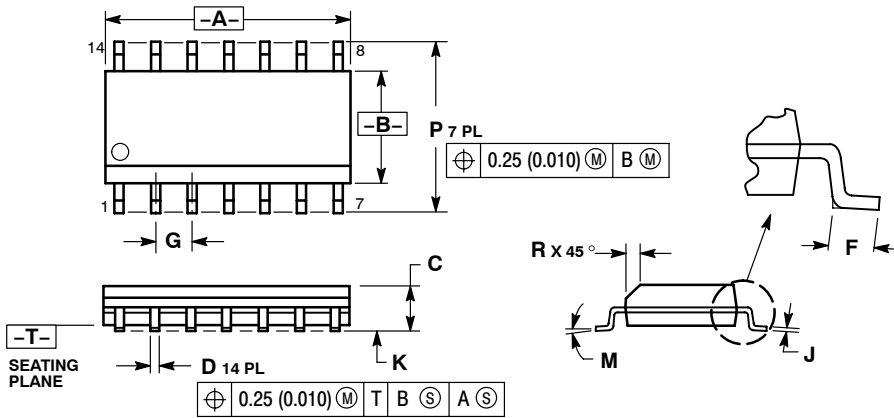


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

SOIC-14
D SUFFIX
CASE 751A-03
ISSUE G



NOTES:

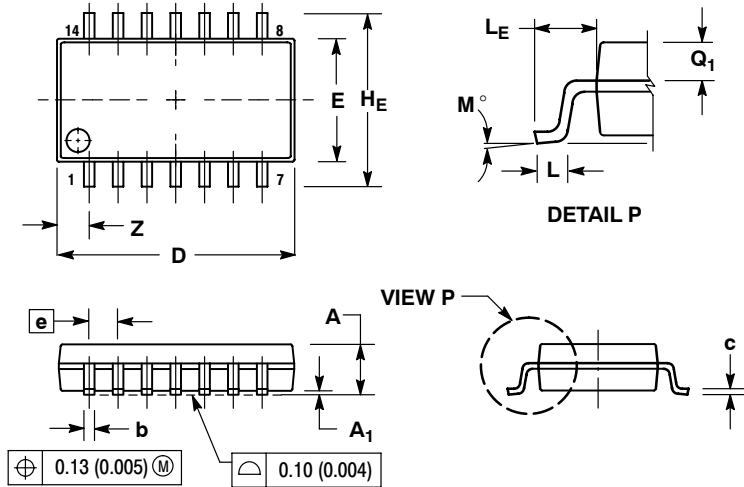
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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PACKAGE DIMENSIONS

SOEIAJ-14
M SUFFIX
CASE 965-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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