MX555ANS200M000

Ultra-Low Jitter 200MHz LVDS XO

ClockWorks® FUSION

General Description

The MX555ANS200M000 is an ultra-low phase jitter XO with LVDS output optimized for high line rate applications.

Features

- 200MHz LVDS
- Typical phase noise:
  - 94fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 5mm x 3.2mm LGA package

Absolute Maximum Ratings

Supply Voltage (VIN)...+4.6V
Lead Temperature (soldering, 10s)............................260°C
Storage Temperature (T_S)...125°C
ESD Rating (HBM)..2kV

Operating Ratings

Supply Voltage (VIN).......................+2.375V to +3.63V
Ambient Temperature (TA)....................-40°C to +85°C

Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 100 Ohms between Q and /Q.[1]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				90	mA
F0	Center Frequency			200		MHz
	Frequency Stability	Note 2			±50	ppm
Øj	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		140 94		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		100		400	ps
	Duty Cycle		45		55	%
VOH	Output High Voltage VOH max = VCM max + 1/2 VOD max	LVDS output levels	1.248	1.375	1.602	V
VOL	Output Low Voltage VOL min = VCM min - 1/2 VOD max	LVDS output levels	0.898	1.025	1.252	V
VOD	Output Differential Voltage		247	350	454	mV
VCM	Common Mode Output Voltage		1.125	1.2	1.375	V

Notes:

1. Guaranteed after thermal equilibrium.

2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX555ANS200M000	MX555A	NS2000	Tube	6-Pin 5mm x 3.2mm LGA
MX555ANS200M000-TR	MX555A	NS2000	Tape and Reel	6-Pin 5mm x 3.2mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration
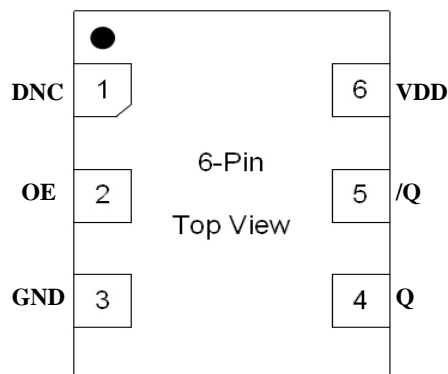
Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	DNC			Make no connection, leave floating.
2	OE	I, SE	LVCMOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVDS	Clock Output Frequency = 200MHz
6	VDD	PWR		Power Supply
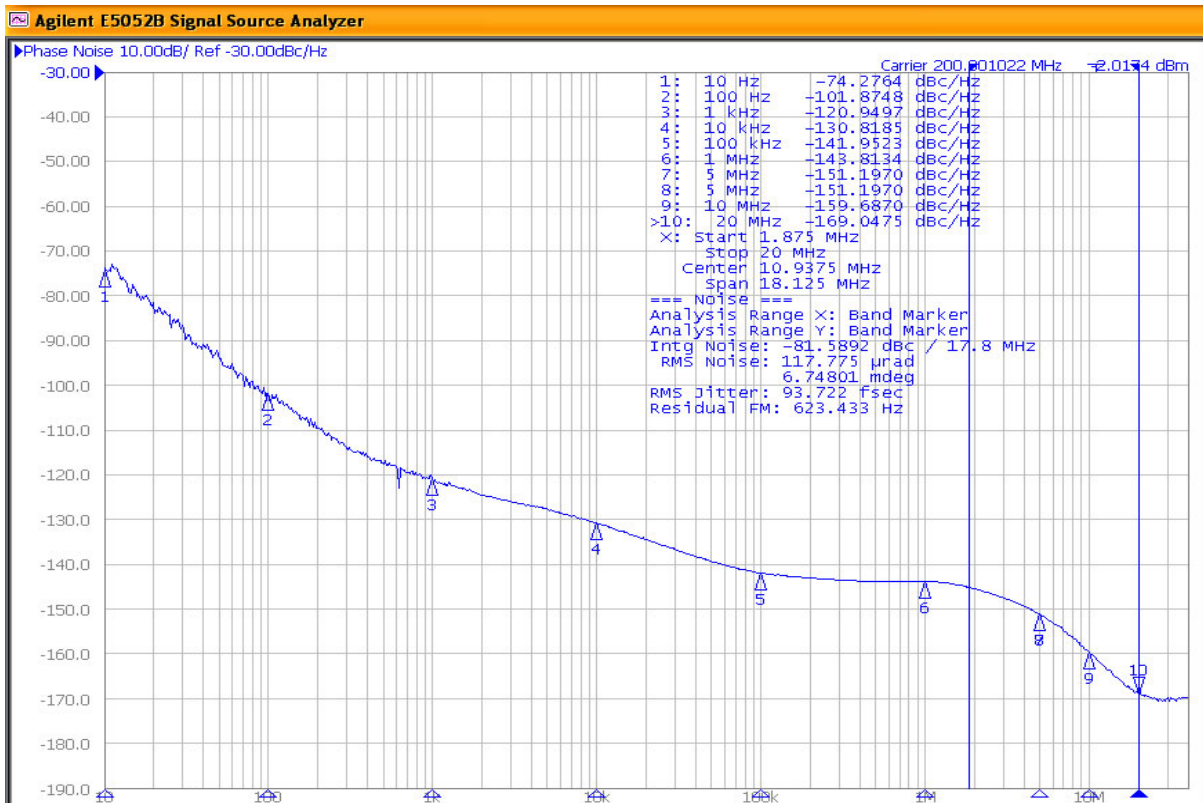
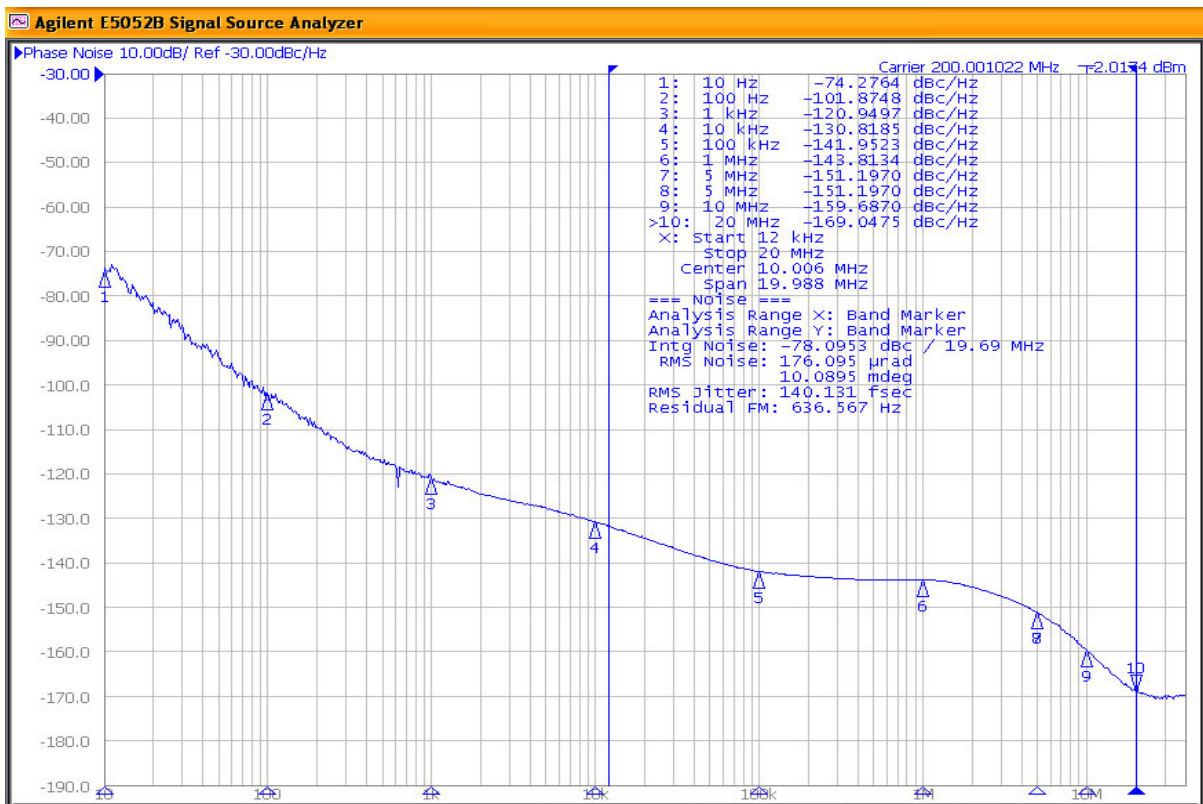**Figure 1. LVDS Output 200MHz 1.875MHz-20MHz 94fs**
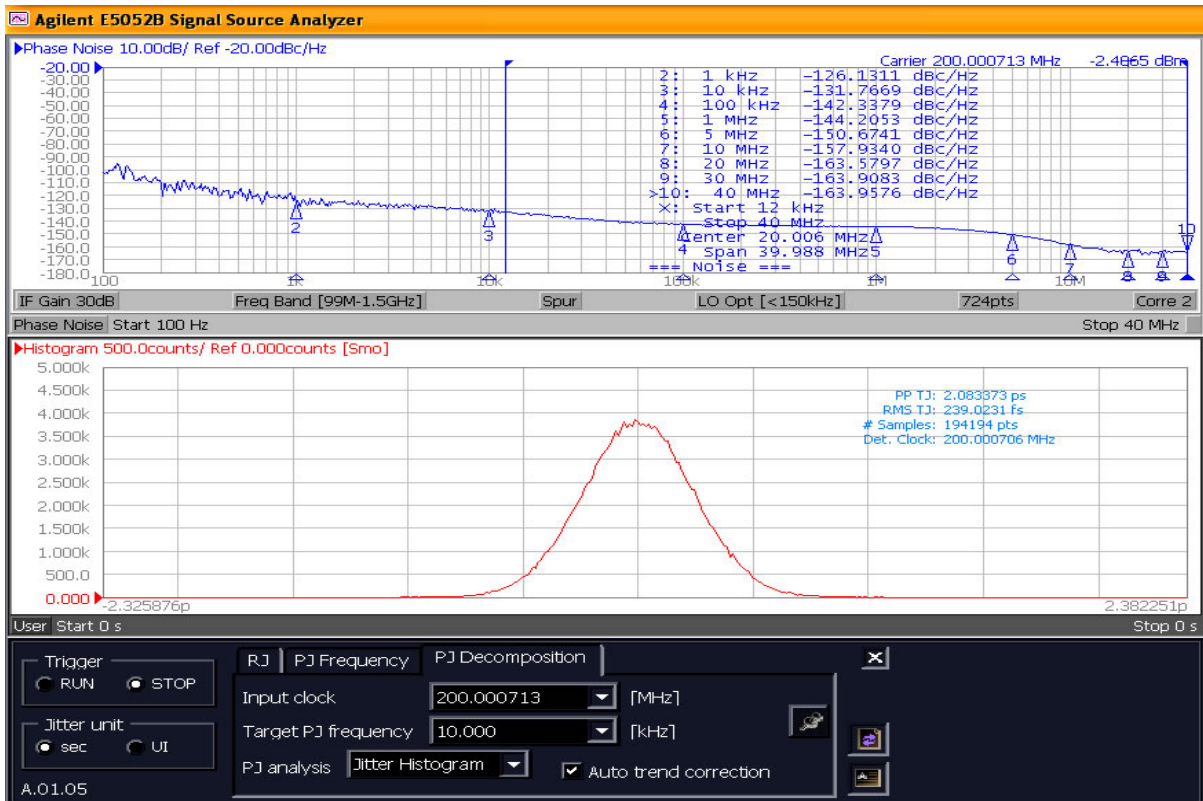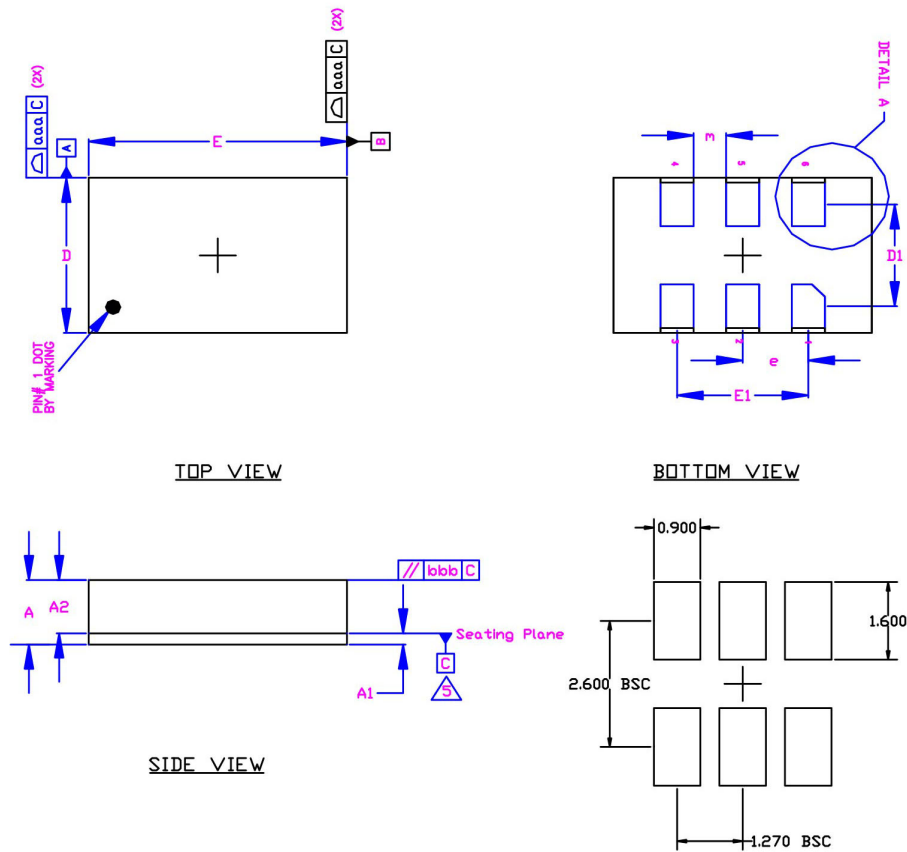

Figure 2. LVDS Output 200MHz 12kHz-20MHz 140fs

Figure 3. E5001A Period Jitter @ 200MHz LVDS, RMS TJ: 239fs, Pk-Pk TJ: 2.08ps

# Package Information and Recommended Land Pattern for 6-Pin LGA³

TOP VIEW

BOTTOM VIEW

SIDE VIEW

0.900

2.600 BSC

1.600

1.270 BSC

RECOMMENDED LAND PATTERN

Dimensional Tol.		
aaa	0.100	
bbb	0.070	

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.260	1.330	1.400
A1	0.190	0.230	0.270
A2	1.070	1.100	1.130
D	3.100	3.200	3.300
D1		2.100 BSC	
E	4.900	5.000	5.100
E1		2.540 BSC	
b	0.850	0.900	0.950
c	0.850	0.900	0.950
e		1.270 BSC	
f	0.050	0.100	0.150
k	0.860	0.910	0.960
m	0.580	0.630	0.680
n		6	

DETAIL A
SCALE 5:1
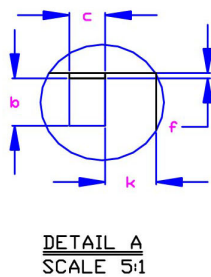
Notes

1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. 'e' represents the basic LGA pitch
4. 'n' is the maximum no. of Land for a specified Package.
5. Package warp shall be 0.050 max.
6. Substrate base is BT Resin
7. The Pin#1 corner must be identified on top side only.
8. Reference Jedec Spec M0-220

6-Pin LGA (5x3.2mm)

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

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