## ACPI Regulator/Controller for Dual Channel DDR Memory Systems

The ISL6532B provides a complete ACPI compliant power solution for up to 4 DIMM dual channel DDR/DDR2 memory systems. Included are both a synchronous buck controller and integrated LDO to supply $V_{DDQ}$ with high current during S0/S1 states and standby current during S3 state. During Run mode, a fully integrated sink-source regulator generates an accurate ($V_{DDQ}$/2) high current $V_{TT}$ voltage without the need for a negative supply. A buffered version of the $V_{DDQ}$/2 reference is provided as $V_{REF}$.

The switching PWM controller drives two N-Channel MOSFETs in a synchronous-rectified buck converter topology. The synchronous buck converter uses voltage-mode control with fast transient response. Both the switching regulator and integrated standby LDO provide a maximum static regulation tolerance of ±2% over line, load, and temperature ranges. The output is user-adjustable by means of external resistors down to 0.8V.

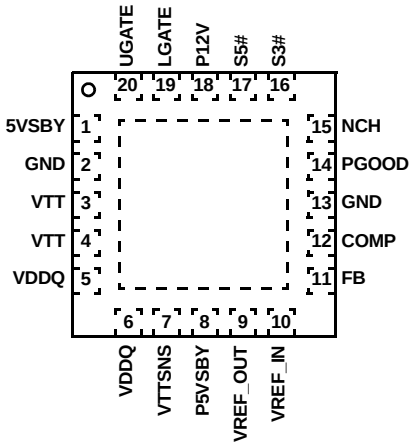
Switching the memory core output between the PWM regulator and the standby LDO during state transitions is accomplished smoothly via the internal ACPI control circuitry. The NCH signal provides synchronized switching of a backfeed blocking switch during the transitions eliminating the need to route 5V Dual to the memory supply.

An integrated soft-start feature brings $V_{DDQ}$ into regulation in a controlled manner when returning to S0/S1 state from S4/S5 or mechanical off states. During S0 the PGOOD signal indicates that all supplies are within spec and operational.

Each output is monitored for under and over-voltage events. Current limiting is included on the $V_{TT}$ and $V_{DDQ}$ standby regulators. Thermal shutdown is integrated.

## Pinout

**ISL6532B (QFN)**
TOP VIEW




## Features

- Generates 2 Regulated Voltages
  - Synchronous Buck PWM Controller with Standby LDO
  - 3A Integrated Sink/Source Linear Regulator with Accurate $V_{DDQ}$/2 Divider Reference
  - Glitch-free Transitions During State Changes
- ACPI Compliant Sleep State Control
- Integrated $V_{REF}$ Buffer
- PWM Controller Drives Low Cost N-Channel MOSFETs
- 250kHz Constant Frequency Operation
- Tight Output Voltage Regulation
  - Both Outputs: ±2% Over Temperature
- 5V or 3.3V Down Conversion
- Fully-Adjustable Outputs with Wide Voltage Range: Down to 0.8V supports DDR and DDR2 Specifications
- Simple Single-Loop Voltage-Mode PWM Control Design
- Fast PWM Converter Transient Response
- Over Current Protection on $V_{TT}$ and Under/Over-Voltage Monitoring of Both Outputs
- Integrated Thermal Shutdown Protection
- QFN Package Option
  - QFN Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - QFN Near Chip Scale Package Footprint; Improves PCB Efficiency, Thinner in Profile
- Pb-free available

## Applications

- Single and Dual Channel DDR Memory Power Systems in ACPI compliant PCs
- Graphics cards - GPU and memory supplies
- ASIC power supplies
- Embedded processor and I/O supplies
- DSP supplies

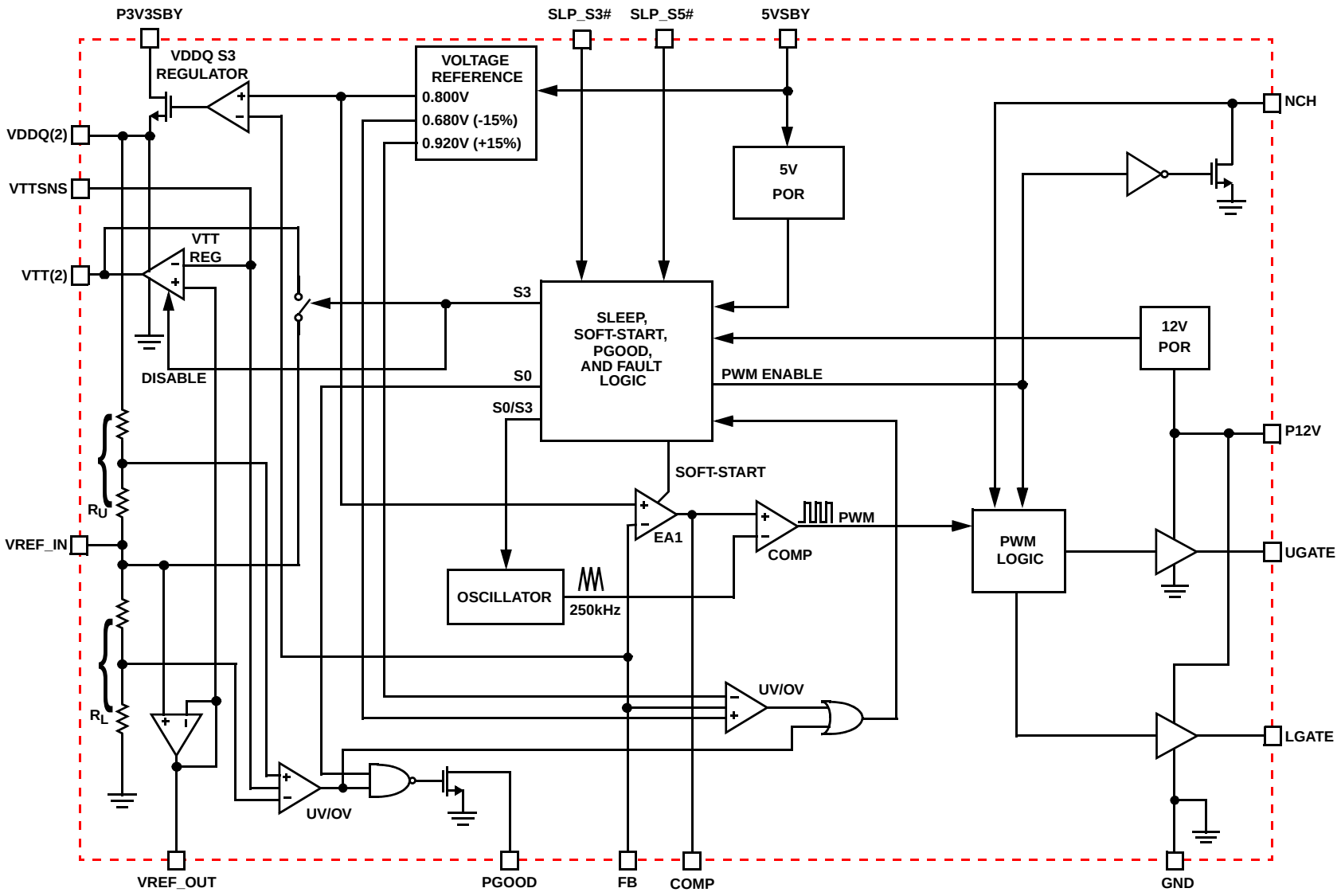
## Ordering Information

| PART NUMBER | TEMP. RANGE ($^{o}$C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| ISL6532BCR | 0 to 70 | 20 Ld 6x6 QFN | L20.6x6 |
| ISL6532BCRZ (See Note) | 0 to 70 | 20 Ld 6x6 QFN (Pb-free) | L20.6x6 |

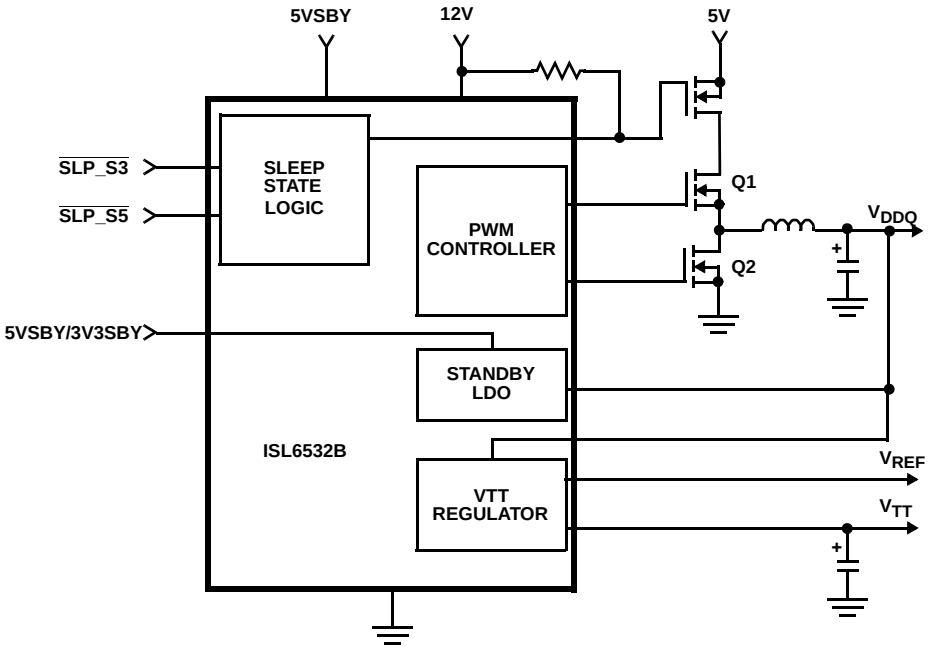
*Add "-T" suffix to part number for tape and reel packaging.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

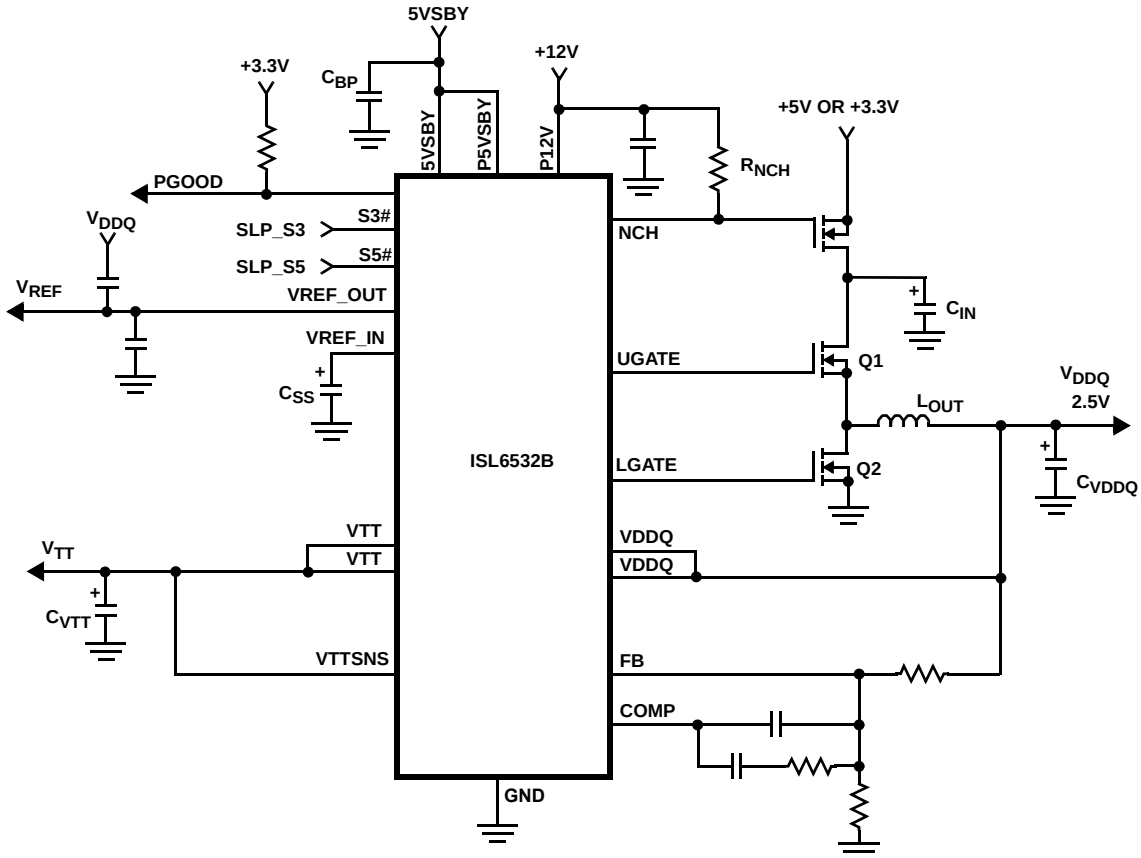
## Block Diagram



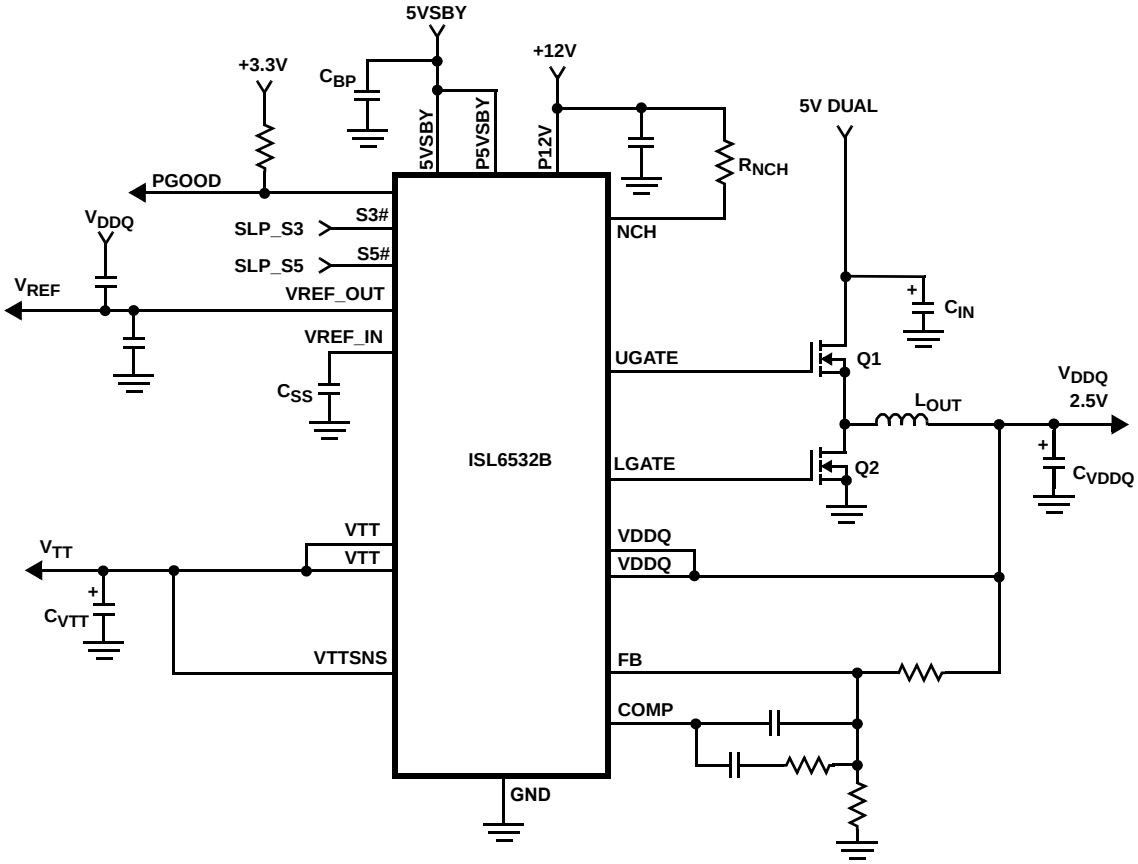
## Simplified Power System Diagram




## Typical Application - 5V or 3.3V Input



## Typical Application - Input From 5V Dual



## Absolute Maximum Ratings

5VSBY . . . . . GND - 0.3V to +7V
P12V . . . . . GND - 0.3V to +14V
UGATE, LGATE, NCH . . . . . GND - 0.3V to P12V + 0.3V
All other Pins . . . . . GND - 0.3V to 5VSBY + 0.3V
ESD Classification . . . . . Level 2

## Thermal Information

| Thermal Resistance (Typical, Notes 1, 2) | $\theta_{JA}$ ($^{o}$C/W) | $\theta_{JC}$ ($^{o}$C/W) |
|---|---|---|
| QFN Package | 32 | 5 |

Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}$C
Maximum Storage Temperature Range . . . . . $-65^{o}$C to $150^{o}$C
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}$C

## Recommended Operating Conditions

Supply Voltage on 5VSBY . . . . . +5V ±10%
Supply Voltage on P12V . . . . . +12V ±10%
Supply Voltage on 3V3SBY . . . . . +3.3V ±10%
Ambient Temperature Range . . . . . $0^{o}$C to $70^{o}$C
Junction Temperature Range . . . . . $0^{o}$C to $125^{o}$C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams and Typical Application Schematics

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **5VSBY SUPPLY CURRENT** | | | | | | |
| Nominal Supply Current | $I_{CC\_S0}$ | S3# & S5# HIGH, UGATE/LGATE Open | 3.00 | 5.25 | 7.25 | mA |
| | $I_{CC\_S3}$ | S3# LOW, S5# HIGH, UGATE/LGATE Open | 3.50 | - | 4.75 | mA |
| | $I_{CC\_S5}$ | S5# LOW, S3# Don't Care, UGATE/LGATE Open | 300 | - | 800 | µA |
| **POWER-ON RESET** | | | | | | |
| Rising 5VSBY POR Threshold | | | 4.00 | - | 4.35 | V |
| Falling 5VSBY POR Threshold | | | 3.60 | - | 3.95 | V |
| Rising P12V POR Threshold | | | 10.0 | - | 10.5 | V |
| Falling P12V POR Threshold | | | 8.80 | - | 9.75 | V |
| **OSCILLATOR AND SOFT-START** | | | | | | |
| PWM Frequency | $f_{OSC}$ | | 220 | 250 | 280 | kHz |
| Ramp Amplitude | $\Delta V_{OSC}$ | | - | 1.5 | - | V |
| Error Amp Reset Time | $t_{RESET}$ | S5# LOW to S5# HIGH | 6.5 | - | 9.5 | ms |
| VDDQ Soft-Start Interval | $t_{SS}$ | S5# LOW to S5# HIGH | 6.5 | - | 9.5 | ms |
| **REFERENCE VOLTAGE** | | | | | | |
| Reference Voltage | $V_{REF}$ | | - | 0.800 | - | V |
| System Accuracy | | | -2.0 | - | +2.0 | % |
| **PWM CONTROLLER ERROR AMPLIFIER** | | | | | | |
| DC Gain | | Guaranteed By Design | - | 80 | - | dB |
| Gain-Bandwidth Product | GBWP | | 15 | - | - | MHz |
| Slew Rate | SR | | - | 6 | - | V/µs |
| **STATE LOGIC** | | | | | | |
| S3# Transition Level | $V_{S3}$ | | - | 1.5 | - | V |
| S5# Transition Level | $V_{S5}$ | | - | 1.5 | - | V |

**Electrical Specifications** Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams and Typical Application Schematics **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PWM CONTROLLER GATE DRIVERS** | | | | | | |
| UGATE and LGATE Source | $I_{GATE}$ | | - | -0.8 | - | A |
| UGATE and LGATE Sink | $I_{GATE}$ | | - | 0.8 | - | A |
| **NCH BACKFEED CONTROL** | | | | | | |
| NCH Current Sink | $I_{NCH}$ | NCH = 0.8V | - | - | 6 | mA |
| NCH Trip Level | $V_{NCH}$ | | 9.0 | 9.5 | 10 | V |
| **VDDQ STANDBY LDO** | | | | | | |
| Output Drive Current | | P5VSBY = 5.0V | - | - | 650 | mA |
| | | P5VSBY = 3.3V | - | - | 550 | mA |
| **VTT REGULATOR** | | | | | | |
| Upper Divider Impedance | $R_U$ | | - | 2.5 | - | kΩ |
| Lower Divider Impedance | $R_L$ | | - | 2.5 | - | kΩ |
| VREF_OUT Buffer Source Current | $I_{VREF\_OUT}$ | | - | - | 2 | mA |
| Maximum $V_{TT}$ Load Current | $I_{VTT\_MAX}$ | Periodic load applied with 30% duty cycle and 10ms period using ISL6532EVAL1 evaluation board (see Application Note AN1055) | -3 | - | 3 | A |
| VTT Over Current Trip | $I_{TRIP\_VTT}$ | By Design | -3.3 | - | 3.3 | A |
| **PGOOD** | | | | | | |
| PGOOD Rising Threshold | $V_{VTTSNS}/V_{VDDQ}$ | S3# & S5# HIGH | - | 57.5 | - | % |
| PGOOD Falling Threshold | $V_{VTTSNS}/V_{VDDQ}$ | S3# & S5# HIGH | - | 45.0 | - | % |
| **PROTECTION** | | | | | | |
| VDDQ OV Level | $V_{FB}/V_{REF}$ | S3# & S5# HIGH | - | 115 | - | % |
| VDDQ UV Level | $V_{FB}/V_{REF}$ | S3# & S5# HIGH | - | 85 | - | % |
| Thermal Shutdown Limit | $T_{SD}$ | By Design | - | 140 | - | °C |

## Functional Pin Description

### 5VSBY (Pin 1)

5VSBY is the bias supply of the ISL6532B. It is typically connected to the 5V standby rail of an ATX power supply. During S4/S5 sleep states the ISL6532B enters a reduced power mode and draws less than 1mA ($I_{CC5}$) from the 5VSBY supply. This pin should be locally bypassed using a 0.1µF capacitor.

### P12V (Pin 18)

P12V provides the gate drive current to the switching MOSFETs of the PWM power stage. The $V_{TT}$ regulation circuit is also powered by P12V. P12V is only required during S0/S1/S2 operation. P12V is typically connected to the +12V rail of an ATX power supply.

### P5VSBY (Pin 8)

This pin provides the $V_{DDQ}$ output power during the S3 sleep state. The regulator is capable of providing standby $V_{DDQ}$ power from either a 5V or 3.3V source.

### GND (Pin 2, 13, 21)

The GND terminals of the ISL6532B provide the return path for the $V_{TT}$ LDO, Standby LDO and switching MOSFET gate drivers. High ground currents are conducted directly through the exposed paddle of the QFN package which must be electrically connected to the ground plane through a path as low in inductance as possible.

### UGATE (Pin 20)

UGATE drives the upper (control) FET of the $V_{DDQ}$ synchronous buck switching regulator. UGATE is driven between GND and P12V.

### LGATE (Pin 19)

LGATE drives the lower (synchronous) FET of the $V_{DDQ}$ synchronous buck switching regulator. LGATE is driven between GND and P12V.

### FB (Pin 11) and COMP (Pin 12)

The $V_{DDQ}$ switching regulator employs a single voltage control loop. FB is the negative input to the voltage loop error amplifier. The positive input of the error amplifier is connected to a precision 0.8V reference and the output of the error amplifier is connected to the COMP pin. The $V_{DDQ}$ output voltage is set by an external resistor divider connected to FB. With a properly selected divider, $V_{DDQ}$ can be set to any voltage between the power rail (reduced by converter losses) and the 0.8V reference. Loop compensation is achieved by connecting an AC network across COMP and FB.

The FB pin is also monitored for under and over-voltage events.

### VDDQ (Pins 5, 6)

The $V_{DDQ}$ pins should be connected externally together to the regulated $V_{DDQ}$ output. During S0/S1 states, the $V_{DDQ}$ pins serve as inputs to the $V_{TT}$ regulator and to the $V_{TT}$ Reference precision divider. During S3 (Suspend to RAM) state, the $V_{DDQ}$ pins serve as an output from the integrated standby LDO.

### VTT (Pins 3, 4)

The VTT pins should be connected together. During S0/S1 states, the VTT pins serve as the outputs of the $V_{TT}$ linear regulator. During any sleep state, the $V_{TT}$ regulator is disabled.

### VTTSNS (Pin 7)

VTTSNS is used as the feedback for control of the $V_{TT}$ linear regulator. Connect this pin to the $V_{TT}$ output at the physical point of desired regulation.

### VREF_OUT (Pin 9)

VREF_OUT is a buffered version of $V_{TT}$ and also acts as the reference voltage for the $V_{TT}$ linear regulator. It is recommended that a minimum capacitance of 0.1µF be connected between $V_{DDQ}$ and VREF_OUT and also between VREF_OUT and GND for proper operation.

### VREF_IN (Pin 10)

A capacitor, $C_{SS}$, connected between VREF_IN and ground is required. This capacitor and the parallel combination of the Upper and Lower Divider Impedance ($R_U||R_L$), sets the time constant for the start up ramp when transitioning from S3 to S0/S1/S2.

The minimum value for $C_{SS}$ can be found through the following equation:

$$C_{SS} > \frac{C_{VTTOUT} \cdot V_{DDQ}}{10 \cdot 2A \cdot R_U \| R_L}$$

The calculated capacitance, $C_{SS}$, will charge the output capacitor bank on the $V_{TT}$ rail in a controlled manner without reaching the current limit of the $V_{TT}$ LDO.

### NCH (Pin 15)

NCH is an open-drain output that controls the MOSFET blocking backfeed from $V_{DDQ}$ to the input rail during sleep states. A 2kΩ or larger resistor is to be tied between the 12V rail and the NCH pin. Until the voltage on the NCH pin reaches the NCH trip level, the PWM is disabled.

If NCH is not actively utilized, it still must be tied to the 12V rail through a resistor. For systems using 5V dual as the input to the switching regulator, a time constant, in the form of a capacitor, can be added to the NCH pad to delay start of the PWM switcher until the 5V dual has switched from 5VSBY to 5VATX.

### PGOOD (Power Good) (Pin 14)

Power Good is an open-drain logic output that changes to a logic low if the $V_{TT}$ regulator is out of regulation in S0/S1/S2 state. PGOOD will always be low in any state other than S0/S1/S2.

### S5# (Pin 17)

This pin accepts the SLP_S5# sleep state signal.

### S3# (Pin 16)

This pin accepts the SLP_S3# sleep state signal.

## Functional Description

### Overview

The ISL6532B provides complete control, drive, protection and ACPI compliance for a regulator powering DDR memory systems. It is primarily designed for computer applications powered from an ATX power supply. A 250kHz Synchronous Buck Regulator with a precision 0.8V reference provides the proper Core voltage to the system memory of the computer. An internal LDO regulator with the ability to both sink and source current and an externally available buffered reference that tracks the $V_{DDQ}$ output by 50% provides the $V_{TT}$ termination voltage.

ACPI compliance is realized through the SLP_S3 and SLP_S5 sleep signals and through monitoring of the 12V ATX bus.

### Initialization

The ISL6532B automatically initializes upon receipt of input power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input bias supply voltages. The POR monitors the bias voltage at the 5VSBY and P12V pins. The POR function initiates soft-start operation after the bias supply voltages exceed their POR thresholds.

## ACPI State Transitions

### Cold Start (S5/S4 to S0 Transition)

At the onset of a mechanical start, the ISL6532B receives it's bias voltage from the 5V Standby bus (5VSBY). As soon as the SLP_S3 and SLP_S5 signals have transitioned HIGH, the ISL6532B starts an internal counter. Following a cold start or any subsequent S5 state, state transitions are ignored until the system enters S0/S1. None of the regulators will begin the soft start procedure until the 5V Standby bus has exceeded POR, the 12V bus has exceeded POR and $V_{NCH}$ has exceeded the trip level.

Once all of these conditions are met, the PWM error amplifier will first be reset by internally shorting the COMP pin to the FB pin. This reset lasts for 2048 clock cycles which is typically 8.2ms (one clock cycle = $1/f_{OSC}$). The digital soft start sequence will then begin.

The PWM error amplifier reference input is clamped to a level proportional to the soft-start voltage. As the soft-start voltage slews up, the PWM comparator generates PHASE pulses of increasing width that charge the output capacitor(s). The internal $V_{TT}$ LDO will also soft start through the reference that tracks the output of the PWM regulator. The soft start lasts for 2048 clock cycles, which is typically 8.2ms. This method provides a rapid and controlled output voltage rise.

Figure 1 shows the soft start sequence for a typical cold start. Due to the soft start capacitance, $C_{SS}$, on the VREF_IN pin, the S5 to S0 transition profile of the $V_{TT}$ rail will have a more rounded features at the start and end of the soft start whereas the $V_{DDQ}$ profile has distinct starting and ending points to the ramp up.

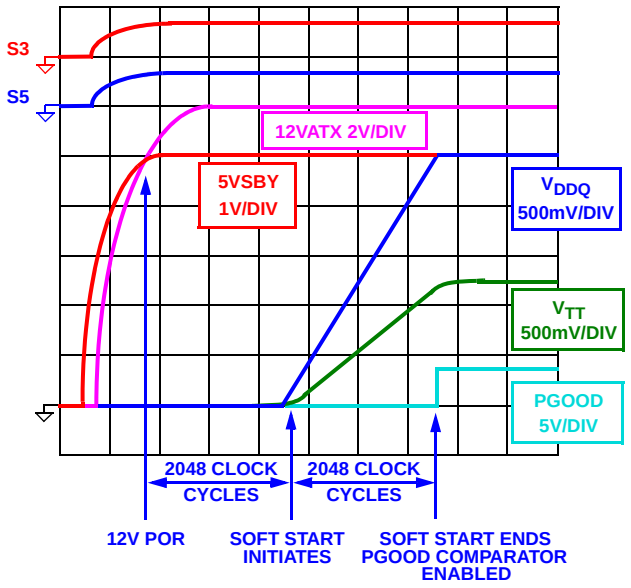



FIGURE 1. TYPICAL COLD START

By directly monitoring 12VATX and the SLP_S3 and SLP_S5 signals, the ISL6532B can achieve PGOOD status significantly faster than other devices that depend on the Latched_Backfeed_Cut signal for timing.

### Active to Sleep (S0 to S3 Transition)

When SLP_S3 goes LOW with SLP_S5 still HIGH, the ISL6532B will disable the $V_{TT}$ linear regulator. The $V_{DDQ}$ standby regulator will be enabled and the $V_{DDQ}$ switching regulator will be disabled. NCH is pulled low to disable the backfeed blocking MOSFET. PGOOD will also transition LOW. When $V_{TT}$ is disabled, the internal reference for the $V_{TT}$ regulator is internally shorted to the $V_{TT}$ rail. This allows the $V_{TT}$ rail to float. When floating, the voltage on the $V_{TT}$ rail will depend on the leakage characteristics of the memory and MCH I/O pins. It is important to note that the $V_{TT}$ rail may not bleed down to 0V.

The $V_{DDQ}$ rail will be supported in the S3 state through the standby $V_{DDQ}$ LDO. When S3 transitions LOW, the Standby regulator is immediately enabled. The switching regulator is disabled synchronous to the switching waveform. The shut off time will range between 4 and 8µs. The standby LDO is capable of supporting up to 650mA of load with P5VSBY tied to the 5V Standby Rail. The standby LDO may receive input from either the 3.3V Standby rail or the 5V Standby rail through the P5VSBY pin. It is recommended that the 5V Standby rail be used as the current delivery capability of the LDO is greater.

### Sleep to Active (S3 to S0 Transition)

When SLP_S3 transitions from LOW to HIGH with SLP_S5 held HIGH and after the 12V rail exceeds POR, the ISL6532B will enable the $V_{DDQ}$ switching regulator, disable the $V_{DDQ}$ standby regulator, enable the $V_{TT}$ LDO and force the NCH pin to a high impedance state turning on the blocking MOSFET. The internal short between the $V_{TT}$ reference and the $V_{TT}$ rail is released. Upon release of the short, the capacitor on VREF_IN is then charged up through the internal resistor divider network. The $V_{TT}$ output will follow this capacitor charge-up, acting as the S3 to S0 transition soft start for the $V_{TT}$ rail. The PGOOD comparator is enabled only after 2048 clock cycles, or typically 8.2ms, have passed following the S3 transition to a HIGH state.

Figure 2 illustrates a typical state transition from S3 to S0. It should be noted that the soft start profile of the $V_{TT}$ LDO output will vary according to the value of the capacitor on the VREF_IN pin.

## Active to Shutdown (S0 to S4/S5 Transition)

When the system transitions from active, S0, state to shutdown, S4/S5, state, the ISL6532B IC disables all regulators and forces the PGOOD pin and the NCH pin LOW.

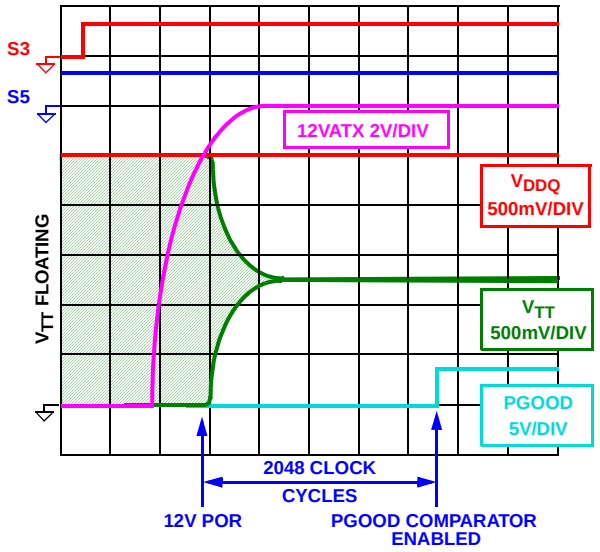



FIGURE 2. TYPICAL S3 TO S0 STATE TRANSITION

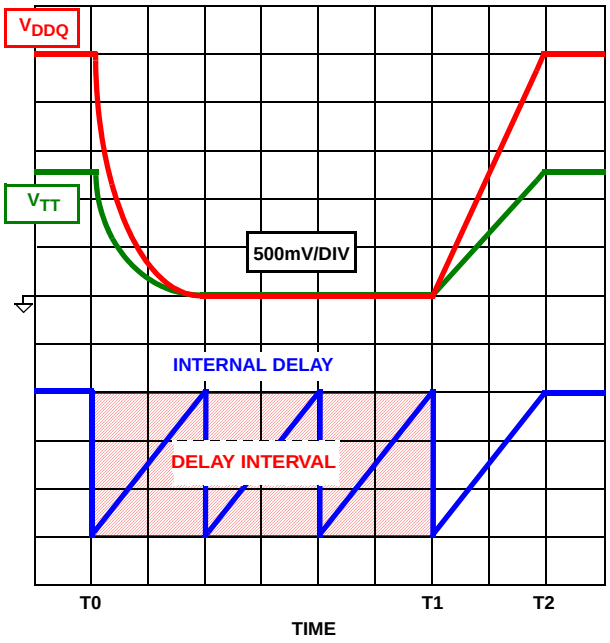



FIGURE 3. $V_{TT}/V_{DDQ}$ LDO UNDER VOLTAGE PROTECTION RESPONSES

### $V_{TT}$ Over Current Protection

The internal $V_{TT}$ LDO is protected from fault conditions through a 3.3A current limit. This current limit protects the ISL6532B if the LDO is sinking or sourcing current. During an overcurrent event on the $V_{TT}$ LDO, only the $V_{TT}$ LDO is disabled. Once the over current condition on the $V_{TT}$ rail is removed, $V_{TT}$ will recover.

### Over/Under Voltage Protection.

Both the internal $V_{TT}$ LDO and the $V_{DDQ}$ regulator are protected from faults through internal Over/Under voltage detection circuitry. If either rail falls below 85% of the targeted voltage, then an undervoltage event is tripped. An under voltage will disable all regulators for a period of 3 soft-start cycles, after which a normal soft-start is initiated. If the output remains under 85% of target, the regulators will continue to be disabled and soft-started in a hiccup mode until the fault is cleared. See Figure 3.

If either rail exceeds 115% of the targeted voltage, then all outputs are immediately disabled. The ISL6532B will not re-enable the outputs until either the bias voltage is toggled in order to initiate a POR or the SLP_S5 signal is forced LOW and then back to HIGH.

### Thermal Protection (S0/S3 State)

If the ISL6532B IC junction temperature reaches a nominal temperature of $140^{o}C$, all regulators will be disabled. The ISL6532B will not re-enable the outputs until the junction temperature drops below $110^{o}C$ and either the bias voltage is toggled in order to initiate a POR or the SLP_S5 signal is forced LOW and then back to HIGH.

### Shoot-Through Protection

A shoot-through condition occurs when both the upper and lower MOSFETs are turned on simultaneously, effectively shorting the input voltage to ground. To protect from a shoot-through condition, the ISL6532B incorporates specialized circuitry which insures that complementary MOSFETs are not ON simultaneously.

The adaptive shoot-through protection utilized by the $V_{DDQ}$ regulator looks at the lower gate drive pin, LGATE, and the upper gate drive pin, UGATE, to determine whether a MOSFET is ON or OFF. If the voltage from UGATE or from LGATE to GND is less than 0.8V, then the respective MOSFET is defined as being OFF and the other MOSFET is allowed to be turned ON. This method allows the $V_{DDQ}$ regulator to both source and sink current.

Since the voltage of the MOSFET gates are being measured to determine the state of the MOSFET, the designer is encouraged to consider the repercussions of introducing external components between the gate drivers and their respective MOSFET gates before actually implementing such measures. Doing so may interfere with the shoot-through protection.

## Application Guidelines

### Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently at 250kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage

spikes can degrade efficiency, radiate noise into the circuit, and lead to device over-voltage stress. Careful component layout and printed circuit board design minimizes these voltage spikes.

As an example, consider the turn-off transition of the upper MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the lower MOSFET. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide traces minimizes the magnitude of voltage spikes.

There are two sets of critical components in the ISL6532B switching converter. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate large amounts of noise. Next are the small signal components which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 4 shows the connections of the critical components in the converter. Note that capacitors $C_{IN}$ and $C_{OUT}$ could each represent numerous physical capacitors. Dedicate one solid layer, usually a middle layer of the PC board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the GATE pins to the MOSFET gates should be kept short and wide enough to easily handle the 1A of drive current.

In order to dissipate heat generated by the internal $V_{TT}$ LDO, the ground pad, pin 21, should be connected to the internal ground plane through at least four vias. This allows the heat to move away from the IC and also ties the pad to the ground plane through a low impedance path.

The switching components should be placed close to the ISL6532B first. Minimize the length of the connections between the input capacitors, $C_{IN}$, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Position the output inductor and output capacitors between the upper and lower MOSFETs and the load.

The critical small signal components include any bypass capacitors, feedback components, and compensation components. Place the PWM converter compensation components close to the FB and COMP pins. The feedback resistors should be located as close as possible to the FB pin with vias tied straight to the ground plane as required.

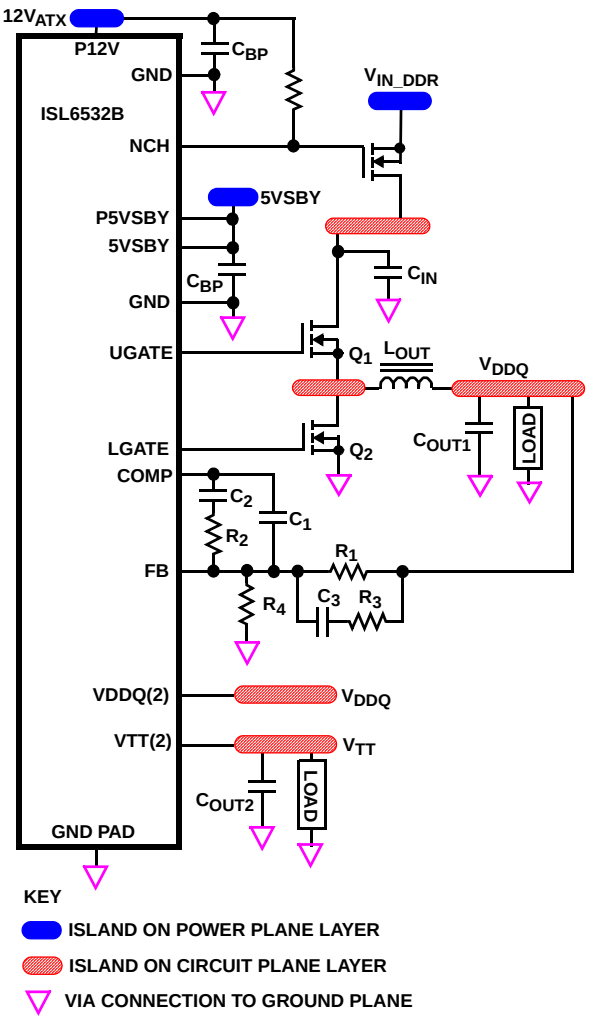



**FIGURE 4. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS**

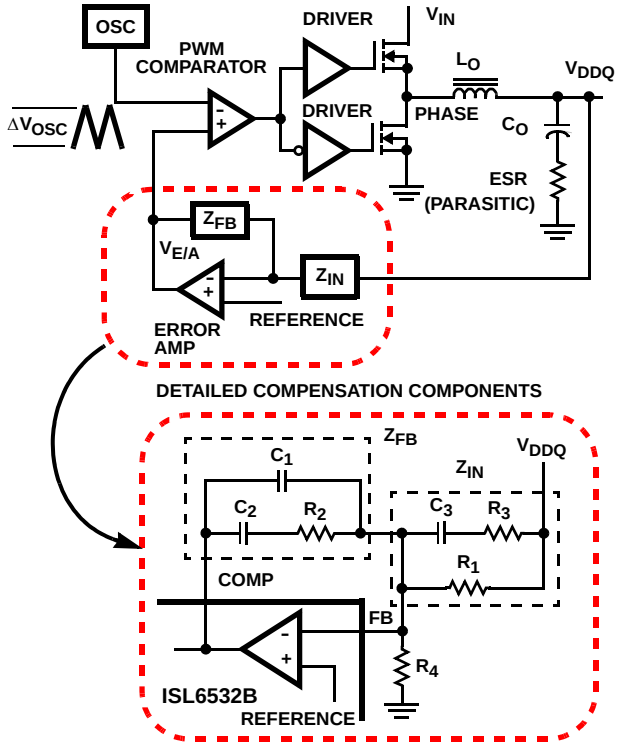
### *Feedback Compensation - PWM Buck Converter*

Figure 5 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage ($V_{OUT}$) is regulated to the Reference voltage level. The error amplifier output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of $V_{IN}$ at the PHASE node. The PWM wave is smoothed by the output filter ($L_O$ and $C_O$).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter ($L_O$ and $C_O$), with a double pole break frequency at $F_{LC}$ and a zero at $F_{ESR}$. The DC Gain of the modulator is simply the input voltage ($V_{IN}$) divided by the peak-to-peak oscillator voltage $\Delta V_{OSC}$.

### *Modulator Break Frequency Equations*

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O}$$




$$V_{DDQ} = 0.8 \times \left(1 + \frac{R_1}{R_4}\right)$$

**FIGURE 5. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN AND OUTPUT VOLTAGE SELECTION**

The compensation network consists of the error amplifier (internal to the ISL6532B) and the impedance networks $Z_{IN}$ and $Z_{FB}$. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency ($f_{0dB}$) and adequate phase margin. Phase margin is the difference between the closed loop phase at $f_{0dB}$ and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components ($R_1$, $R_2$, $R_3$, $C_1$, $C_2$, and $C_3$) in Figure 5. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain ($R_2/R_1$) for desired converter bandwidth.
2. Place 1$^{ST}$ Zero Below Filter's Double Pole (~75% $F_{LC}$).
3. Place 2$^{ND}$ Zero at Filter's Double Pole.
4. Place 1$^{ST}$ Pole at the ESR Zero.
5. Place 2$^{ND}$ Pole at Half the Switching Frequency.
6. Check Gain against Error Amplifier's Open-Loop Gain.
7. Estimate Phase Margin - Repeat if Necessary.

### Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R_2 \times C_2} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \qquad F_{P2} = \frac{1}{2\pi \times R_3 \times C_3}$$

Figure 6 shows an asymptotic plot of the DC-DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 6. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at FP2 with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the graph of Figure 6 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks $Z_{FB}$ and $Z_{IN}$ to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

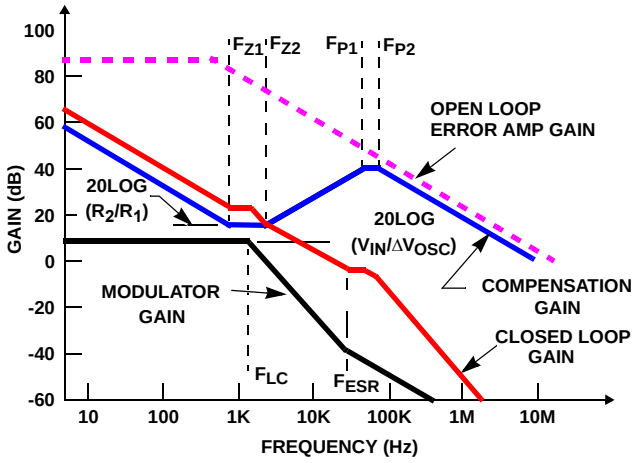



**FIGURE 6. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN**

### Output Voltage Selection

The output voltage of the VDDQ PWM converter can be programmed to any level between VIN and the internal reference, 0.8V. An external resistor divider is used to scale the output voltage relative to the reference voltage and feed it back to the inverting input of the error amplifier, see Figure 6.

However, since the value of R1 affects the values of the rest of the compensation components, it is advisable to keep its value less than 5kΩ. Depending on the value chosen for R1, R4 can be calculated based on the following equation:

$$R4 = \frac{R1 \times 0.8V}{V_{DDQ} - 0.8V}$$

If the output voltage desired is 0.8V, simply route $V_{DDQ}$ back to the FB pin through R1, but do not populate R4.

The output voltage for the internal $V_{TT}$ linear regulator is set internal to the ISL6532B to track the $V_{DDQ}$ voltage by 50%. There is no need for external programming resistors.

## Component Selection Guidelines

### Output Capacitor Selection - PWM Buck Converter

An output capacitor is required to filter the inductor current and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

DDR memory systems are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

### Output Capacitor Selection - LDO Regulator

The output capacitors used in LDO regulators are used to provide dynamic load current. The amount of capacitance and type of capacitor should be chosen with this criteria in mind.

### Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6532B will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}}$$

where: $I_{TRAN}$ is the transient load current step, $t_{RISE}$ is the response time to the application of load, and $t_{FALL}$ is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

### Input Capacitor Selection - PWM Buck Converter

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time the upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs, between the drain of upper MOSFET and the source of lower MOSFET.

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a conservative guideline. For worst cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC output load current.

The maximum RMS current required by the regulator may be closely approximated through the following equation:

$$I_{RMS_{MAX}} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left( {I_{OUT_{MAX}}}^2 + \frac{1}{12} \times \left( \frac{V_{IN} - V_{OUT}}{L \times f_{sw}} \times \frac{V_{OUT}}{V_{IN}} \right)^2 \right)}$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

### *MOSFET Selection - PWM Buck Converter*

The ISL6532B requires 2 N-Channel power MOSFETs for switching power and a third MOSFET to block backfeed from $V_{DDQ}$ to the Input in S3 Mode. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor. The switching losses seen when sourcing current will be different from the switching losses seen when sinking current. When sourcing current, the upper MOSFET realizes most of the switching losses. The lower switch realizes most of the switching losses when the converter is sinking current (see the equations below). These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the upper and lower MOSFET's body diode. The gate-charge losses are dissipated in part by the ISL6532B and do not significantly heat the MOSFETs. However, large gate-charge increases the switching interval, tSW which increases the MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

Approximate Losses while Sourcing current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times f_s$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D)$$

Approximate Losses while Sinking current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D) + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times f_s$$

Where: D is the duty cycle = $V_{OUT}$ / $V_{IN}$,
$t_{SW}$ is the combined switch ON and OFF time, and
$f_s$ is the switching frequency.

## ISL6532B Application Circuit

Figure 7 shows an application circuit utilizing the ISL6532B. Detailed information on the circuit, including a complete Bill-of-Materials and circuit board description, can be found in Application Note AN1055.

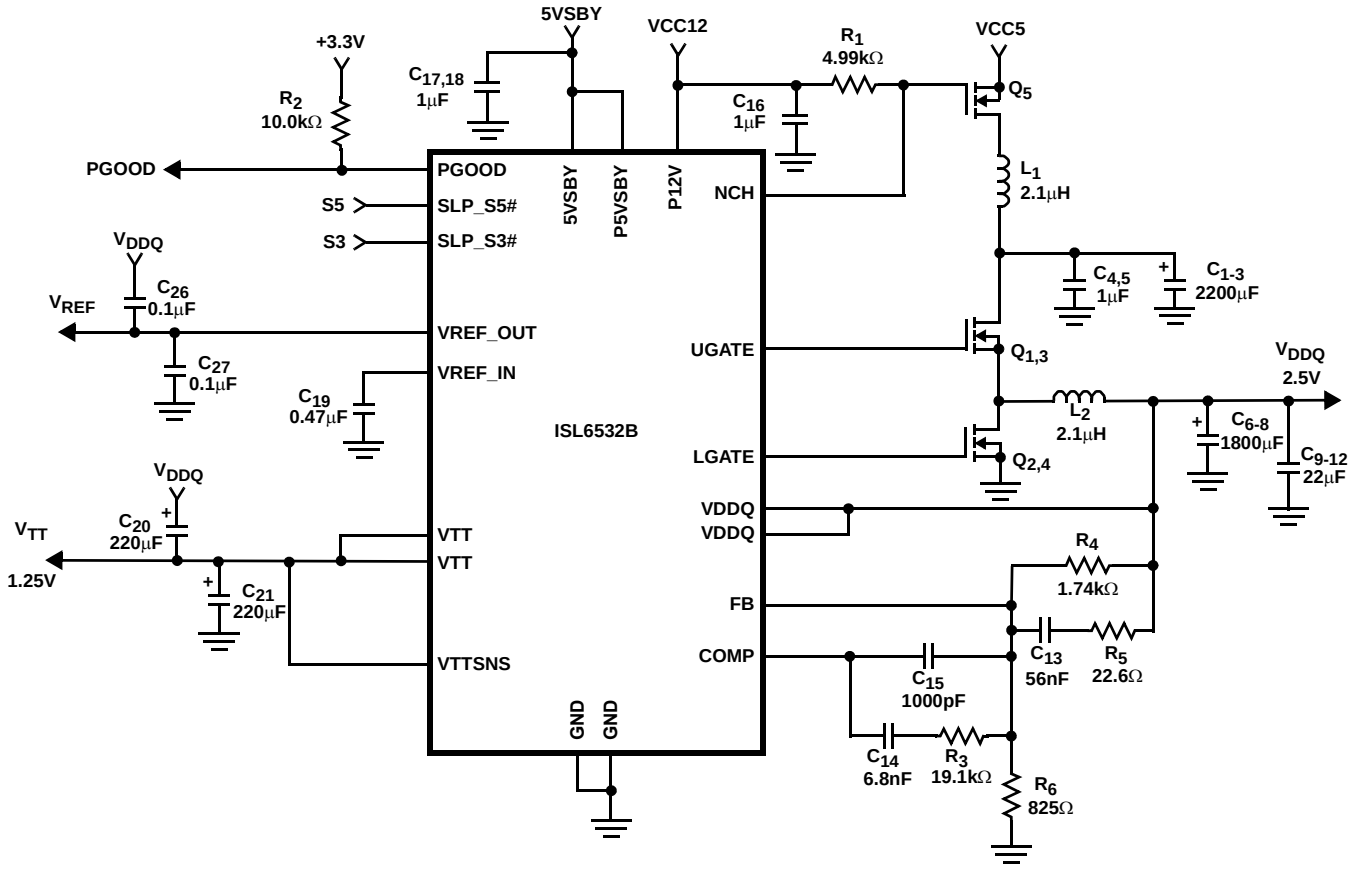
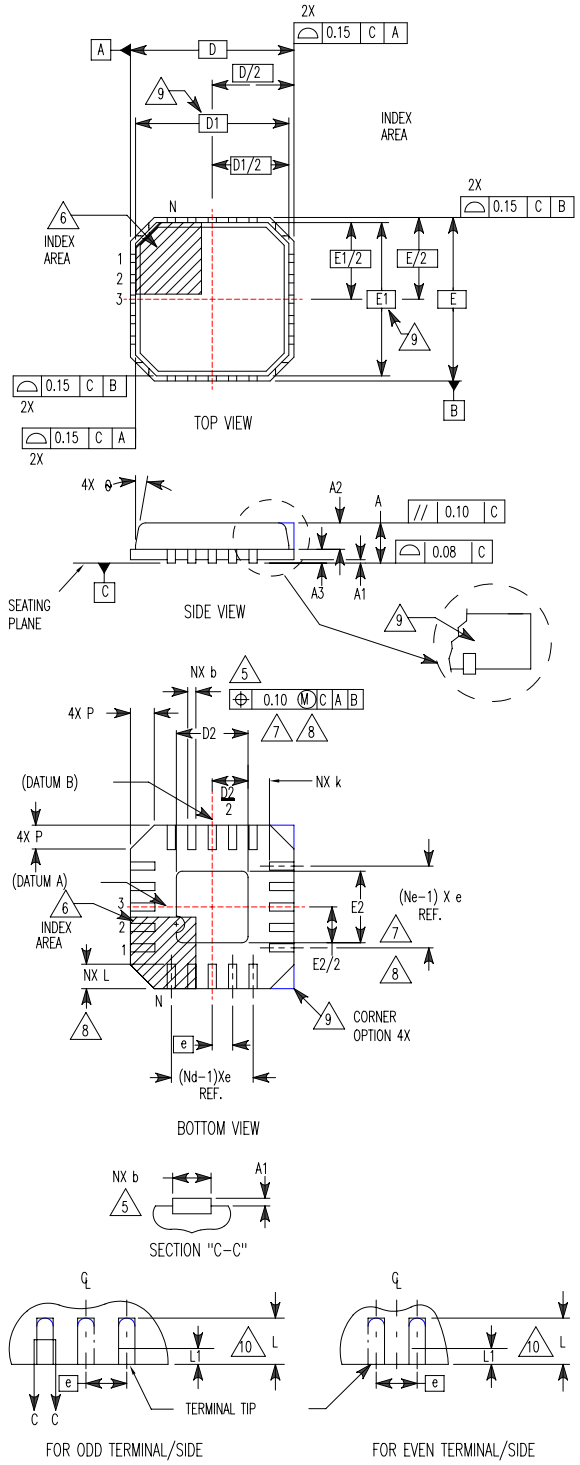



**FIGURE 7. DDR SDRAM AND AGP VOLTAGE REGULATOR USING THE ISL6532B**

## Quad Flat No-Lead Plastic Package (QFN)
## Micro Lead Frame Plastic Package (MLFP)




## L20.6x6

**20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VJJB ISSUE C)**

| SYMBOL | MILLIMETERS | | | NOTES |
|---|---|---|---|---|
| | MIN | NOMINAL | MAX | |
| A | 0.80 | 0.90 | 1.00 | - |
| A1 | - | - | 0.05 | - |
| A2 | - | - | 1.00 | 9 |
| A3 | | 0.20 REF | | 9 |
| b | 0.28 | 0.33 | 0.40 | 5, 8 |
| D | | 6.00 BSC | | - |
| D1 | | 5.75 BSC | | 9 |
| D2 | 3.55 | 3.70 | 3.85 | 7, 8 |
| E | | 6.00 BSC | | - |
| E1 | | 5.75 BSC | | 9 |
| E2 | 3.55 | 3.70 | 3.85 | 7, 8 |
| e | | 0.80 BSC | | - |
| k | 0.25 | - | - | - |
| L | 0.35 | 0.60 | 0.75 | 8 |
| L1 | - | - | 0.15 | 10 |
| N | | 20 | | 2 |
| Nd | | 5 | | 3 |
| Ne | | 5 | | 3 |
| P | - | - | 0.60 | 9 |
| θ | - | - | 12 | 9 |

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.