DATA SHEET

BF998; BF998R
Silicon N-channel dual-gate MOS-FETs

Product specification
Supersedes data of April 1991

1996 Aug 01

Silicon N-channel dual-gate MOS-FETs BF998; BF998R

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.

APPLICATIONS

- VHF and UHF applications with 12 V supply voltage, such as television tuners and professional communications equipment.

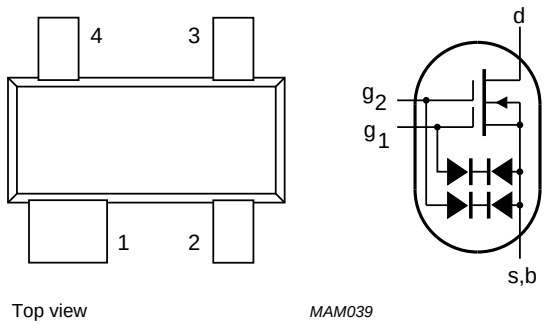
DESCRIPTION

Depletion type field effect transistor in a plastic microminiature SOT143B or SOT143R package with source and substrate interconnected. The transistors are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

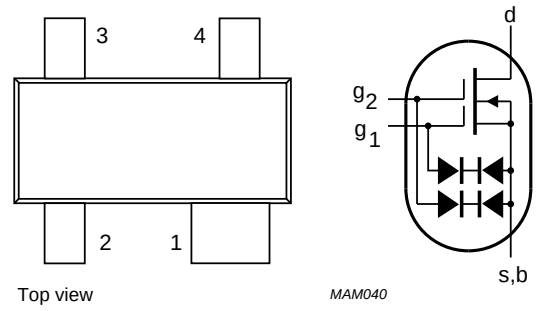
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MOp.

Fig.1 Simplified outline (SOT143B) and symbol; BF998.



Marking code: MO$\overline{p}$.

Fig.2 Simplified outline (SOT143R) and symbol; BF998R.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	30	mA
P_{tot}	total power dissipation		–	200	mW
$\lvert y_{fs} \rvert$	forward transfer admittance		24	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		2.1	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	25	–	fF
F	noise figure	f = 800 MHz	1	–	dB
T_j	operating junction temperature		–	150	°C

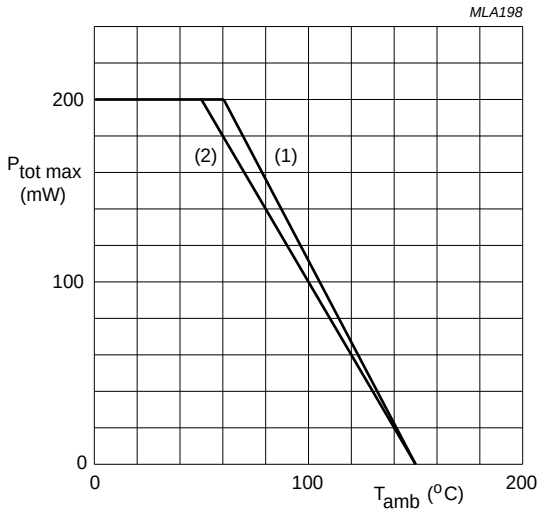
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	30	mA
$\pm I_{G1}$	gate 1 current		–	10	mA
$\pm I_{G2}$	gate 2 current		–	10	mA
P_{tot}	total power dissipation; BF998	up to T_{amb} = 60 °C; see Fig.3; note 1	–	200	mW
		up to T_{amb} = 50 °C; see Fig.3; note 2	–	200	mW
P_{tot}	total power dissipation; BF998R	up to T_{amb} = 50 °C; see Fig.4; note 1	–	200	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	150	°C

Notes

1. Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.
2. Device mounted on a printed-circuit board.



(1) Ceramic substrate.
(2) Printed-circuit board.

Fig.3 Power derating curves; BF998.

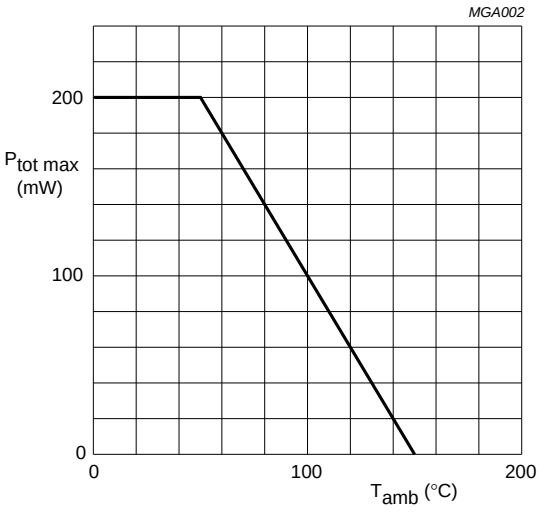


Fig.4 Power derating curve; BF998R.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air; BF998	note 1	460	K/W
		note 2	500	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air; BF998R	note 1	500	K/W

Notes

1. Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.
2. Device mounted on a printed-circuit board.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}SS}$ = ±10 mA	6	20	V
$\pm V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}SS}$ = ±10 mA	6	20	V
$-V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; I_D = 20 μA	–	2.0	V
$-V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$V_{G1\text{-}S}$ = 0; V_{DS} = 8 V; I_D = 20 μA	–	1.5	V
I_{DSS}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0; note 1	2	18	mA
$\pm I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = ±5 V	–	50	nA
$\pm I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = ±5 V	–	50	nA

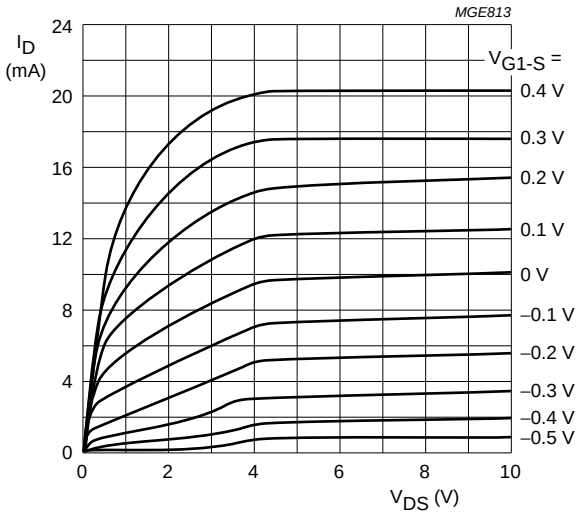
Note

1. Measured under pulse condition.

DYNAMIC CHARACTERISTICS

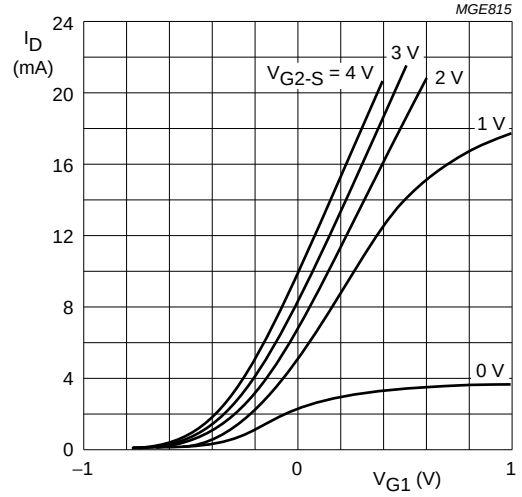
Common source; T_{amb} = 25 °C; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	f = 1 kHz	21	24	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.1	2.5	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{os}	output capacitance	f = 1 MHz	–	1.05	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}	–	0.6	–	dB
		f = 800 MHz; G_S = 3.3 mS; B_S = B_{Sopt}	–	1.0	–	dB



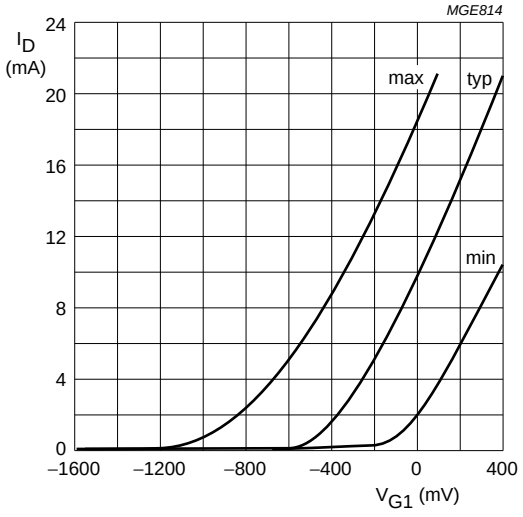
V_{G2-S} = 4 V; T_{amb} = 25 °C.

Fig.5 Output characteristics; typical values.



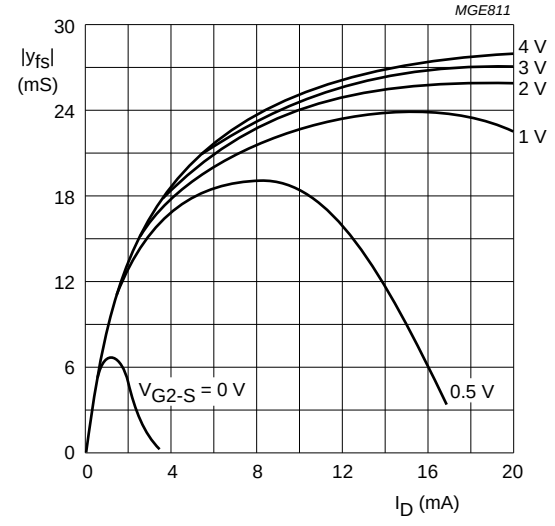
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.6 Transfer characteristics; typical values.



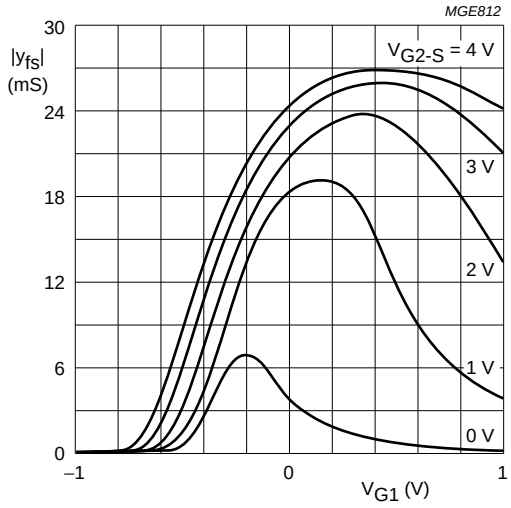
V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

Fig.7 Drain current as a function of gate 1 voltage; typical values.



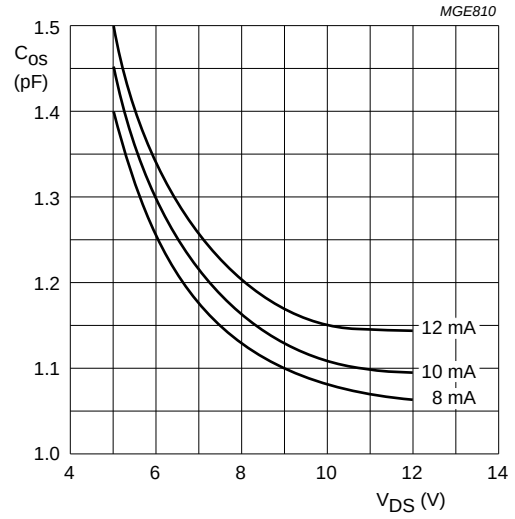
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.8 Forward transfer admittance as a function of drain current; typical values.



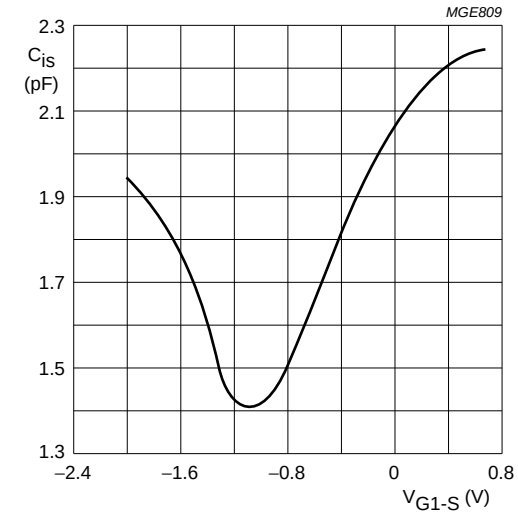
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.9 Forward transfer admittance as a function of gate 1 voltage; typical values.



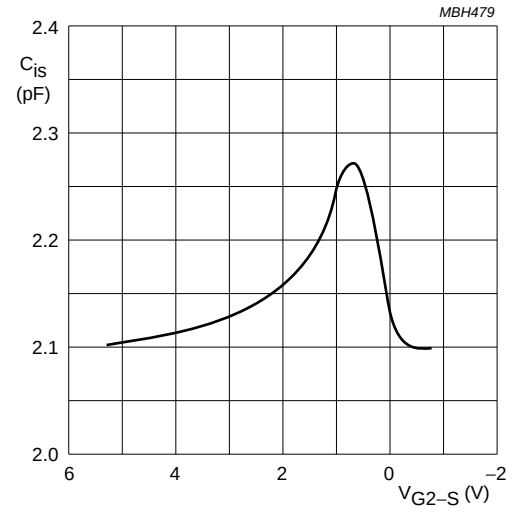
V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.10 Output capacitance as a function of drain-source voltage; typical values.



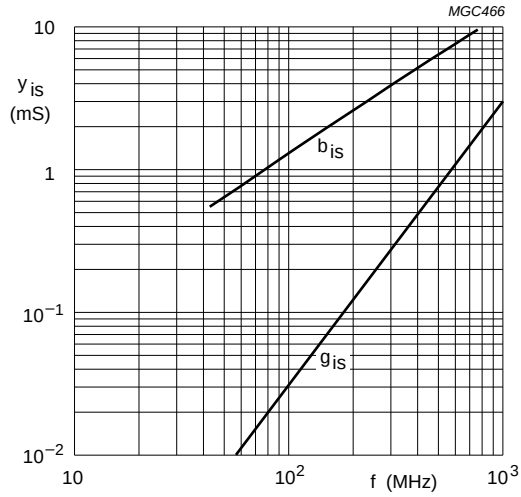
V_{DS} = 8 V; V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.11 Gate 1 input capacitance as a function of gate 1-source voltage; typical values.



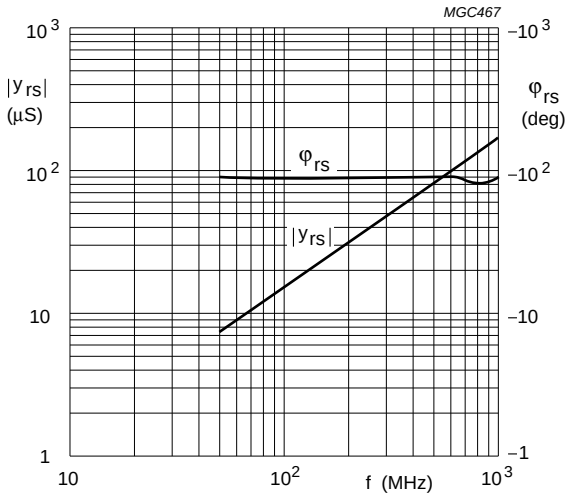
V_{DS} = 8 V; V_{G1-S} = 0 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.12 Gate 1 input capacitance as a function of gate 2-source voltage; typical values.



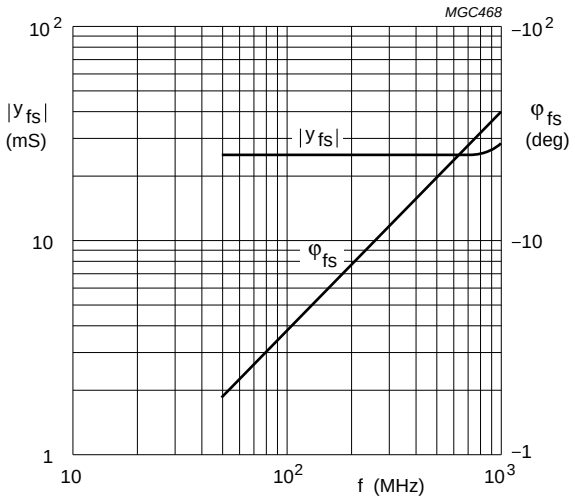
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.13 Input admittance as a function of the frequency; typical values.



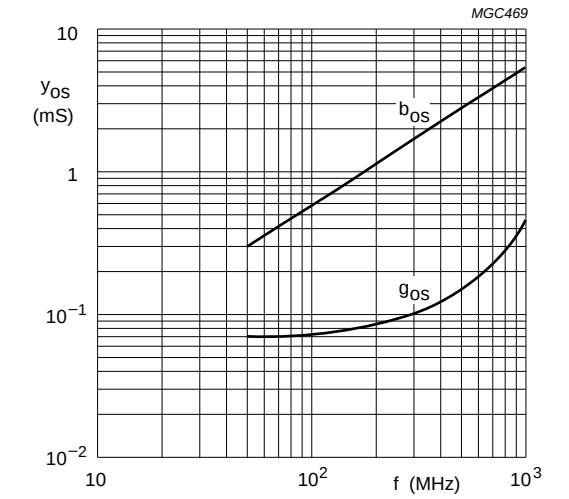
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.14 Reverse transfer admittance and phase as a function of frequency; typical values.



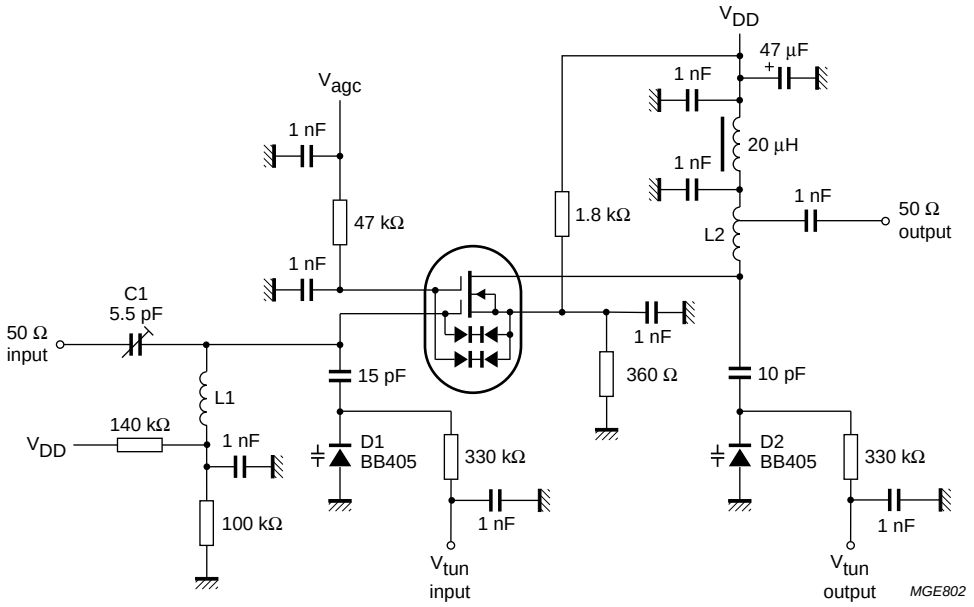
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.15 Forward transfer admittance and phase as a function of frequency; typical values.



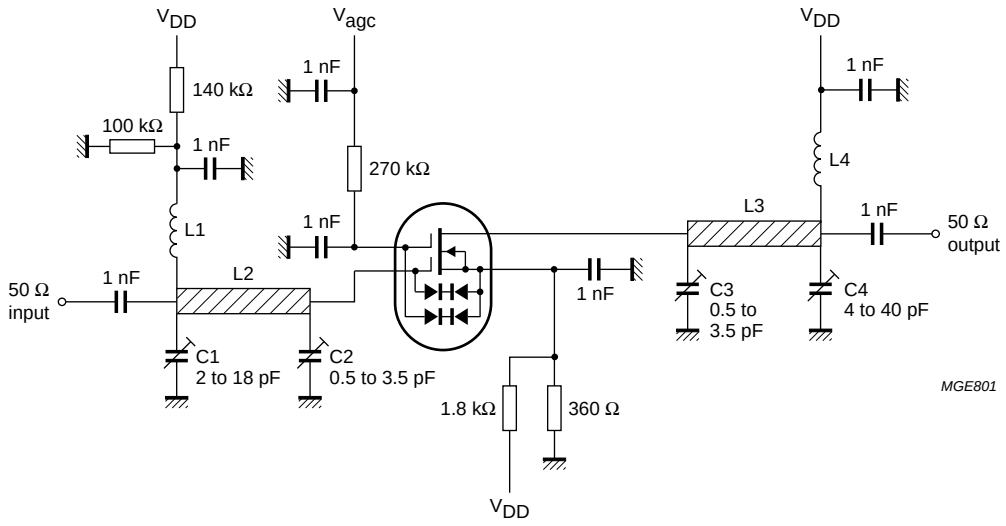
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.16 Output admittance as a function of the frequency; typical values.



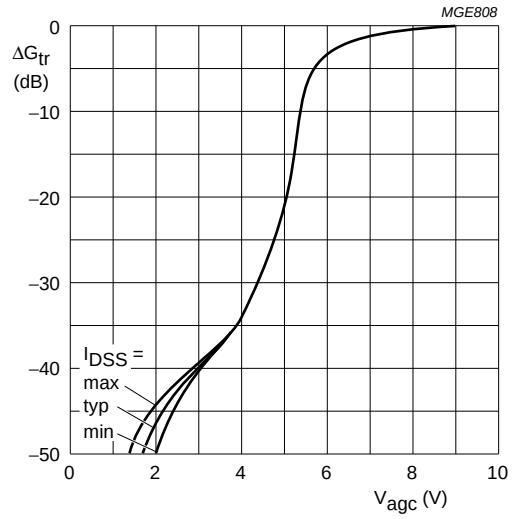
V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.
L1 = 45 nH; 4 turns 0.8 mm copper wire, internal diameter 4 mm.
L2 = 160 nH; 3 turns 0.8 mm copper wire, internal diameter 8 mm.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS. C1 adjusted for G_S = 2 mS.

Fig.17 Gain control test circuit at f = 200 MHz.



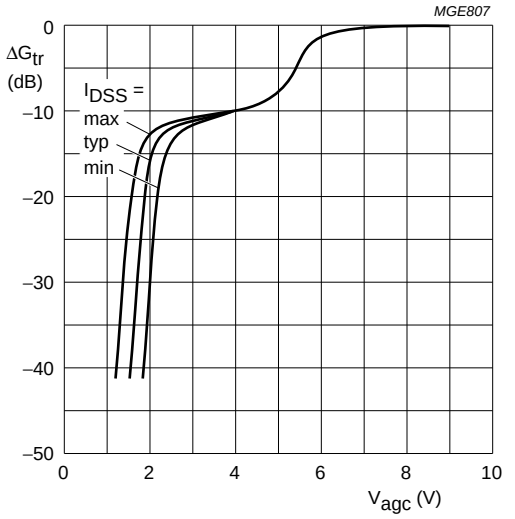
V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.
L1 = L4 = 200 nH; 11 turns 0.5 mm copper wire, without spacing, internal diameter 3 mm.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.18 Gain control test circuit at f = 800 MHz.



V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

Fig.19 Automatic gain control characteristics measured in circuit of Fig.17.

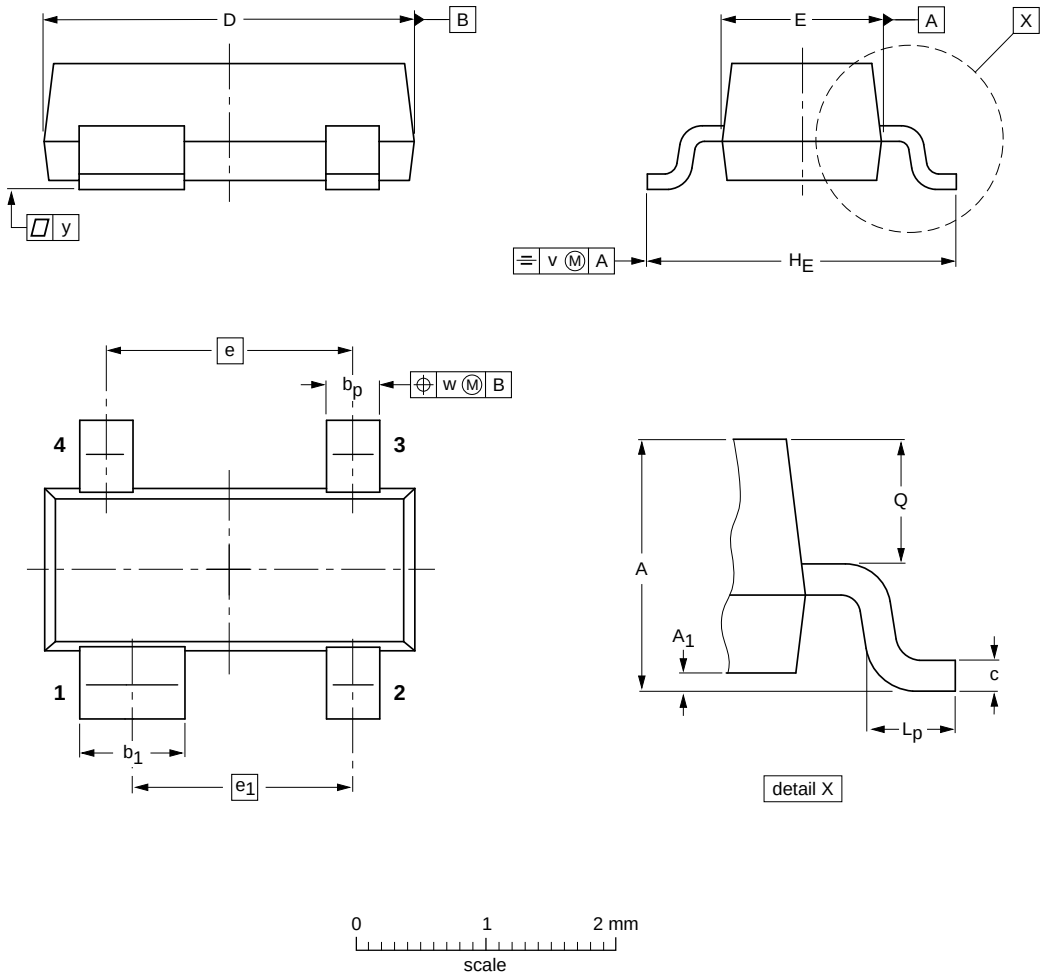


V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

Fig.20 Automatic gain control characteristics measured in circuit of Fig.18.

PACKAGE OUTLINES

Plastic surface-mounted package; 4 leads **SOT143B**

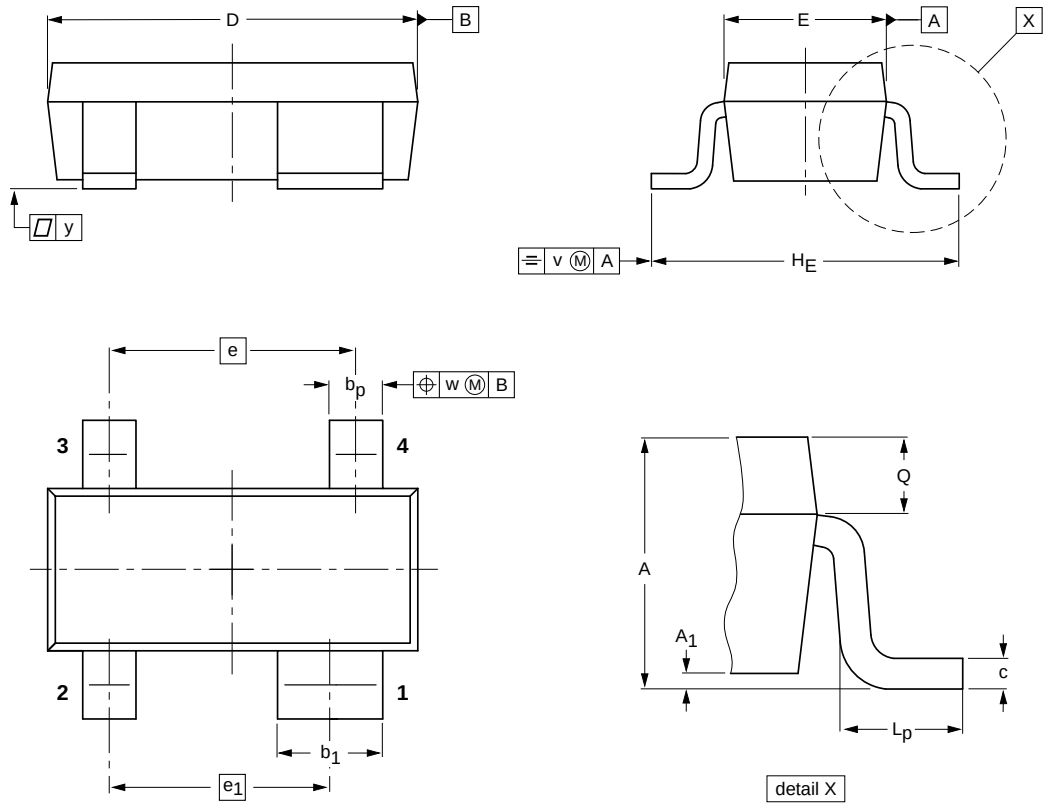


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143B						~~04-11-16~~ 06-03-16

Plastic surface-mounted package; reverse pinning; 4 leads **SOT143R**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143R			SC-61AA			~~04-11-16~~ 06-03-16

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

DEFINITIONS

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

DISCLAIMERS

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

NXP Semiconductors

provides High Performance Mixed Signal and Standard Product solutions that leverage its leading RF, Analog, Power Management, Interface, Security and Digital Processing expertise

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: **http://www.nxp.com**
For sales offices addresses send e-mail to: **salesaddresses@nxp.com**

Printed in The Netherlands R77/02/pp15 Date of release:1996 Aug 01