PE29102

Document Category: Product Specification

UltraCMOS® High-speed FET Driver, 40 MHz

Features

- High- and Low-side FET drivers
- Dead-time control
- Fast propagation delay, 9 ns
- Tri-state enable mode
- Sub-nanosecond rise and fall time
- 2A/4A peak source/sink current
- Package – Flip chip

Applications

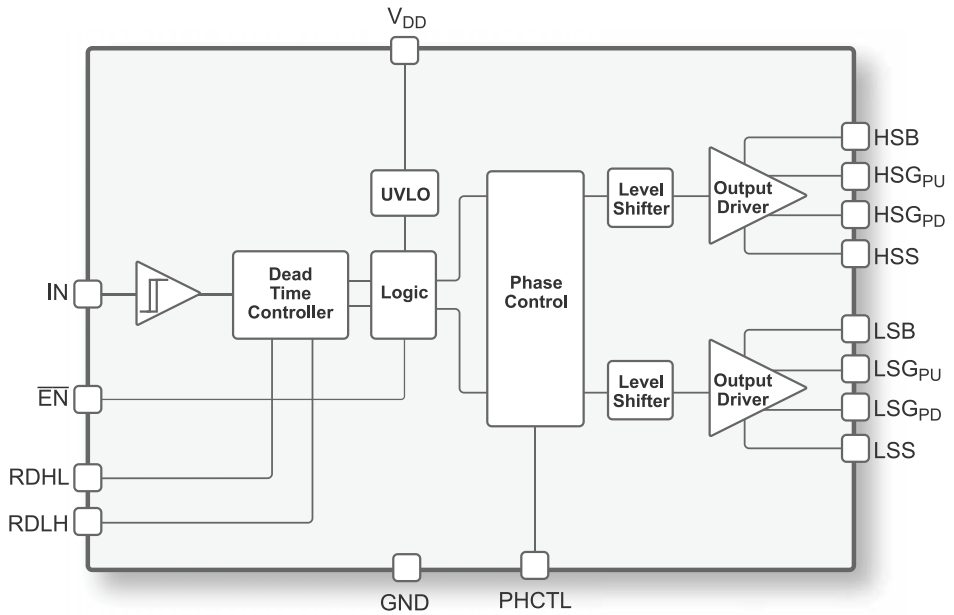
- Class D audio
- DC–DC / AC–DC converters
- Wireless charging
- Envelope tracking
- LiDAR

Product Description

The PE29102 is an integrated high-speed driver designed to control the gates of external power devices, such as enhancement mode gallium nitride (GaN) FETs. The outputs of the PE29102 are capable of providing switching transition speeds in the sub-nanosecond range for switching applications up to 40 MHz. The PE29102 is optimized for matched dead time and offers best-in-class propagation delay to improve system bandwidth. High switching speeds result in smaller peripheral components and enable innovative designs for applications such as class D audio and wireless charging. The PE29102 is available in a flip chip package.

The PE29102 is manufactured on Peregrine's UltraCMOS process, a patented advanced form of silicon-on-insulator (SOI) technology, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1 • *PE29102 Functional Diagram*



Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE29102*

Parameter/Condition	Min	Max	Unit
Low-side bias (LSB) to low-side source (LSS)	–0.3	7	V
High-side bias (HSB) to high-side source (HSS)	–0.3	7	V
Input signal	–0.3	7	V
HSS to LSS	–1	100	V
ESD voltage HBM(*), all pins		500	V

Note: * Human body model (JEDEC JS–001, Table 2A).

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the PE29102. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Recommended Operating Conditions for PE29102*

Parameter	Min	Typ	Max	Unit
Supply for driver front-end, V_{DD}	4.0	5.0	6.0	V
Supply for high-side driver, HSB	4.0	5.0	6.0	V
Supply for low-side driver, LSB	4.0	5.0	6.0	V
HIGH level input voltage, VIH	1.6		6.0	V
LOW level input voltage, VIL	0		0.6	V
HSS range	0		60	V
Operating temperature	–40		+105	°C
Junction temperature	–40		+125	°C

Electrical Specifications

Table 3 provides the key electrical specifications @ +25 °C, V_{DD} = 5V, 100 pF load, HSB and LSB bootstrap diode included unless otherwise specified.

Table 3 • *DC Characteristics*

Parameter	Condition	Min	Typ	Max	Unit
DC Characteristics					
V_{DD} quiescent current	V_{DD} = 5V		1.3		mA
HSB quiescent current	V_{DD} = 5V		2.7		mA
LSB quiescent current	V_{DD} = 5V		2.7		mA
Total quiescent current	V_{DD} = 5V		6.7	9.0	mA
V_{DD} quiescent current	V_{DD} = 6V		1.6		mA
HSB quiescent current	V_{DD} = 6V		3.6		mA
LSB quiescent current	V_{DD} = 6V		3.6		mA
Total quiescent current	V_{DD} = 6V		9.0	11.6	mA
Under Voltage Lockout					
Under voltage release (rising)			3.6	3.8	V
Under voltage hysteresis			400		mV
Gate Drivers					
HSG_{PU}/LSG_{PU} pull-up resistance			1.9		Ω
HSG_{PD}/LSG_{PD} pull-down resistance			1.3		Ω
HSG_{PU}/LSG_{PU} leakage current	HSB–HSG_{PU} = 5V, LSB–LSG_{PU} = 5V		10		µA
HSG_{PD}/LSG_{PD} leakage current	HSG_{PD}–HSS = 5V, LSG_{PD}–LSS = 5V		10		µA

Table 3 • *DC Characteristics (Cont.)*

Parameter	Condition	Min	Typ	Max	Unit
Dead-time Control					
Dead-time control voltages	80 kΩ resistor to GND		1.3		V
Dead-time from HSG going low to LSG going high	RDHL = 30 kΩ		1.9		ns
	RDHL = 80.6 kΩ		7.0		ns
	RDHL = 150 kΩ		13.6		ns
	RDHL = 255 kΩ		23.5		ns
Dead-time from LSG going low to HSG going high	RDLH = 30 kΩ		1.8		ns
	RDLH = 80.6 kΩ		6.7		ns
	RDLH = 150 kΩ		13.2		ns
	RDLH = 255 kΩ		22.7		ns
Switching Characteristics					
LSG turn-off propagation delay	At min dead time		9.1		ns
HSG rise time	10 - 90% with 100pF load		0.9		ns
LSG rise time	10 - 90% with 100pF load		0.9		ns
HSG fall time	90 - 10% with 100pF load		0.8		ns
LSG fall time	90 - 10% with 100pF load		0.9		ns
Minimum output pulse width			2.8	5.0	ns
Max switching frequency @ 50% duty cycle	RDHL = RDLH = 80 kΩ	40			MHz

Control Logic

Table 4 provides the control logic truth table for the PE29102.

Table 4 • *Truth Table for PE29102*

$\overline{EN}$	IN	HSG_{PU}–HSS	HSG_{PD}–HSS	LSG_{PU}–LSS	LSG_{PD}–LSS
L	L	Hi–Z	L	H	Hi–Z
L	H	H	Hi–Z	Hi–Z	L
H	L	Hi–Z	L	Hi–Z	L
H	H	Hi–Z	L	Hi–Z	L

Typical Performance Data

Figure 2 through **Figure 4** show the typical performance data @ +25 °C, V_{DD} = 5V, load = 2.2Ω resistor in series with 100 pF capacitor, HSB and LSB bootstrap diode included, unless otherwise specified.

Figure 2 • ***Total Quiescent Current (mA)***

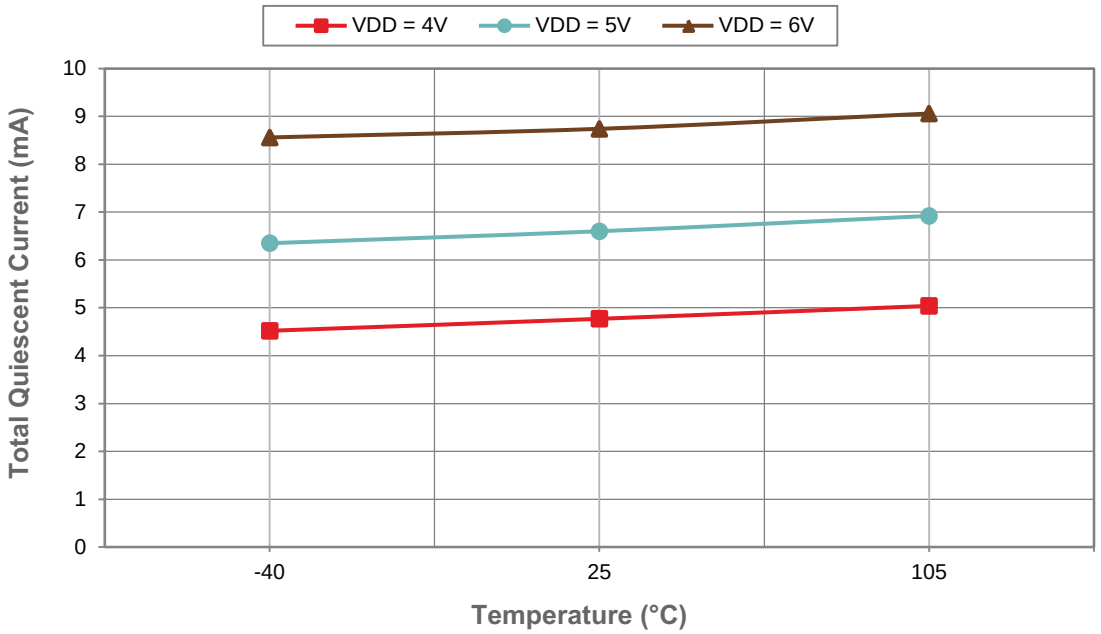


Figure 3 • *UVLO Threshold (V)*

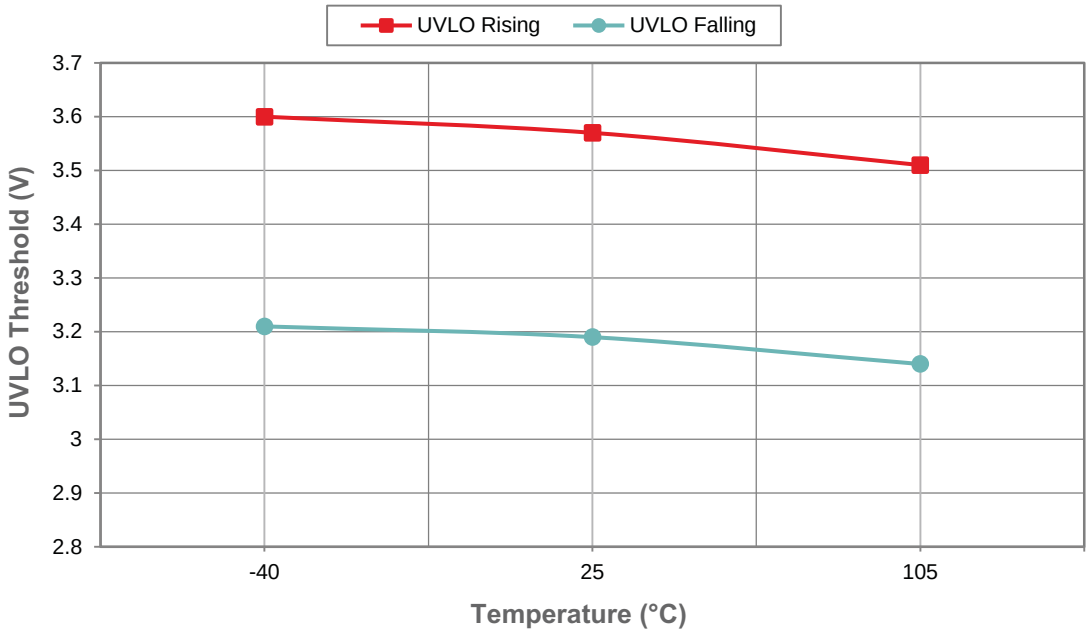
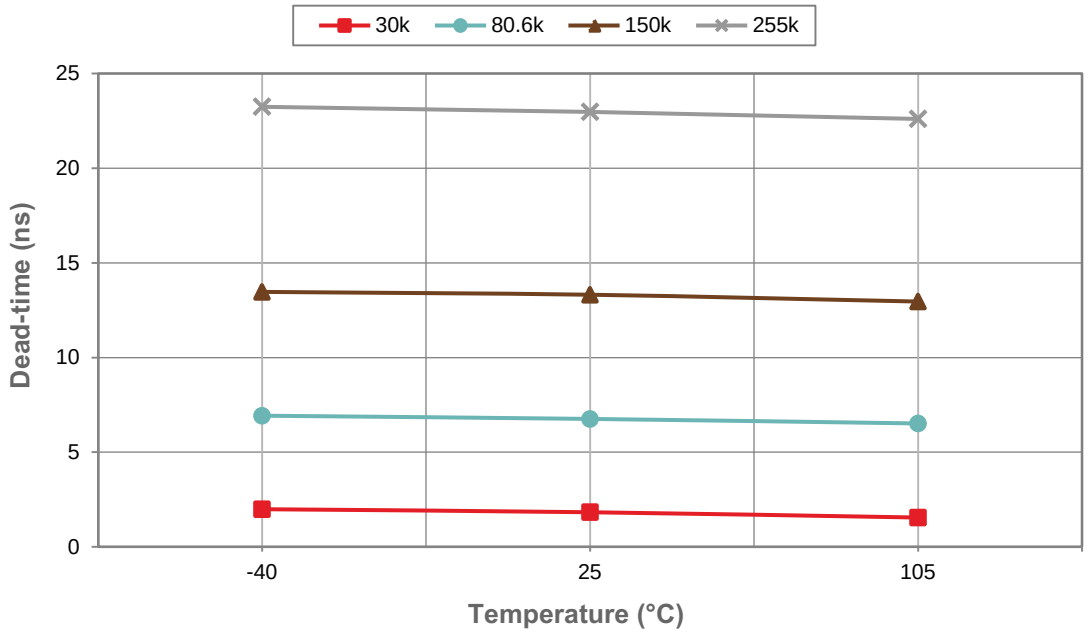


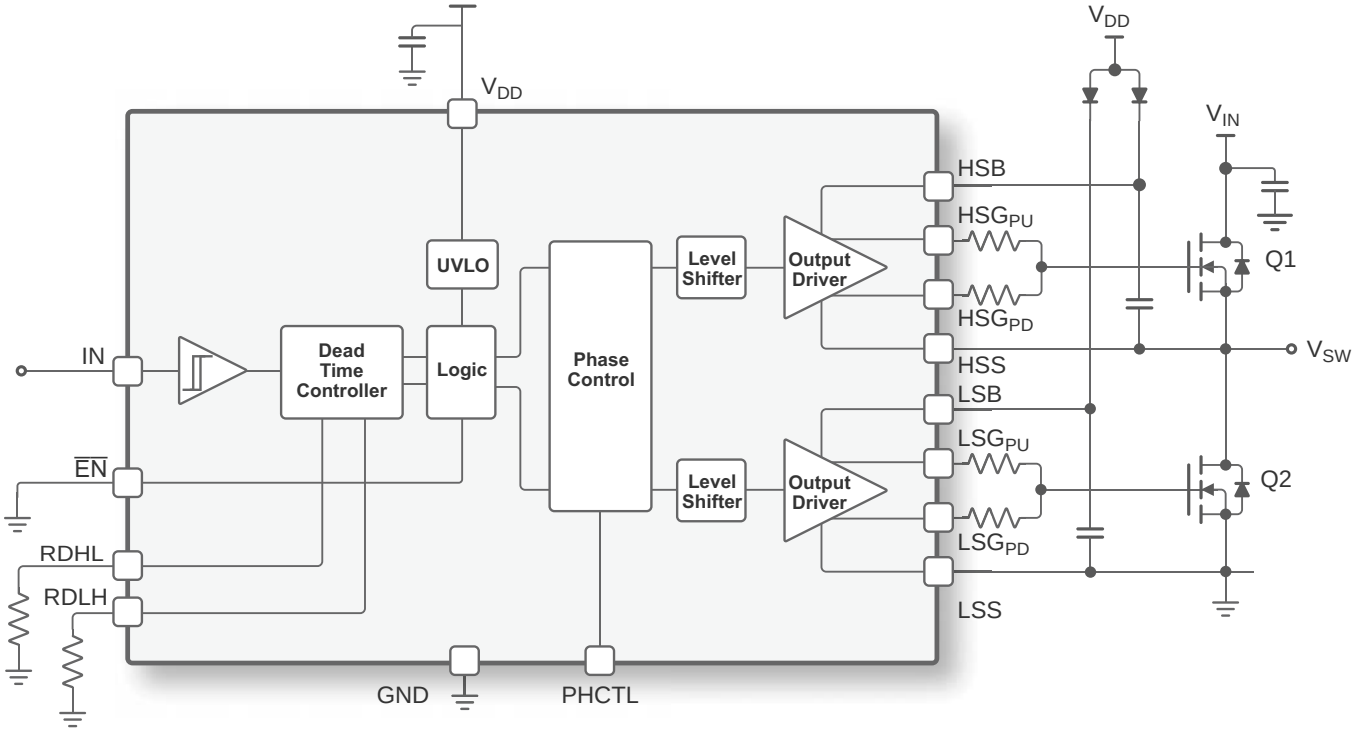
Figure 4 • *Dead-time (ns)*



Test Diagram

Figure 5 shows the test circuit used for obtaining measurements. The two bootstrap diodes shown in the schematic are used for symmetry purposes in characterization. In practice, only the HSB diode is required. Removing the LSB diode will result in higher low-side supply voltage since the diode drop is eliminated. As a result, the dead-time resistor can be adjusted to compensate for any changes in propagation delay.

Figure 5 • *Test Circuit for PE29102*



Theory of Operation

General

The PE29102 is intended to drive both the high-side (HS) and the low-side (LS) gates of external power FETs, such as enhancement mode GaN FETs, for power management applications. The PE29102 is suited for applications requiring higher switching speeds due to the reduced parasitic properties of the high resistivity insulating substrate inherent with Peregrine's UltraCMOS process.

The driver uses a single-ended pulse width modulation (PWM) input that feeds a dead-time controller, capable of generating a small and accurate dead-time. The dead-time circuit prevents shoot-through current in the output stage. The propagation delay of the dead-time controller must be small to meet the fast switching requirements when driving GaN FETs. The differential outputs of the dead-time controller are then level-shifted from a low-voltage domain to a high-voltage domain required by the output drivers.

Each of the output drivers includes two separate pull-up and pull-down outputs allowing independent control of the turn-on and turn-off gate loop resistance. The low impedance output of the drivers improves external power FETs switching speed and efficiency, and minimizes the effects of the voltage rise time (dv/dt) transients.

Under-voltage Lockout

An internal under-voltage lockout (UVLO) feature prevents the PE29102 from powering up before input voltage rises above the UVLO threshold of 3.6V (typ), and 400 mV (typ) of hysteresis is built in to prevent false triggering of the UVLO circuit. The UVLO must be cleared and the $\overline{EN}$ pin must be released before the part will be enabled.

Dead-time Adjustment

The PE29102 features a dead-time adjustment that allows the user to control the timing of the LS and HS gates to eliminate any large shoot-through currents, which could dramatically reduce the efficiency of the circuit and potentially damage the GaN FETs. Two external resistors control the timing of outputs in the dead-time controller block. The timing waveforms are illustrated in **Figure 6**.

The dead-time resistors only affect the rising edge of the low-side gate (LSG) and high-side gate (HSG) outputs. Dead-time resistor RDLH will delay the rising edge of HSG, thus providing the desired dead-time between LSG falling and HSG rising. Likewise, dead-time resistor RDHL will delay the rising edge of LSG, thus providing the desired dead-time between HSG falling and LSG rising. **Figure 7** shows the resulting dead-time versus the external resistor values with both HS and LS bias diode/capacitors installed as indicated in **Figure 5**. The LS bias diode and capacitor are included for symmetry only and are not required for the part to function. Removing the LS bias diode will increase the LSG voltage by approximately 0.3V, resulting in a wider separation of the t_{DHL} and t_{DLH} curves in **Figure 7**.

Phase Control

Pin 10 (PHCTL) controls the polarity of the gate driver outputs. When PHCTL is high, the HSG will be in phase with the input signal. When PHCTL is low, the LSG will be in phase with the input signal. The PHCTL pin includes an internal pull-down resistor and can be left floating.

Figure 6 and **Figure 7** provide the dead-time description for the PE29102.

Figure 6 • *Dead-time Description*

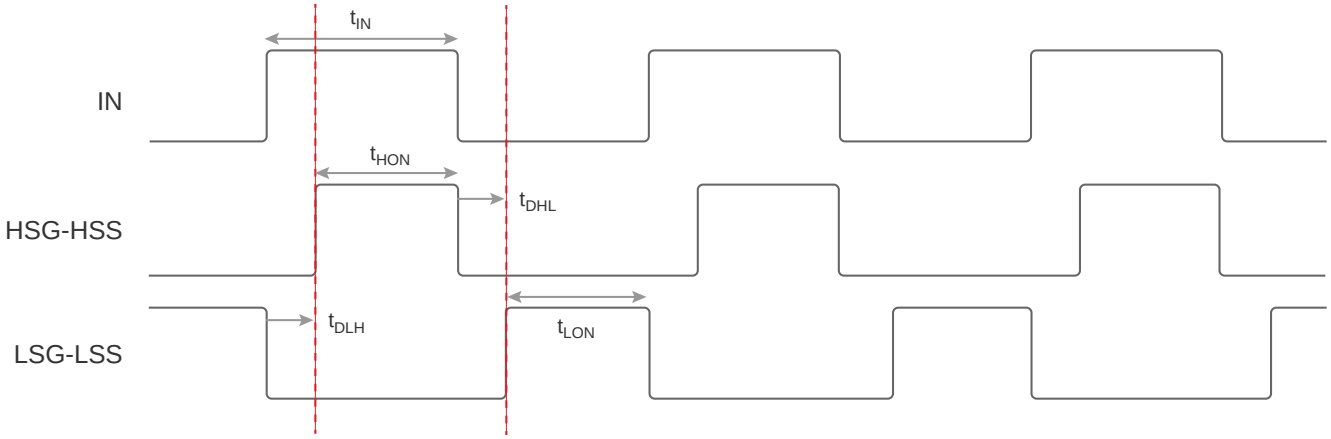
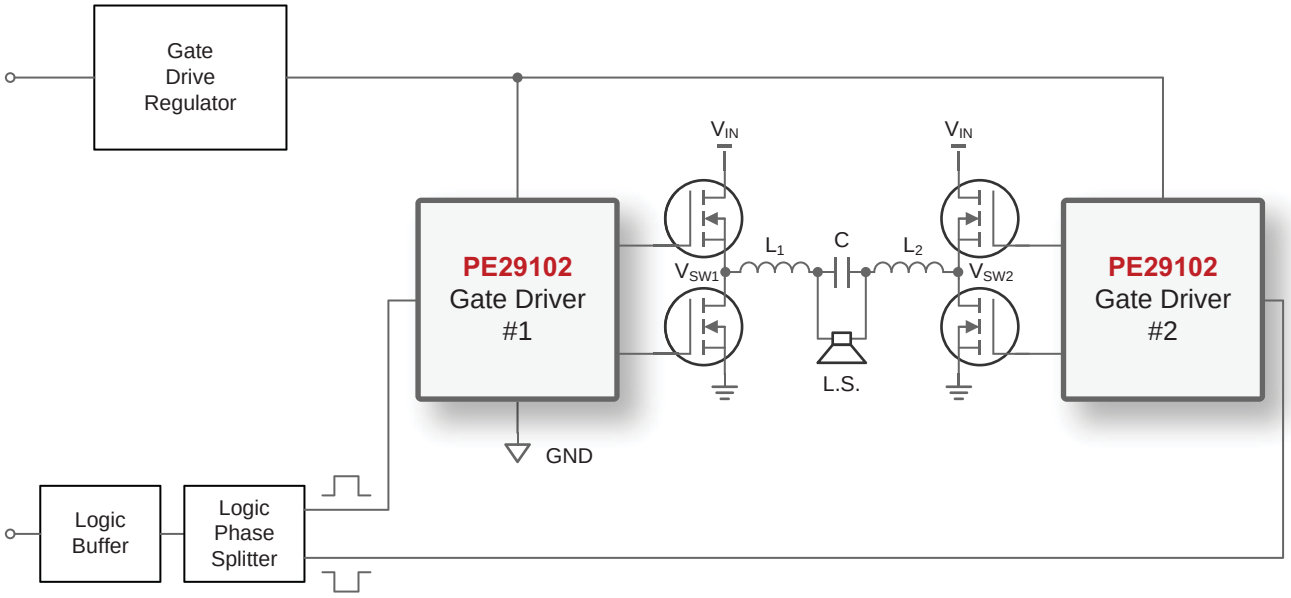


Figure 7 • *Dead-time between HSG and LSG (ns)*

Application Circuit

Figure 8 shows a class-D audio amplifier application diagram using two PE29102 gate drivers in a full-bridge configuration. The full-bridge circuit comprises two half bridge topologies that share a common supply and load. The low-level logic circuitry is powered by the gate drive regulator that supplies the PE29102 drivers, logic buffer and phase splitter. The PWM input signal feeds a single logic buffer, which drives a common logic X-OR gate Phase Splitter that provides phase inverted signals to each driver. VIN is designed to operate at 60V DC (max.) to provide between 100 — 120W of power into an 8Ω load.

Figure 8 • *PE29102 Class D Audio Amplifier Block Diagram*



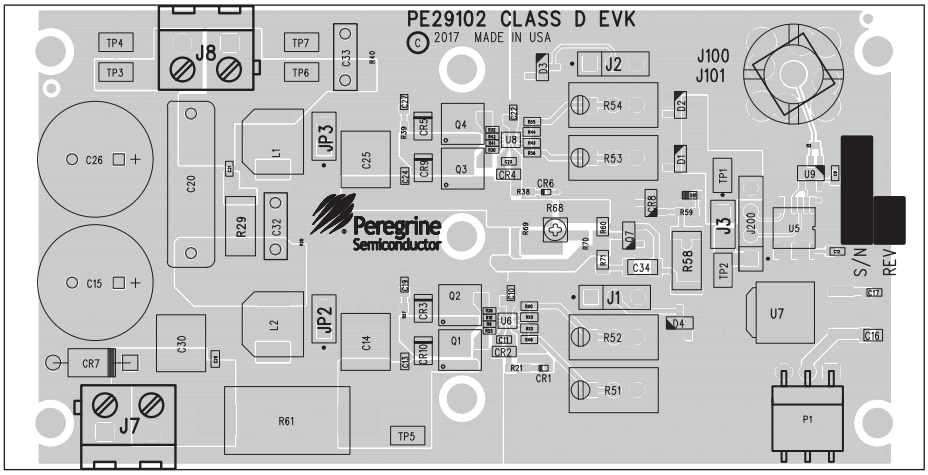
Evaluation Board

The PE29102 evaluation board (EVB) allows the user to evaluate the PE29102 gate driver in either a full-bridge configuration or two independent half-bridge configurations. The EVB is assembled with two PE29102 FET drivers and four GS61004B E-mode GaN FETs. Refer to Peregrine Semiconductor DOC-82956 for more information.

Because the PE29102 is capable of generating fast switching speeds, the printed circuit board (PCB) layout is a critical component of the design. The layout should occupy a small area with the power FETs and external bypass capacitors placed as close as possible to the driver to reduce any resonances associated with the gate loops, common source and power loop inductances. Since the maximum allowable gate-to-source voltage for the GS61004B FETs is 7V, resonance in the gate loops can generate ringing that can degrade the performance and potentially damage the power devices due to high voltage spikes. Additionally, it is important to keep ground paths short.

The PCB is fabricated on FR4 material, with a total thickness of 0.062 inches. A minimum copper thickness of 1.5 ounces or more is recommended on the PCB outer layers to limit resistive losses and improve thermal spreading.

Figure 9 • *PE29102 Evaluation Board Assembly*



Pin Configuration

This section provides pin information for the PE29102. **Figure 10** shows the pin map of this device for the available package. **Table 5** provides a description for each pin.

Figure 10 • *Pin Configuration (Bumps Up)*

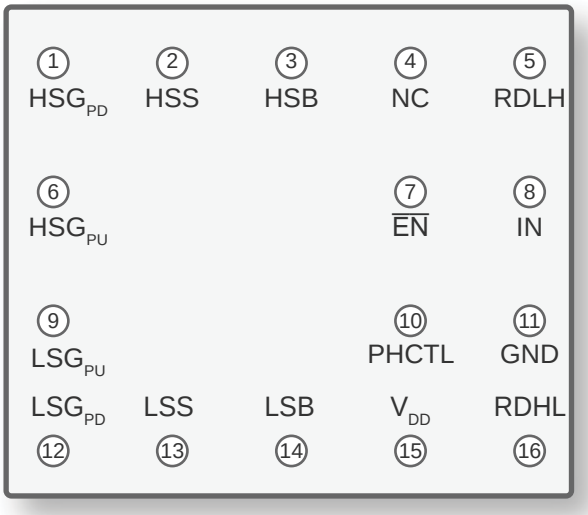


Table 5 • *Pin Descriptions for PE29102*

Pin No.	Pin Name	Description
1	HSG_{PD}	High-side gate drive pull-down
2	HSS	High-side source
3	HSB	High-side bias
4	NC	No connect (tie to board ground)
5	RDLH	Dead-time control resistor sets LSG falling to HSG rising delay (external resistor to GND)
6	HSG_{PU}	High-side gate drive pull-up
7(*)	$\overline{EN}$	Enable active low, tri-state outputs when high
8(*)	IN	Control input
9	LSG_{PU}	Low-side gate drive pull-up
10(*)	PHCTL	Controls the polarity of the gate driver outputs
11	GND	Ground
12	LSG_{PD}	Low-side gate drive pull-down
13	LSS	Low-side source
14	LSB	Low-side bias
15	V_{DD}	+5V supply voltage
16	RDHL	Dead-time control resistor sets HSG falling to LSG rising delay (external resistor to ground)

Note: * Internal 100k pull down resistor

Die Mechanical Specifications

This section provides the die mechanical specifications for the PE29102.

Table 6 • *Die Mechanical Specifications for PE29102*

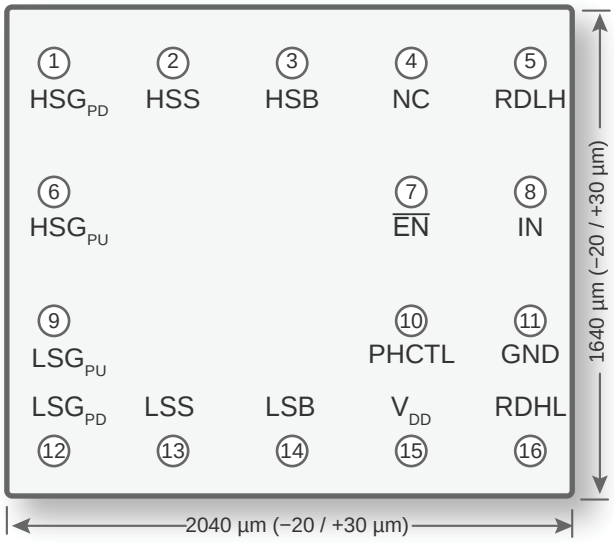
Parameter	Min	Typ	Max	Unit	Test Condition
Die size, singulated (x,y)		2040 × 1640		µm	Including sapphire, max tolerance = –20/+30
Wafer thickness	180	200	220	µm	
Wafer size				µm	
Bump pitch		400		µm	
Bump height		85		µm	
Bump diameter		110		µm	max tolerance = ±17

Table 7 • *Pin Coordinates for PE29102*(*)

Pin #	Pin Name	Pin Center (µm)	
		X	Y
1	HSG_{PD}	–800	600
2	HSS	–400	600
3	HSB	0	600
4	NC	400	600
5	RDLH	800	600
6	HSG_{PU}	–800	200
7	$\overline{EN}$	400	200
8	IN	800	200
9	LSG_{PU}	–800	–200
10	PHCTL	400	–200
11	GND	800	–200
12	LSG_{PD}	–800	–600
13	LSS	–400	–600
14	LSB	0	–600
15	V_{DD}	400	–600
16	RDHL	800	–600

Note: * All pin locations originate from the die center and refer to the center of the pin.

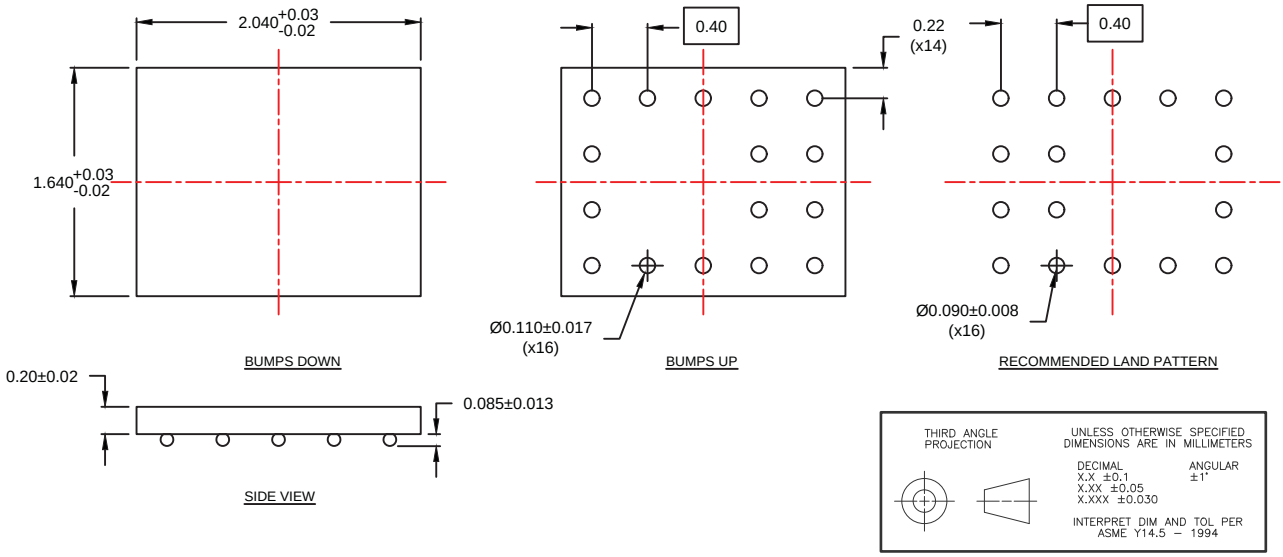
Figure 11 • *Pin Layout for PE29102*(1)(2)



Notes:

1) Drawings are not drawn to scale.
2) Singulated die size shown, bump side up.

Figure 12 • *Recommended Land Pattern for PE29102*



Ordering Information

Table 8 lists the available ordering code for the PE29102.

Table 8 • *Order Code for PE29102*

Order Codes	Description	Packaging	Shipping Method
PE29102A-X	PE29102 flip chip	Die on tape and reel	500 units/T&R
PE29102A-Z	PE29102 flip chip	Die on tape and reel	3000 units/T&R

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

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