Active T89C51AC2, AT89C51AC2 Errata List

- **Flash/EEPROM – First Read After Write Disturbed**
- **Timer 2 – Baud Rate Generator – No IT When TF2 is Set by Software**
- **Timer 2 – Baud Rate Generator – Long Start Time**
- **UART – RB8 Lost with JBC on SCON Register**
- **ADC – Interrupt Controller/ADC Idle Mode/Loops In High Priority Interrupt**
- **Flash/EEPROM – First Read After Load Disturbed**
- **C51 Core – Bad Exit of Power-down in X2 Mode**
- **Timer0/1 – Extra interrupt**
- **Timer1 - Mode1 Does Not Generate Baud Rate Generator for UART**
- **EEPROM – Lock-up during ISP write.**

A/T89C51AC2 Errata History

Lot Number	Errata List
A00151	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14
A00369	1, 3, 4, 5, 6, 7, 8, 9,10, 11, 12, 13,14
A00367, A00368, A00396 to A00529	1, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13,14
A00510, all lots from A00588	**1, 6, 7, 8, 9, 10, 11, 12, 13,14**

A/T89C51AC2 Errata Description

1. Flash/EEPROM – First Read After Write Disturbed

After a write of more than 32 bytes in the EEPROM and 16 bytes in the User Flash memory, the read of the first byte may be disturbed if it occurs just after the write.

Workaround

Do not load/write more than 32 bytes at a time for EEPROM memory.

Do not load/write more than 16 bytes at a time for User Flash memory,

OR wait 10 ms before reading the first byte.

2. Buffer Noise

Large bounces and high noise are generated when buffers are switching (both rising and falling edges).

Workaround

None.

3. Double IT on External Falling Edge on INT1 or INT0 in X2 Mode

When the CPU is in X2 mode and Timer1 or Timer 0 in X1 mode (CKCON = 0x7F), IEx flag is not cleared by hardware after servicing interrupt. In this case, the CPU executes the ISR a second time.

Workaround

The workaround is to clear IEx bit in Interrupt subroutine.

```
INT1_ISR :                    ; Interrupt sub routine
CLR IE1
....
```

80C51 MCUs

AT89C51AC2
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Errata Sheet

4. Movc Instruction on Boot Memory from Boot Memory Does Not Work

No Movc instruction is performed when a program running on the boot memory tries to read its own code by the Movc instruction.

Workaround

None.

5. Power OFF Flag

Power ON Flag does not work.

Workaround

None.

6. Timer 2 – Baud Rate Generator – No IT When TF2 is Set by Software

When Timer 2 is used in baud rate generator mode, setting TF2 by software does not generate an interrupt.

Workaround

Use Timer 1 instead of Timer 2 to generate baud rate and interrupt.

7. Timer 2 – Baud Rate Generator – Long Start Time

When Timer 2 is used as baud rate generator, TH2 is not loaded with RCAP2H at the beginning, then UART is not operational before 10000 machine cycles.

Workaround

Add the initialization of TH2 and TL2 in the initialization of Timer 2.

8. UART – RB8 Lost With JBC on SCON Register

May lose RB8 value, if RB8 changes from 1 to 0 during JBC instruction on SCON register.

Workaround

Clear RB8 at the beginning of the code and after each time it goes to 1.

9. ADC – Interrupt Controller/ADC Idle Mode/Loops In High Priority Interrupt

The problem occurs during an A/D conversion in idle mode if a hardware interrupt occurs followed by a second interrupt with higher priority before the end of the A/D conversion. If the above configuration occurs, the highest priority interrupt is served immediately after the A/D conversion. At the end of the highest priority interrupt service, the processor will not serve the hardware reset interrupt pending. It will also not serve any new interrupt requests with a priority lower than the high level priority last served.

Workaround

Disable all interrupts (Interrupt Global Enable Bit) before starting an A/D conversion in idle mode, then re-enable all interrupts immediately after.

10. Flash/EEPROM – First Read After Load Disturbed

This “Read After Load” problem does not occur with Atmel Bootloader (workaround 2 is Implemented).

In the "In-Application Programming" mode from the Flash, if the user software application loads the Column Latch Area prior to call the programming sequence in the Bootloader, the "Read after load" issue leads to a wrong Opcode Fetch during the column latch load sequence.

Workaround

Two workarounds are possible:

– A NOP instruction has to be inserted after the load instruction in the application.
  MOVX @DPTR,A ;Load Column latches
  NOP ; ADDED INSTRUCTION
– Load of the column latch in the bootloader area.

11. C51 Core – Bad Exit of Power-down in X2 Mode

When exiting power-down mode by interrupt while CPU is in X2 mode, it leads to bad execution of the first instruction run when CPU restarts.

Workaround

Set the CPU in X1 mode directly before entering power-down mode.

12. Timer0/1 – Extra interrupt.

When the Timer0 is in X1 mode and Timer1 in X2 mode and vice versa, extra interrupt may randomly occurred for Timer0 or Timer1.

Workaround

Use the same mode for the two timers.

13. EEPROM – Lock-up during ISP write.

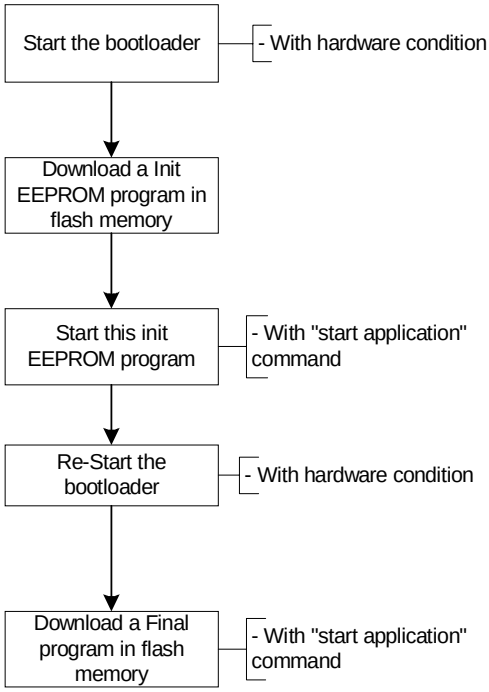
Program lock-up can be experienced when using Atmel FLIP software or a custom In system Programming tools to write in the internal EEPROM. This problem occurs with clock frequency > 12MHz in X2 mode or 24MHz in X1 mode. Neither the code Flash nor the EEPROM are corrupted by the lock-up. Although the EEPROM cannot be written by the bootloader.

This problem does not affect the capability to erase, read and write into the code Flash and the additional bytes with In-System Programming as Atmel FLIP.

This problem is bootloader related and doesn't affect the capability for the user to read and write into the EEPROM. This problem is technology dependant. The likelihood of experiencing the problem is low at Clock frequency > 24 MHz in X1 mode and null below. A reset can be applied to recover from the lock-up.

Workaround

The following process can be done to work around the problem.



C Init EEPROM program example:

```
#define SIZE_EEPROM 12

unsigned char code
tab_eep[SIZE_EEPROM]={0x11,0x22,0x33,0x44,0x55,0x66,0x77,0x88,0x99,0xAA};

void main (void)
{
  unsigned char xdata * address;
  unsigned char cpt;

  address =0x00;
  for (cpt=0; cpt<SIZE_EEPROM; cpt++)
  {
    EECON = 0x02; // enable eeprom access
    *(address + cpt) = tab_eep[cpt];
    EECON = 0x50;
    EECON = 0xA0;
    while (EECON&0x01);
  }
}
```

Assembler Init EEPROM program example:

```
SIZE_EEPROM EQU 00Ah

CSEG AT 0000H
```

```
Mov  R1, #SIZE_EEPROM
Mov  DPTR, #0h

Load_eeprom:
  MovEECON, #02h    ; set bit EEE for access to the column latches
  MovA, #Tab_eep
  Movc   A, @A + DPTR
  Movx  @DPTR, A

  Mov EECON, #050h
  Mov EECON, #0A0h

WAIT_FBUSY:
  Mov  A, EECON
  AnlA, #001h
  Xrl A, #001h
  JzWAIT_FBUSY
  Inc   DPTR
  Djnz  R1, Load_eeprom

End_loop:
  jmp End_loop

  Tab_eep: DB     012h, 023h, 045h, 067h, 089h, 0ABh, 0CDh, 0EFh
```

14. Timer1 – in Mode 1 Does Not Generate Baud Rate to UART

The timer1, when used as a baud rate generator in mode 1 (16 bits counter) for low baud rates, does not generate baud rate to UART.

Workaround

No.

Active UART Bootloader Errata List

- **Timer 2 and UART Are Not Stopped**
- **Watchdog and Flash API Starting the Bootloader Execution**
- **Autobaud False Start Bit Detection**
- **Flash API “__api_wr_code_page” with 0 Data in Length Parameter Field**

UART Bootloader Errata History

Version Number	Errata List
1.2 (1.1.2 displayed by FLIP)	1, 2, 3, 4
1.4	**1, 2, 3, 5**

UART Bootloader Errata Description

1. Timer 2 and UART Are Not Stopped

When the bootloader receives the command “Start Application” (LJMP 0), the Timer 2 and the UART are not stopped.

Workaround

The application must have in its setup function a reset of Timer 2 and UART.

```
mov SCON, #00h
mov T2CON, #00h
mov RCAP2L, #00h
mov RCAP2H, #00h
mov TL2, #00h
mov TH2, #00h
```

2. Watchdog and Flash API Starting the Bootloader Execution

When an application call “__api_start_bootloader” or”__api_start_isp” routines while the watchdog is enabled, when the watchdog overflow it will restart the application instead of the bootloader

Workaround

Set BLJB(=1) before calling the __api_start_bootloader or __api_start_isp if the watchdog is used.

3. Autobaud False Start Bit Detection

UART autobaud sequence does not work on some special UARTs.

Some laptops have the UART TX line set to 0 when unused (COM port closed), this results in a false baud rate calculation on the ‘U’ character.

The autobaud sequence checks for a ‘0’ state (not a falling edge) on the Rx line of the UART microcontroller to detect the ‘start’ bit of the ‘U’ synchro character.

As this line is ‘0’ by default when COM port is closed, the autobaud routine starts its baudrate calculation at the opening sequence of the UART.

Workaround

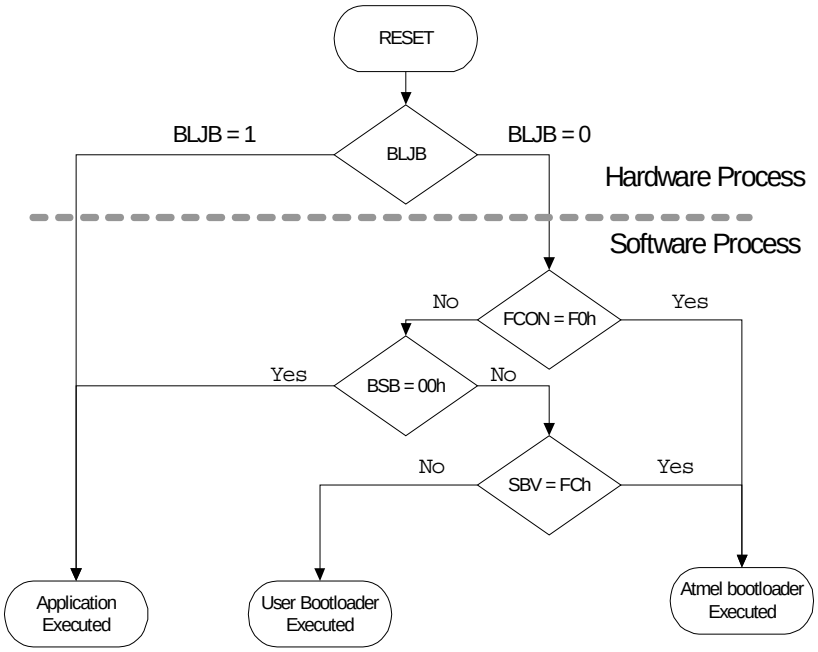
A ‘Special Sync’ can be used with ‘FLIP’ software.

In this case, the open port event and the ‘U’ sent are dissociated. The user must first open his COM port with the ‘connect’ button, then reset its hardware and finally push the ‘sync’ button.

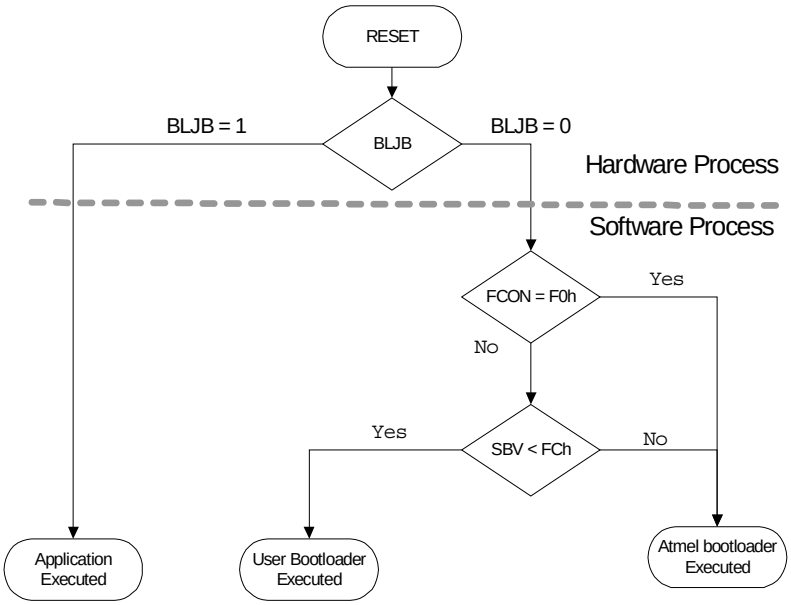
4. Boot Process Compatibility

There are some differences between Boot process of bootloader 1.2 and newer versions.

Version 1.2:



Version 1.4:



Workaround

Use the fuse bit BLJB to start the application on both versions.

5. Flash API “__api_wr_code_page” with 0 Data in Length Parameter Field

When the Flash API “__api_wr_code_page” is called with the field nb_data equal 0 then 255 data is written in Flash.

Workaround

Include a test on nb_data before executed __api_wr_code_page routine.

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4159G–8051–05/06