SL28DB200

100 MHz Differential Buffer for PCI Express and SATA

Features

- **Two differential 0.7V clock output pairs**
- **OE# input for enabling SRC outputs**
- **Individual OE controls**
- **Low CTC jitter (< 50 ps)**
- **Spread Aware**
- **3.3V operation**
- **Industrial Temperature Grade -40°C to +85°C**
- **16-pin TSSOP package**

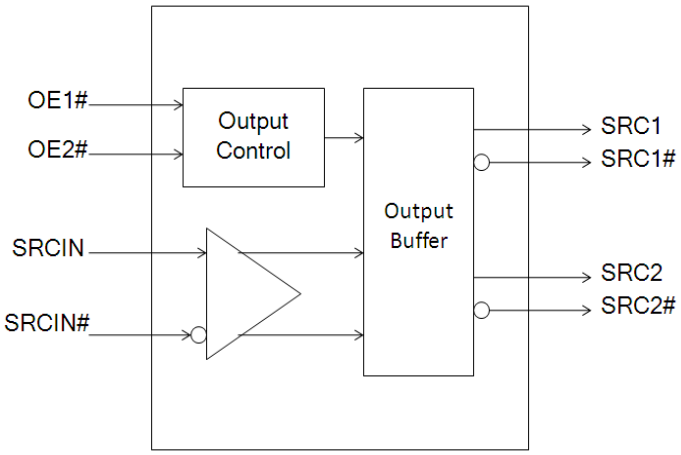
Functional Description

The SL28DB200 is a differential buffer capable of distributing the Serial Reference Clock (SRC) for PCI Express Gen2 and SATA implementations. The buffer enables the application system to control the distribution of the SRC.

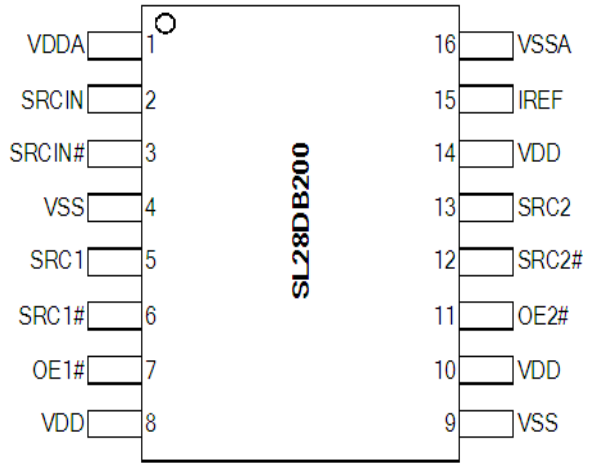
Applications

- **Network/Media Attached Storage**
- **Routers/IP Gateways**
- **Multi-function Printers**

Block Diagram



Pin Configuration



16 TSSOP

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Pin Description

Pin	Name	Type	Description
2,3	SRCIN, SRCIN#	I,DIF	**0.7V Differential inputs**
5,6,13,12	SRC[1:2], SRC[1:2]#	O,DIF	**0.7V Differential Clock Outputs**
7,11	OE[1:2]#	I,SE	**3.3V LVTTL input for enabling differential outputs**
15	IREF	I	**A precision resistor 475 ohm is attached to this pin to set the differential output current**
1	VDDA	PWR	**3.3V Power Supply**
16	VSSA	GND	**Ground**
8,10,14	VDD	PWR	**3.3V power supply for outputs**
4,9	VSS	GND	**Ground for outputs**

Notes: I=Input, O=Output, DIF=Differential signal, SE=Single Ended, PWR=Power input, GND=Ground

Table 1. Buffer Power-up State Machine

State	Description
S0	3.3V Buffer power off
S1	After 3.3V supply is detected to rise above 1.8V - 2.0V, the buffer enters state 1 and initiates a 0.2-ms–0.3-ms delay
S2	Buffer waits for a valid clock on the SRCIN input
S3	Once a valid input is detected, the buffer enters state 3 and enables outputs for normal operation

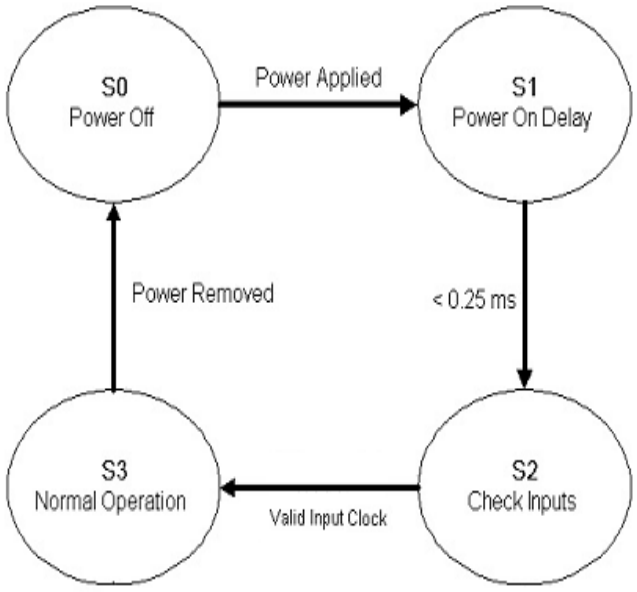


Figure 1. Buffer Power-up State Diagram

Output Enable Clarification

OE# functionality allows for enabling and disabling individual outputs. OE1# and OE2# are Active LOW inputs. Disabling the outputs may be implemented by deasserting the OE# input pin. If the OE# pin is deasserted, the output of interest will be tri-stated. (The assertion and deassertion of this signal is absolutely asynchronous.)

OE Assertion

All differential outputs that were tri-stated will resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2–6 SRC clock periods. In addition, SRC clocks will be driven high within 15 ns of OE# assertion to a voltage greater than 200 mV

OE Deassertion

The impact of deasserting OE# is that each corresponding output will transition from normal operation to tri-state in a glitch-free manner. The maximum latency from the deassertion to tri-stated outputs is between 2–6 DIF clock periods.

Table 2. OE Functionality

OE#	SRC,SRC#
0	Enable
1	Tri-State

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
VDD	Core Supply Voltage		–0.5	4.6	V
VDDA	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient (Commercial Grade)	Functional	0	85	°C
T_A	Temperature, Operating Ambient (Industrial Grade)	Functional	-40	85	°C
T_J	Temperature, Junction	Functional		150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC (JESD 22 - A114)	2000	–	V
UL-94	Flammability Rating	UL (Class)	V–0		
MSL	Moisture Sensitivity Level		1		

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDDA, VDD	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{IL}	3.3V Input Low Voltage		V_{SS} – 0.5	0.8	V
V_{IH}	3.3V Input High Voltage		2.0	V_{DD} + 0.5	V
I_{IL}	Input Low Leakage Current	except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5		µA
I_{IH}	Input High Leakage Current	except internal pull-down resistors, $0 < V_{IN} < V_{DD}$		5	µA
C_{IN}	Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance		–-	6	pF
L_{IN}	Pin Inductance		–	7	nH
$I_{DD3.3V}$	Dynamic Supply Current	At max. load, Full Active, at 100MHz	–	60	mA

AC Electrical Specifications

All measurements at VDD (typical) = 3.3V, T_A = 25°C unless otherwise stated

Parameter	Description	Condition	Min.	Max.	Unit
SRCIN at 0.7V					
T_{PERIOD}	Average Period	Measured at crossing point V_{OX}	9.9970	10.0533	ns
$T_{ABSMIN-IN}$	Absolute minimum clock periods	Measured at crossing point V_{OX}	9.8720		ns
T_R / T_F	SRC and SRC# Rise and Fall Times	Single ended measurement: V_{OL} = 0.175 to V_{OH} = 0.525V (Averaged)	0.6	4	V/ns
V_{IH}	Differential Input High Voltage		150		mV
V_{IL}	Differential Input Low Voltage			–150	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing	Single-ended measurement	250	550	mV
ΔV_{OX}	Vcross Variation over all edges	Single-ended measurement		140	mV
V_{RB}	Differential Ringback Voltage		–100	100	mV
T_{STABLE}	Time before ringback allowed		500		ps
V_{MAX}	Absolute maximum input voltage			1.15	V
V_{MIN}	Absolute minimum input voltage		–0.3		V
T_{DC}	SRC and SRC# Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R – T_F)/(T_R + T_F)$	–	20	%
SRC at 0.7V					
F_{IN}	Input Frequency		90	210	MHz
F_{ERROR}	Input/Output Frequency Error		–	0	ppm
T_{DC}	SRC and SRC# Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	Average Period	Measured at crossing point V_{OX} at 100 MHz	9.9970	10.0533	ns
T_R / T_F	SRC[1:2] and SRC[1:2]# Rise and Fall Times	Single-ended measurement: V_{OL} = 0.175 to V_{OH} = 0.525V (Averaged)	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2 * (T_R – T_F)/(T_R + T_F)$	–	20	%
$\Delta T_R/\Delta T_F$	Rise and Fall Time Variation Variation	Single-ended measurement: V_{OL} = 0.175 to V_{OH} = 0.525V (Real Time)	–	125	ps
V_{HIGH}	Voltage High	Single-ended measurement	660	850	mv
V_{LOW}	Voltage Low	Single-ended measurement	–150	–	mv
V_{OX}	Crossing Point Voltage at 0.7V Swing	Single-ended measurement	250	550	mv
ΔV_{OX}	Vcross Variation over all edges	Single-ended measurement	–	140	mV
V_{OVS}	Maximum Overshoot Voltage	Single-ended measurement	–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage	Single-ended measurement	–	–0.3	V
V_{RB}	Ring Back Voltage	Single-ended measurement	0.2	N/A	V
T_{CCJ}	Cycle to Cycle Jitter	Jitter is additive	–	50	ps
T_{SKEW}	Any SRC/SRC# to SRC/SRC# Clock Skew	Measured at crossing point V_{OX}	–	50	ps
T_{PD}	Input to output skew	Measured at crossing point V_{OX}	2.5	4.5	ns

Test and Measurement Setup

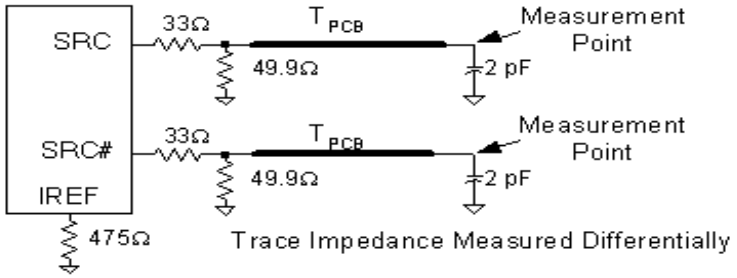


Figure 1. Differential Clock Termination

Switching Waveforms

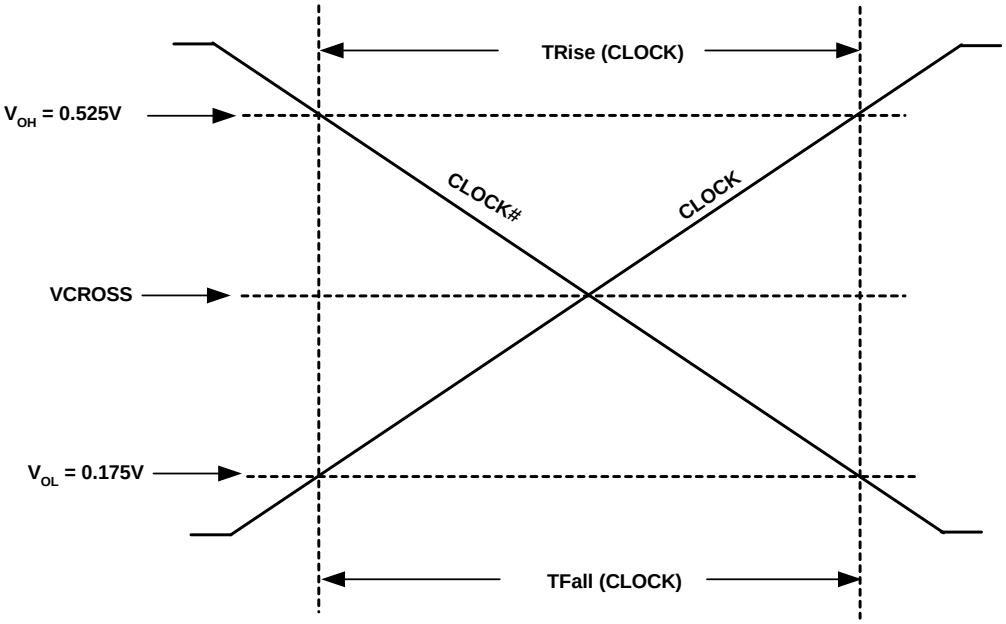


Figure 2. Single-Ended Measurement Points for TRise and TFall

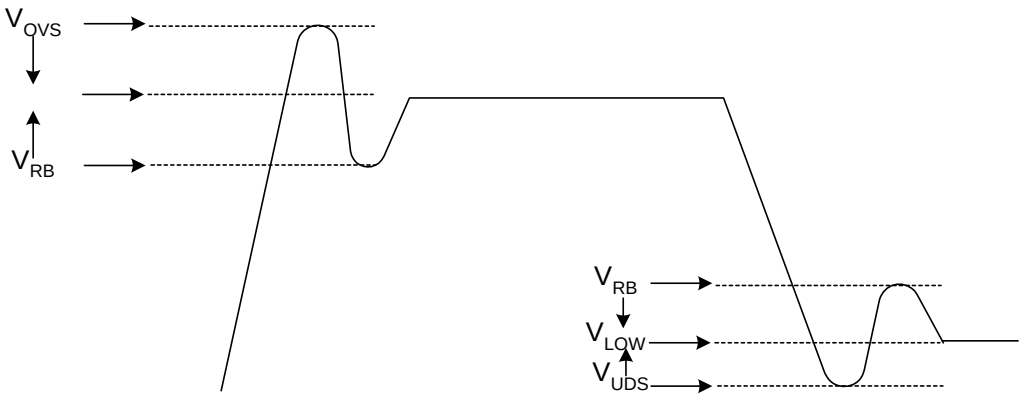


Figure 3. Single-ended Measurement Points for V_{OVS},V_{UDS} and V_{RB}

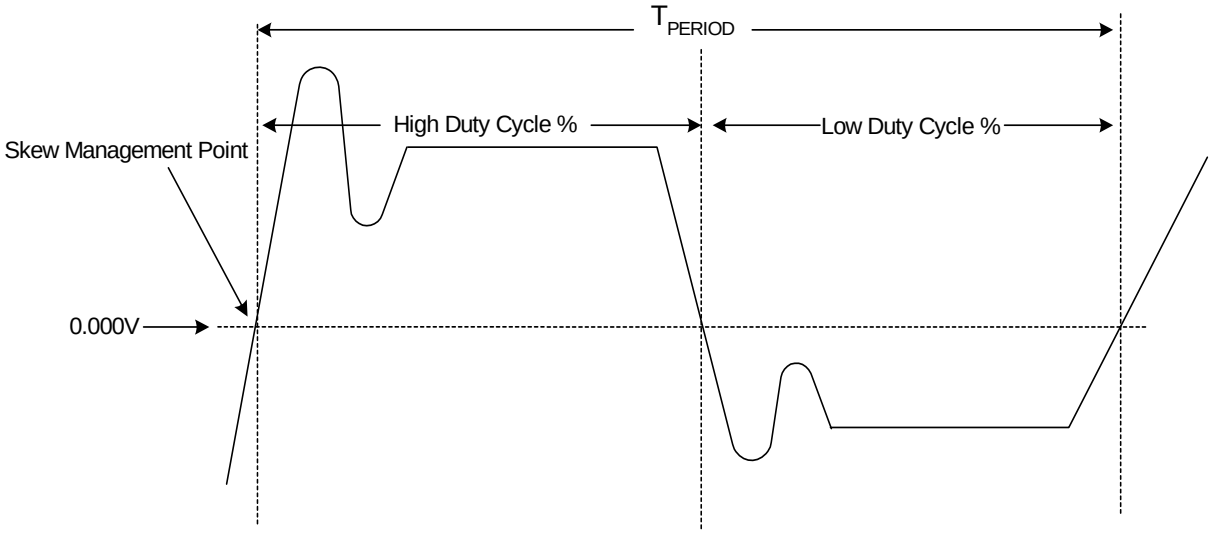


Figure 4. Differential (Clock-Clock#) Measurement Points (Tperiod, Duty Cycle and Jitter)

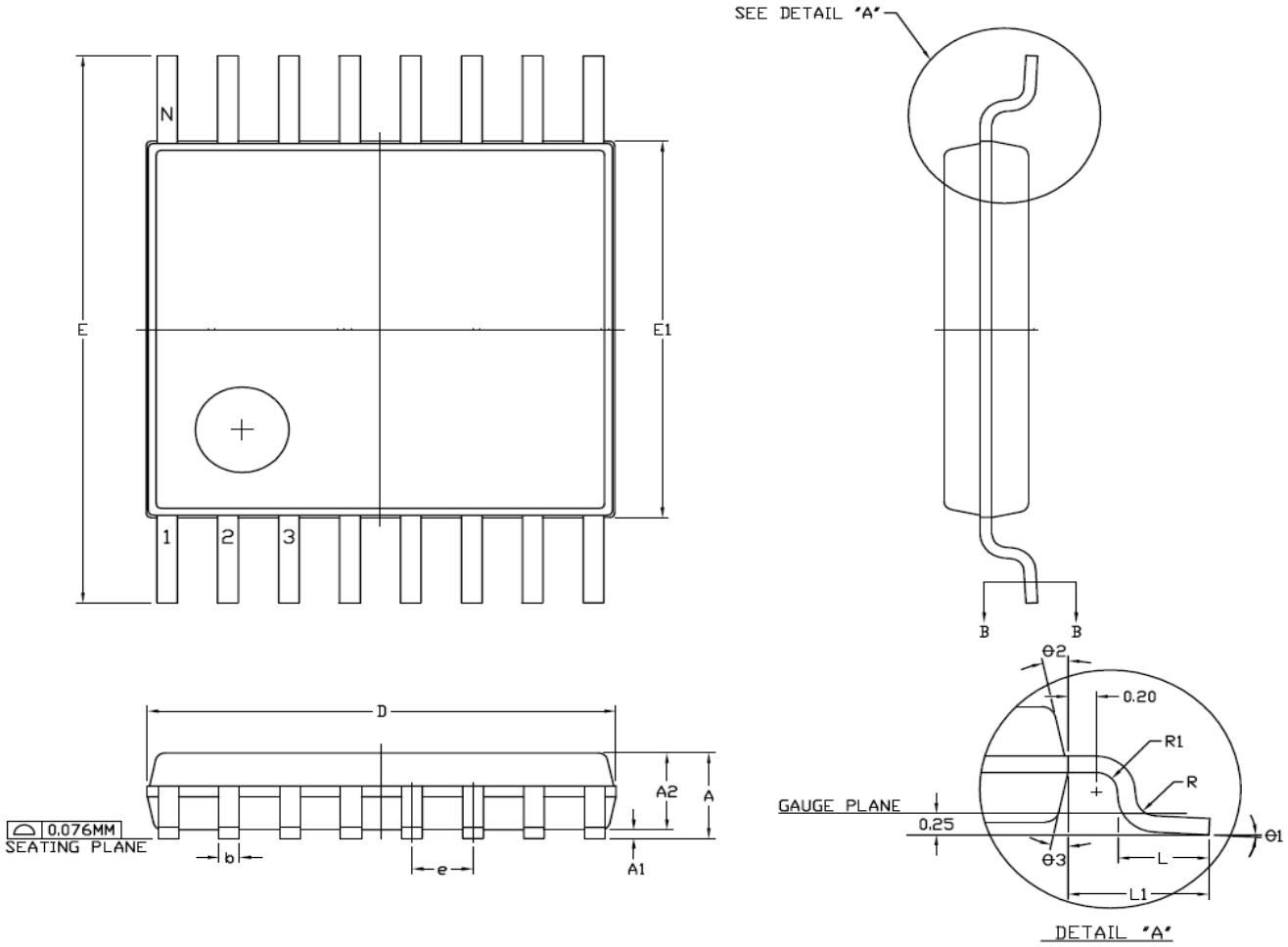
Ordering Information

Ordering Code	Package Type	Operating Range
Lead-free		
SL28DB200AZC	16-pin TSSOP	Commercial, 0°C to 85°C
SL28DB200AZCT	16-pin TSSOP—(Tape and Reel)	Commercial, 0°C to 85°C
SL28DB200AZI	16-pin TSSOP	Industrial, -40°C to 85°C
SL28DB200AZIT	16-pin TSSOP—(Tape and Reel)	Industrial, -40°C to 85°C

Note: All oderables are Lead-free and RoHS compliant

Package Drawing and Dimensions

16-Lead Thin Shrunk Small Outline Package



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			.047
A1	0.05		0.15	.002		.006
A2	0.80	0.90	1.05	.031	.035	.041
b	0.19		0.30	.007		.012
b1	0.19	0.22	0.25	.007	.009	.010
c	0.09		0.20	.004		.008
c1	0.09		0.16	.004		.006
D	4.90	5.00	5.10	.193	.197	.200
e	0.65 BSC.			.026 BSC.		
E	6.40 BSC.			.252 BSC.		
E1	4.30	4.40	4.50	.169	.173	.177
L	0.50	0.60	0.75	.020	.024	.030
L1	1.00 REF.			.039 REF.		
R	0.09			.004		
R1	0.09			.004		
θ1	0		8	0		8
θ2	12 REF.			12 REF.		
θ3	12 REF.			12 REF.		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. "N" IS THE NUMBER OF TERMINAL POSITIONS.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. REFERENCE DRAWING JEDEC MO-153, VARIATION AB.

Document History Page

Document Title: SL28DB200 PCI Express Gen2 and SATA Differential Buffer Document #: 38-07722 Rev *C				
REV.	**ECR#**	**Issue Date**	**Orig. of Change**	**Description of Change**
1.0		06/17/10	TRP	Initial Release
AA		09/27/10	TRP	Updated Dynamic Supply Current