This product is not recommended for new designs.

LNK501
LinkSwitch Family

Energy Efficient, CV/CC Switcher for
Very Low Cost Chargers and Adapters

Product Highlights

Cost Effective Linear/RCC Replacement

- Lowest cost and component count, constant voltage, constant current (CV/CC) solution
- Extremely simple circuit configuration
- Up to 75% lighter power supply reduces shipping cost
- Primary based CV/CC solution eliminates 10 to 20 secondary components for low system cost
- Combined primary clamp, feedback, IC supply, and loop compensation functions – minimizes external components
- Fully integrated auto-restart for short circuit and open loop fault protection – saves external component costs
- 42 kHz operation simplifies EMI filter design
- 3 W output with EE13 core for low cost and small size

Much Higher Performance Over Linear/RCC

- Universal input range allows worldwide operation
- Up to 70% reduction in power dissipation – reduces enclosure size significantly
- CV/CC output characteristic without secondary feedback
- System level thermal and current limit protection
- Meets all single point failure requirements with only one additional clamp capacitor
- Controlled current in CC region provides inherent soft-start
- Optional opto feedback improves output voltage accuracy

EcoSmart™ – Extremely Energy Efficient

- Consumes <300 mW at 265 VAC input with no load
- Meets California Energy Commission (CEC), Energy Star, and EU requirements
- No current sense resistors – maximizes efficiency

Applications

- Linear transformer replacement in all ≤3 W applications
- Chargers for cell phones, cordless phones, PDAs, digital cameras, MP3/portable audio devices, shavers, etc.
- Home appliances, white goods and consumer electronics
- Constant output current LED lighting applications
- TV standby and other auxiliary supplies

Description

LinkSwitch™ is specifically designed to replace all linear transformer/RCC chargers and adapters in the ≤3 W universal range at equal or lower system cost with much higher performance and energy efficiency. LinkSwitch introduces a revolutionary topology for the design of low power switching power supplies that rivals the simplicity and low cost of linear adapters, and enables a much smaller, lighter, and attractive package when compared with the traditional “brick.” With efficiency of up to 75% at 3 W output and < 300 mW no-load consumption, **a LinkSwitch solution can save the end user enough energy over a linear design to completely pay for the power supply cost in less than one year**. LinkSwitch integrates a 700 V power MOSFET, PWM control, high voltage start-up, current limit, and thermal shutdown circuitry, onto a monolithic IC.

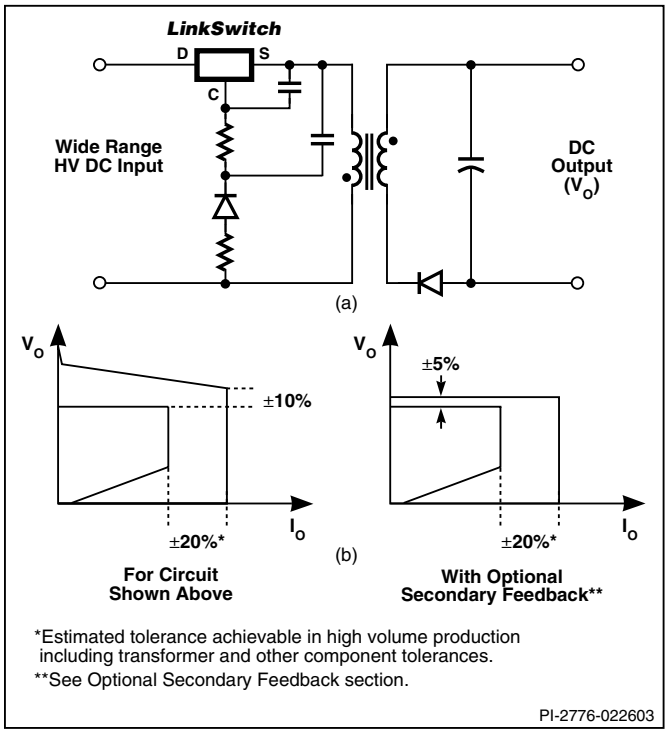


Figure 1. Typical Application – Not a Simplified Circuit (a) and Output Characteristic Tolerance Envelopes (b).

Output Power Table[1]			
Product[3]	230 VAC ±15%	85-265 VAC	No-Load Input Power
LNK501P or G	4 W	3 W	<300 mW
	5.5 W	3.5 W	<500 mW[2]

Table 1. Notes: 1. Typical output power for designs in an enclosed adapter measured at 50 °C ambient. 2. Uses higher reflected voltage transformer designs for increased power capability – See Key Application Considerations section. 3. For lead-free package options, see Part Ordering Information.

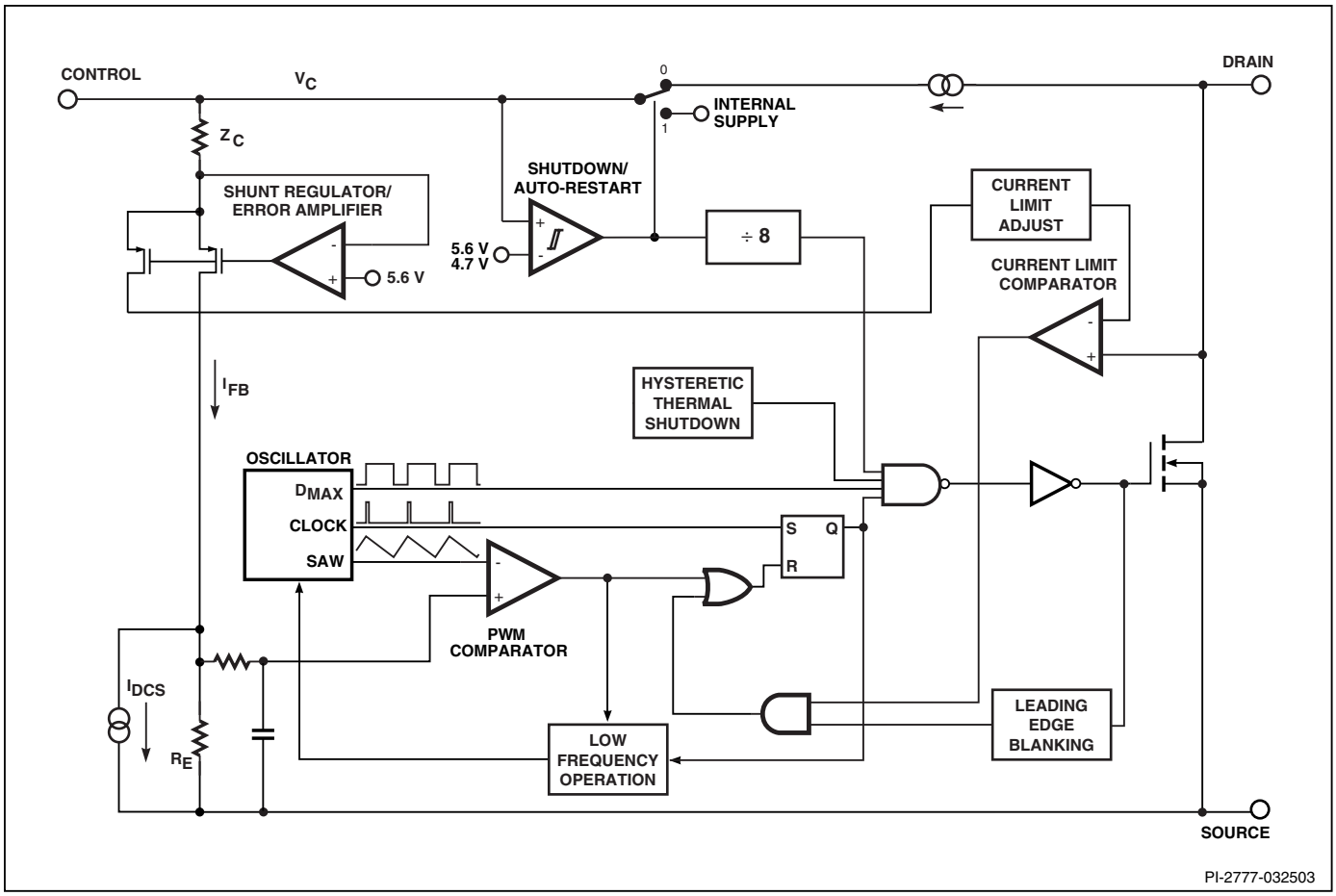


Figure 2. Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
Power MOSFET drain connection. Provides internal operating current for start-up. Internal current limit sense point for drain current.

CONTROL (C) Pin:
Error amplifier and feedback current input pin for duty cycle and current limit control. Internal shunt regulator connection to provide internal bias current during normal operation. It is also used as the connection point for the supply bypass and auto-restart/compensation capacitor.

SOURCE (S) Pin:
Output MOSFET source connection for high voltage power return. Primary side control circuit common and reference point.

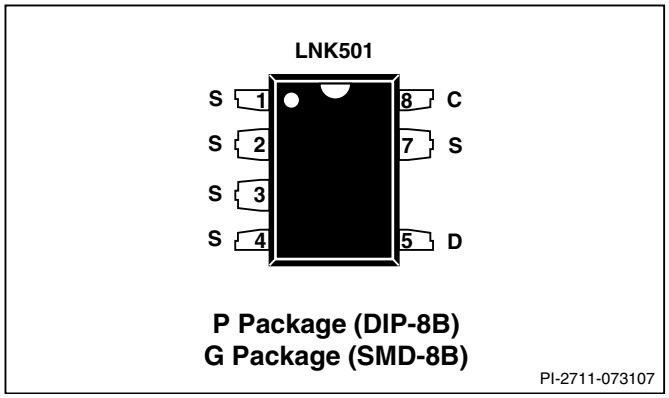


Figure 3. Pin Configuration.

LinkSwitch Functional Description

The duty cycle, current limit and operating frequency relationships with CONTROL pin current are shown in Figure 4. Figure 5 shows a typical power supply outline schematic which is used below to describe the LinkSwitch operation.

Power Up

During power up, as V_{IN} is first applied (Figure 5), the CONTROL pin capacitor C1 is charged through a switched high voltage current source connected internally between the DRAIN and CONTROL pins (see Figure 2). When the CONTROL pin voltage reaches approximately 5.6 V relative to the SOURCE pin, the high voltage current source is turned off, the internal control circuitry is activated and the high voltage internal MOSFET starts to switch. At this point, the charge stored on C1 is used to supply the internal consumption of the chip.

Constant Current (CC) Operation

As the output voltage, and therefore the reflected voltage across the primary transformer winding ramp up, the feedback CONTROL current I_C increases. As shown in Figure 4, the internal current limit increases with I_C and reaches I_{LIM} when I_C is equal to I_{DCT}. The internal current limit vs. I_C characteristic is designed to provide an approximately constant power supply output current as the power supply output voltage rises.

Constant Voltage (CV) Operation

When I_C exceeds I_{DCS}, typically 2 mA (Figure 4), the maximum duty cycle is reduced. At a value of I_C that depends on power supply input voltage, the duty cycle control limits LinkSwitch peak current below the internal current limit value. At this point the power supply transitions from CC to CV operation. With minimum input voltage in a typical universal input design, this transition occurs at approximately 30% duty cycle. Resistor R1 (Figure 5) is therefore initially selected to conduct a value of I_C approximately equal to I_{DCT} when V_{OUT} is at the desired value at the minimum power supply input voltage. The final choice of R1 is made when the rest of the circuit design is complete. When the duty cycle drops below approximately 4%, the frequency is reduced, which reduces energy consumption under light load conditions.

Auto-Restart Operation

When a fault condition, such as an output short circuit or open loop, prevents flow of an external current into the CONTROL pin, the capacitor C1 discharges towards 4.7 V. At 4.7 V, auto-restart is activated, which turns the MOSFET off and puts the control circuitry in a low current fault protection mode. In auto-restart, LinkSwitch periodically restarts the power supply so that normal power supply operation can be restored when the fault is removed.

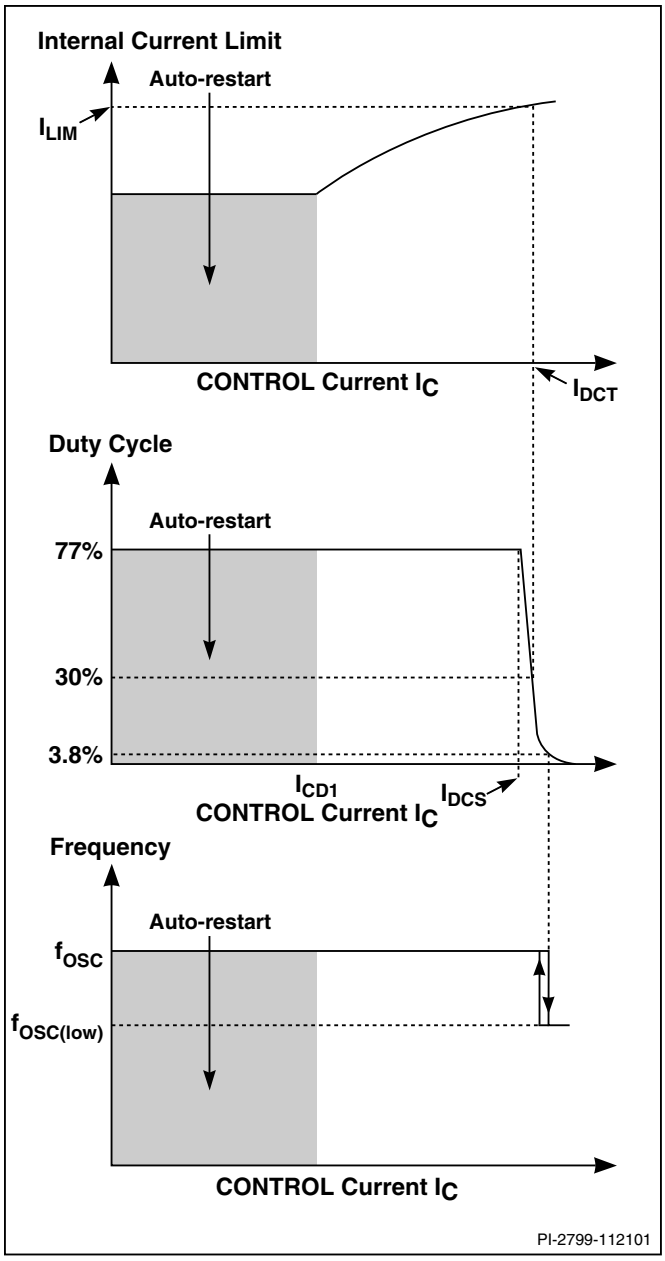


Figure 4. CONTROL Characteristics.

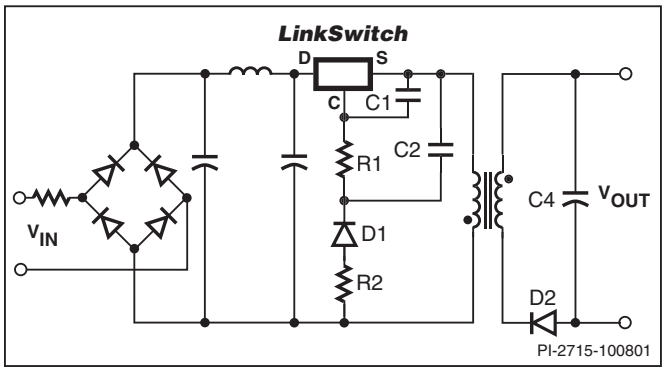


Figure 5. Power Supply Outline Schematic.

The characteristics described above provide an approximate CV/CC power supply output without the need for secondary side voltage or current feedback. The output voltage regulation is influenced by how well the voltage across C2 tracks the reflected output voltage. This tracking is influenced by the value of the transformer leakage inductance which introduces an error. Resistor R2 and capacitor C2 partially filter the leakage inductance voltage spike, reducing this error. This circuitry, used with standard transformer construction techniques, provides much better output load regulation than a linear transformer, making this an ideal power supply solution in many low power applications. If tighter load regulation is required, an optocoupler configuration can be used while still employing the constant output current characteristics provided by LinkSwitch.

Optional Secondary Feedback

Figure 6 shows a typical power supply outline schematic using LinkSwitch with optocoupler feedback to improve output voltage regulation. On the primary side, the schematic differs from Figure 5 by the addition of R3, C3 and optocoupler U1. Resistor R3 forms a potential divider with R1 to limit the U1 collector emitter voltage.

On the secondary side, the addition of voltage sense circuit components R4, VR1 and U1 LED provide the voltage feedback signal. In the example shown, a simple Zener (VR1) reference is used though a precision TL431 reference is typically needed to provide ±5% output voltage tolerancing and cable drop compensation, if required. Resistor R4 provides biasing for VR1. The regulated output voltage is equal to the sum of the VR1 Zener voltage plus the forward voltage drop of the U1 LED. Resistor R5 is an optional low value resistor to limit U1 LED peak current due to output ripple. Manufacturer's specifications for U1 current and VR1 slope resistance should be consulted to determine whether R5 is required.

U1 is arranged with collector connected to primary ground and emitter to the anode of D1. This connection keeps the opto in an electrically "quiet" position in the circuit. If the opto was instead placed on the cathode side of D1, it would become

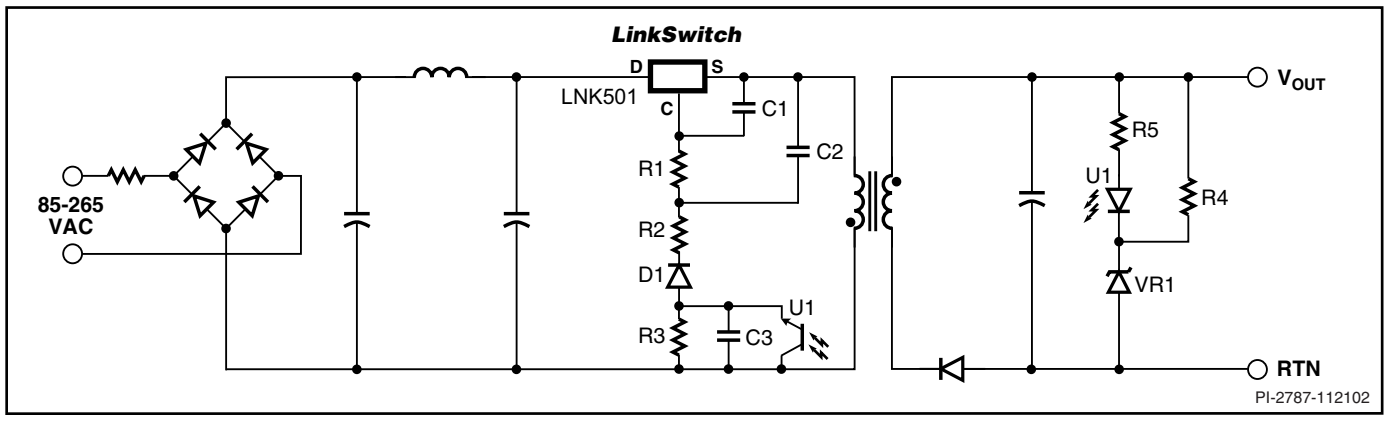


Figure 6. Power Supply Outline Schematic with Optocoupler Feedback.

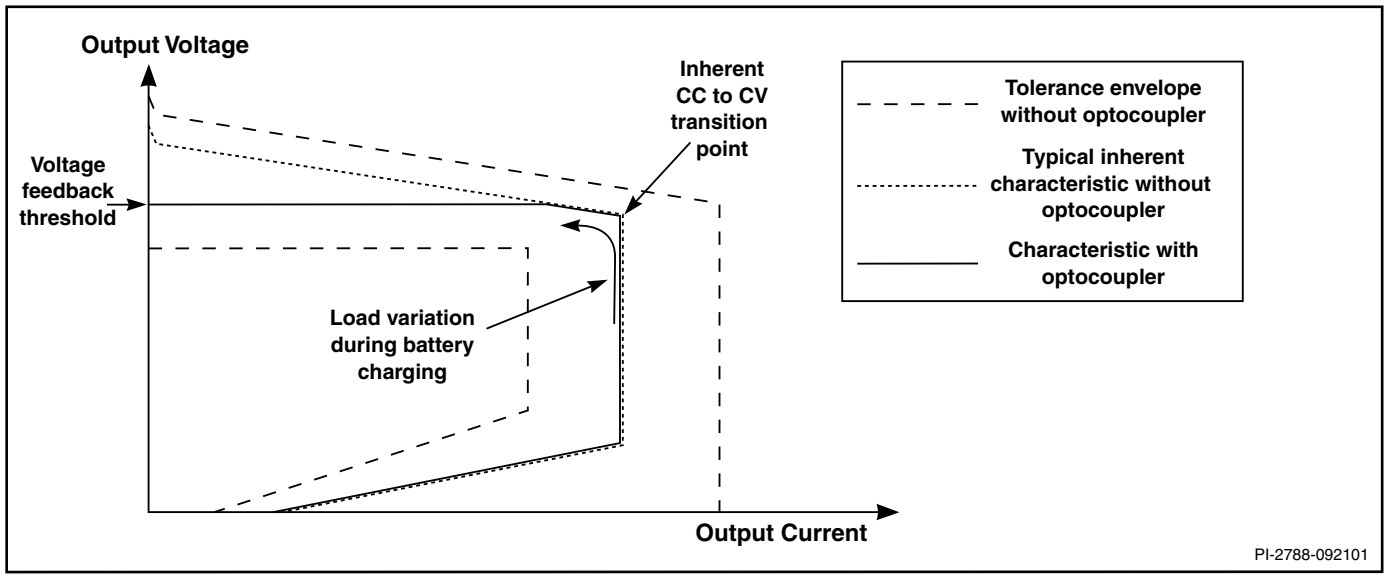


Figure 7. Influence of the Optocoupler on the Power Supply Output Characteristic.

a switching node, generating additional common mode EMI currents through its internal parasitic capacitance.

The feedback configuration in Figure 6 is simply a resistive divider made up of R1 and R3 with D1, R2, C1 and C2 rectifying, filtering and smoothing the primary winding voltage signal. The optocoupler therefore effectively adjusts the resistor divider ratio to control the DC voltage across R1 and therefore, the feedback current received by the LinkSwitch CONTROL pin.

When the power supply operates in the constant current (CC) region, for example when charging a battery, the output voltage is below the voltage feedback threshold defined by U1 and VR1 and the optocoupler is fully off. In this region, the circuit behaves exactly as previously described with reference to Figure 5 where the reflected voltage increases with increasing output voltage and the LinkSwitch internal current limit is adjusted to provide an approximate CC output characteristic. Note that for similar output characteristics in the CC region, the value of R1 in Figure 5 will be equal to the value of R1 + R3 in Figure 6.

When the output reaches the voltage feedback threshold set by U1 and VR1, the optocoupler turns on. Any further increase in the power supply output voltage results in the U1 transistor current increasing, which increases the percentage of the reflected voltage appearing across R1. The resulting increase in the LinkSwitch CONTROL current reduces the duty cycle according to Figure 4 and therefore, maintains the output voltage regulation.

Normally, R1 and R3 are chosen to be equal in value. However, increasing R3 (while reducing R1 to keep R1 + R3 constant) increases loop gain in the CV region, improving load regulation. The extent to which R3 can be increased is limited by opto transistor voltage and dissipation ratings and should be fully tested before finalizing a design. The values of C2 and C3 are less important other than to make sure they are large enough to have very little influence on the impedance of the voltage division circuit set up by R1, R3 and U1 at the switching frequency. Normally, the values of C2 and C3 in Figure 6 are chosen equal to the value of C2 in Figure 5, though the voltage rating may be reduced depending on the relative values of R1 and R2 discussed above. See Applications section for typical values of components.

Figure 7 shows the influence of optocoupler feedback on the output characteristic. The envelope defined by the dashed lines represent the worst case power supply DC output voltage and current tolerances (unit-to-unit and over the input voltage range) if an optocoupler is not used. A typical example of an inherent (without optocoupler) output characteristic is shown dotted. This is the characteristic that would result if U1, R4 and VR1 were removed. The optocoupler feedback results in the characteristic shown by the solid line. The load variation arrow in Figure 7 represents the locus of the output characteristic normally seen during a battery charging cycle. The two characteristics are identical as the output voltage rises but then separate as shown when the voltage feedback threshold is reached. This is the characteristic seen if the voltage feedback threshold is above the output voltage at the inherent CC to CV transition point also indicated in Figure 7.

Figure 8 shows a case where the voltage feedback threshold is set below the voltage at the inherent CC to CV transition point. In this case, as the output voltage rises, the secondary feedback circuit takes control before the inherent CC to CV transition occurs. In an actual battery charging application, this simply limits the output voltage to a lower value.

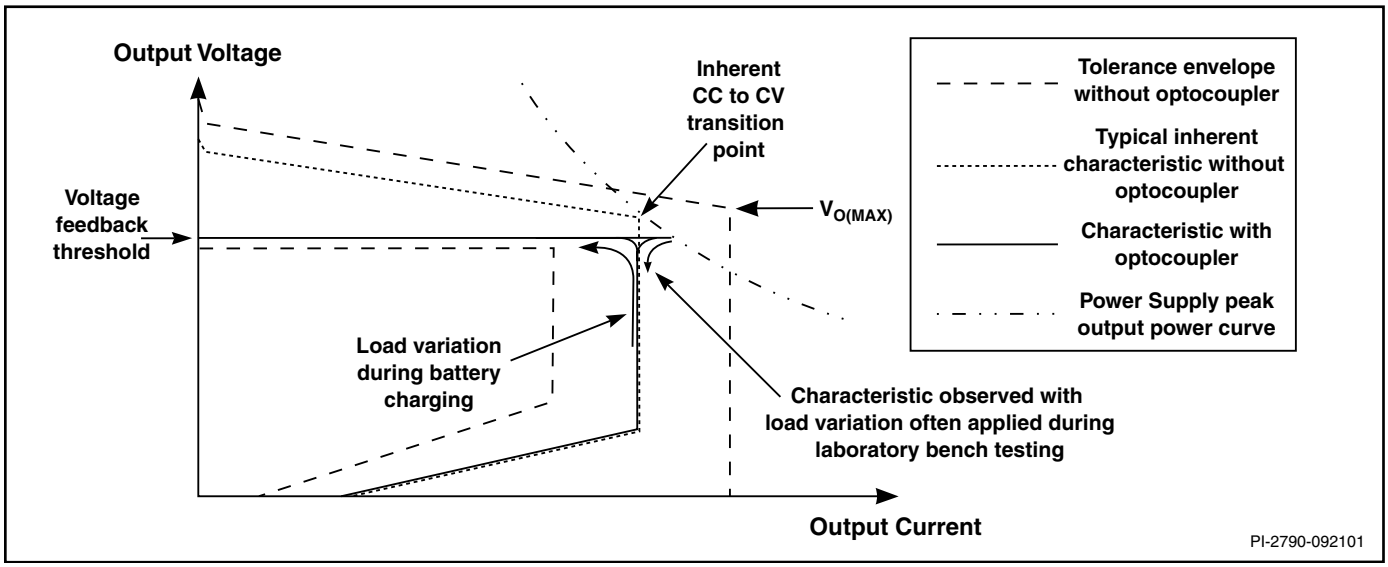


Figure 8. Output Characteristic with Optocoupler Regulation (Reduced Voltage Feedback Threshold).

However, in laboratory bench tests, it is often more convenient to test the power supply output characteristic starting from a low output current and gradually increasing the load. In this case, the optocoupler feedback regulates the output voltage until the peak output power curve is reached as shown in Figure 8. Under these conditions, the output current will continue to rise until the peak power point is reached and the optocoupler turns off. Once the optocoupler is off, the CONTROL pin feedback current is determined only by R1 and R3 and the output current therefore folds back to the inherent CC characteristic as shown. Since this type of load transition does not normally occur in a battery charger, the output current never overshoots the inherent constant current value in the actual application.

In some applications it may be necessary to avoid any output current overshoot, independent of the direction of load variation. To achieve this goal, the minimum voltage feedback threshold should be set at $V_{O(MAX)}$. This will ensure that the voltage at the CC to CV transition point of the inherent characteristic will always occur below the voltage feedback threshold. However, the output voltage tolerance is then increased, since the inherent CV characteristic tolerance below $V_{O(MAX)}$ is added to the tolerance of the optocoupler feedback circuit.

Applications Example

The circuit shown in Figure 9 shows a typical implementation of an approximate constant voltage / constant current (CV/CC) charger using LinkSwitch. This design delivers 2.75 W with a nominal peak power point voltage of 5.5 V and a current of 500 mA. Efficiency is greater than 70% over an input range of 85 VAC to 265 VAC.

The bridge rectifier, BR1, rectifies the AC input. Resistor RF1 is a fusible type providing protection from primary side short circuits. The rectified AC is smoothed by C1 and C2 with inductor L1 forming a pi-filter in conjunction with C1 and C2 to filter conducted EMI. The switching frequency of 42 kHz allows such a simple EMI filter to be used without the need for a Y capacitor while still meeting international EMI standards.

When power is applied, high voltage DC appears at the DRAIN pin of LinkSwitch (U1). The CONTROL pin capacitor C3 is then charged through a switched high voltage current source connected internally between the DRAIN and CONTROL pins. When the CONTROL pin reaches approximately 5.6 V relative to the SOURCE pin, the internal current source is turned off. The internal control circuitry is activated and the high voltage MOSFET starts to switch, using the energy in C3 to power the IC.

When the MOSFET is on, the high voltage DC bus is connected to one end of the transformer primary, the other end being connected to primary return. As the current ramps in the primary of flyback transformer T1, energy is stored. This energy is delivered to the output when the MOSFET turns off each switching cycle.

The secondary of the transformer is rectified and filtered by D6 and C5 to provide the DC output to the load.

LinkSwitch dramatically simplifies the secondary side by controlling both the constant voltage and constant current regions entirely from the primary side. This is achieved by monitoring the primary-side V_{OR} (voltage output reflected).

Diode D5 and capacitor C4 form the primary clamp network. This both limits the peak drain voltage due to leakage inductance and provides a voltage across C4, which is equal to the V_{OR} plus an error due to the parasitic leakage inductance. Resistor R2 filters the leakage inductance spike and reduces the error in the value of the V_{OR}. Resistor R1 converts this voltage into a current that is fed into the CONTROL pin to regulate the output.

During CV operation the output is regulated through control of the duty cycle. As the current into the CONTROL pin exceeds approximately 2 mA, the duty cycle begins to reduce, reaching 30% at a CONTROL pin current of 2.3 mA.

Under light or no-load conditions, when the duty cycle reaches approximately 4%, the switching frequency is reduced to lower energy consumption.

If the output load is increased beyond the peak power point (defined by $0.5 \cdot L_P \cdot I_{LIM}^2 \cdot f$), the output voltage and V_{OR} falls. The reduced CONTROL pin current will lower the internal LinkSwitch current limit (current limit control) providing an approximately constant current output characteristic. If the load is increased and the CONTROL pin current falls below approximately 1 mA, the CONTROL pin capacitor C3 will discharge and the supply enters auto-restart.

Current limit control removes the need for any secondary side current sensing components (sense resistor, transistor, opto coupler and associated components). Removing the secondary sense circuit dramatically improves efficiency, giving the associated benefit of reduced enclosure size.

Key Application Considerations

Design Output Power

Table 1 (front page) shows the maximum continuous output power that can be obtained under the following conditions:

1. The minimum DC input bus voltage is 90 V or higher. This corresponds to a filter capacitor of 3 µF/W for universal input and 1 µF/W for 230 VAC or 115 VAC input with doubler input stage.
2. Design is a discontinuous mode flyback converter, with nominal primary inductance value and a V_{OR} in the range 40 V to 60 V. Continuous mode designs can result in loop instability and are therefore not recommended.

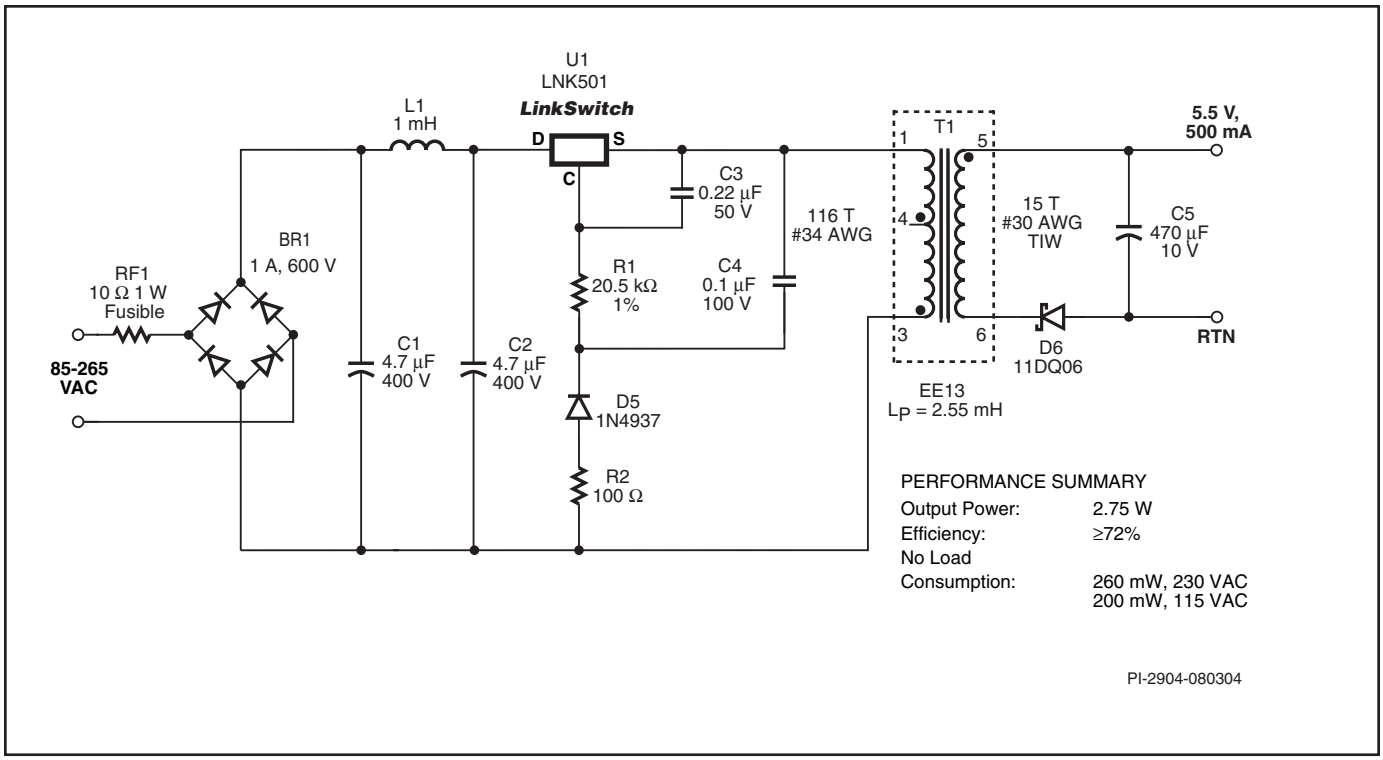


Figure 9. 2.75 W Constant Voltage/Constant Current (CV/CC) Charger using LinkSwitch.

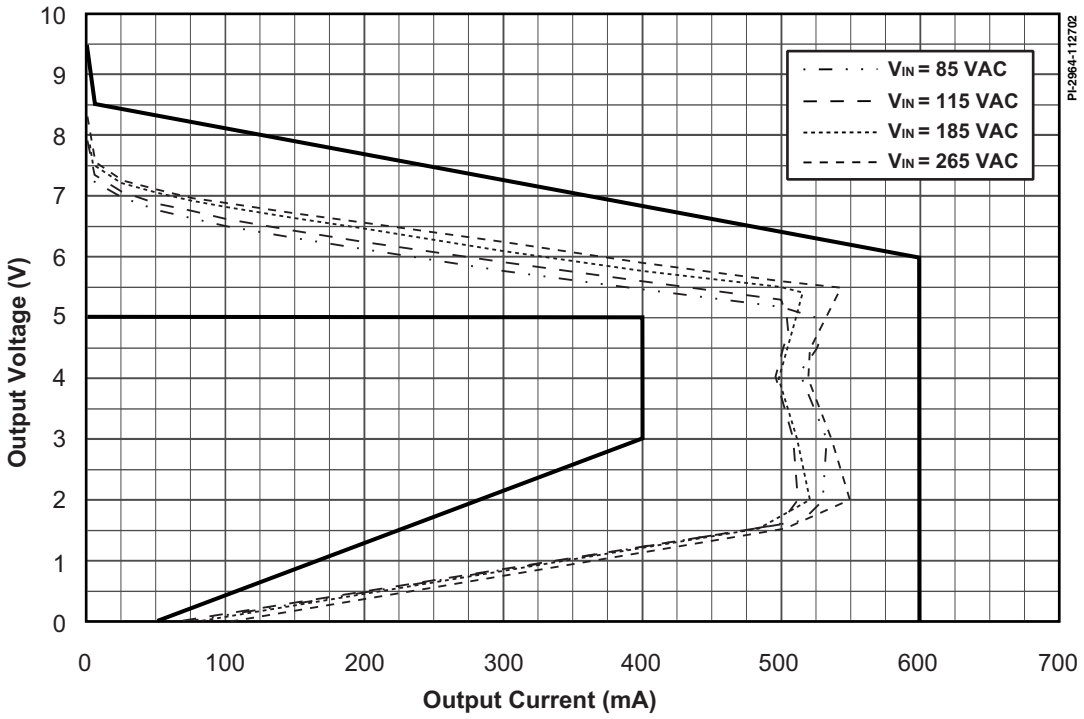


Figure 10. Measured Output Characteristic of the Circuit in Figure 9.

3. A secondary output of 5 V with a Schottky rectifier diode.
4. Assumed efficiency of 70%.
5. The part is board mounted with SOURCE pins soldered to sufficient area of copper to keep the die temperature at or below 100 °C.
6. An output cable with a total resistance of 0.2 Ω.

In addition to the thermal environment (sealed enclosure, ventilated, open frame, etc), the maximum power capability of LinkSwitch in a given application depends on transformer core size, efficiency, primary inductance tolerance, minimum specified input voltage, input storage capacitance, output voltage, output diode forward drop, etc., and can be different from the values shown in Table 1.

In designs not required to meet 300 mW no-load consumption, the transformer can be designed with higher V_{OR} to extend power capability as noted in the following section.

Transformer Design

To provide an approximately CV/CC output, the transformer should be designed to be discontinuous; all the energy stored in the transformer is transferred to the secondary during the MOSFET off time. Energy transfer in discontinuous mode is independent of line voltage.

The peak power point prior to entering constant current operation is defined by the maximum power transferred by the transformer. The power transferred is given by the expression $P = 0.5 \cdot L_P \cdot I^2 \cdot f$, where L_P is the primary inductance, I^2 is the primary peak current squared and f is the switching frequency.

To simplify analysis, the data sheet parameter table specifies an I^2f coefficient. This is the product of current limit squared and switching frequency normalized to the feedback parameter I_{DCT}. This provides a single term that specifies the variation of the peak power point in the power supply due to LinkSwitch.

As primary inductance tolerance is part of the expression that determines the peak output power point (start of the CC characteristic) this parameter should be well controlled. For an estimated overall constant current tolerance of ±20% the primary inductance tolerance should be ±10% or better. This is achievable using standard low cost, center leg gapping techniques where the gap size is typically 0.08 mm or larger. Smaller gap sizes are possible but require non-standard, tighter ferrite A_L tolerances.

Other gapping techniques such as film gapping allow tighter tolerances (±7% or better) with associated improvements in the tolerance of the peak power point. Please consult your transformer vendor for guidance.

Core gaps should be uniform. Uneven core gapping, especially with small gap sizes, may cause variation in the primary inductance with flux density (partial saturation) and make the constant current region non-linear. To verify uniform gapping it is recommended that the primary current wave-shape be examined while feeding the supply from a DC source. The gradient is defined as di/dt = V/L and should remain constant throughout the MOSFET on time. Any change in gradient of the current ramp is an indication of uneven gapping.

Measurements made using a LCR bridge should not be solely relied upon; typically these instruments only measure at currents of a few milliamps. This is insufficient to generate high enough flux densities in the core to show uneven gapping.

For a typical EE13 core using center leg gapping, a 0.08 mm gap (A_{LG} of 190 nH/t^2) allows a primary inductance tolerance of ±10% to be maintained in standard high volume production. This allows the EE13 to be used in designs up to 2.75 W with less than 300 mW no-load consumption. If film gapping is used then this increases to 3 W. Moving to a larger core, EE16 for example, allows a 3 W output with center leg gapping.

The transformer turns ratio should be selected to give a V_{OR} (output voltage reflected through secondary to primary turns ratio) of 40 V to 60 V. In designs not required to meet 300 mW no-load consumption targets, the transformer can be designed with higher V_{OR} as long as discontinuous mode operation is maintained. This increases the output power capability. For example, a 230 VAC input design using an EE19 transformer core with V_{OR} >70 V, is capable of delivering up to 5 W typical output power. Note: the linearity of the CC region of the power supply output characteristic is influenced by V_{OR}. If this is an important aspect of the application, the output characteristic should be checked before finalizing the design.

Output Characteristic Variation

Both the device tolerance and external circuit govern the overall tolerance of the LinkSwitch output characteristic. Estimated peak power point tolerances for a 2.75 W design are ±10% for voltage and ±20% for current limit for overall variation in high volume manufacturing. This includes device and transformer tolerances and line variation. Lower power designs may have poorer constant current linearity.

As the output load reduces from the peak power point, the output voltage will tend to rise due to tracking errors compared to the load terminals. Sources of these errors include the output cable drop, output diode forward voltage and leakage inductance, which is the dominant cause. As the load reduces, the primary operating peak current reduces, together with the leakage inductance energy, which reduces the peak charging of the clamp capacitor. With a primary leakage inductance of 50 µH, the output voltage typically rises 30% over a 100% to 5% load change.

At very light or no-load, typically less than 2 mA of output current, the output voltage rises due to leakage inductance peak charging of the secondary. This voltage rise can be reduced with a small preload with little change to no-load power consumption.

The output voltage load variation can be improved across the whole load range by adding an optocoupler and secondary reference (Figure 6). The secondary reference is designed to only provide feedback above the normal peak power point voltage to maintain the correct constant current characteristic.

Component Selection

The schematic shown in Figure 5 outlines the key components needed for a LinkSwitch supply.

Clamp diode – D1 Diode D1 should be either a fast (t_{rr} <250 ns) or ultra-fast type (t_{rr} <50 ns), with a voltage rating of 600 V or higher. Fast recovery types are preferred, being typically lower cost. Slow diodes are not recommended; they can allow excessive DRAIN ringing and the LinkSwitch to be reverse biased.

Clamp Capacitor – C2
Capacitor C2 should be a 0.1 µF, 100 V capacitor. Low cost metallized plastic film types are recommended. The tolerance of this part has a very minor effect on the output characteristic so any of the standard ±5%, ±10% or ±20% tolerances are acceptable. Ceramic capacitors are not recommended. The common dielectrics used such as Y5U or Z5U are not stable with voltage or temperature and may cause output instability. Ceramic capacitors with high stability dielectrics may be used but are expensive compared to metallized film types.

CONTROL Pin Capacitor – C1
Capacitor C1 is used during start-up to power LinkSwitch and sets the auto-restart frequency. For designs that have a battery load this component should have a value of 0.22 µF and for resistive loads a value of 1 µF. This ensures there is sufficient time during start-up for the output voltage to reach regulation. Any capacitor type is acceptable with a voltage rating of 10 V or above.

Feedback Resistor – R1 The value of R1 is selected to give a feedback current into the CONTROL pin of approximately 2.3 mA at the peak output power point of the supply. The actual value depends on the V_{OR} selected during design. Any 1%, 0.25 W resistor is suitable.

Output Diode – D2
Either PN fast, PN ultra-fast or Schottky diodes can be used depending on the efficiency target for the supply, Schottky diodes giving higher efficiency then PN diodes. The diode voltage rating should be sufficient to withstand the output voltage plus the input voltage transformed through the turns ratio (a typical V_{OR} of 50 V requires a diode PIV of 50 V). Slow recovery diodes are not recommended (1N400X types).

Output Capacitor – C4
Capacitor C4 should be selected such that its voltage and ripple current specifications are not exceeded.

LinkSwitch Layout considerations

Primary Side Connections
Since the SOURCE pins in a LinkSwitch supply are switching nodes, the copper area connected to SOURCE together with C1, C2 and R1 (Figure 5) should be minimized, within the thermal contraints of the design, to reduce EMI coupling.

The CONTROL pin capacitor C1 should be located as close as possible to the SOURCE and CONTROL pins.

To minimize EMI coupling from the switching nodes on the primary to both the secondary and AC input, the LinkSwitch should be positioned away from the secondary of the transformer and AC input.

Routing the primary return trace from the transformer primary around LinkSwitch and associated components further reduces coupling.

Y Capacitor
If a Y capacitor is required, it should be connected close to the transformer secondary output return pin(s) and the primary bulk capacitor negative return. Such placement will maximize the EMI benefit of the Y capacitor and avoid problems in common-mode surge testing.

Quick Design Checklist

As with any power supply design, all LinkSwitch designs should be verified on the bench to make sure that component specifications are not exceeded under worst case conditions. Note: In a LinkSwitch circuit, the SOURCE is a switching node. This should be taken into consideration during testing. Oscilloscope measurements should be made with probe grounded to DC voltages such as primary return or DC rail but not to SOURCE. Power supply input voltage should always be supplied using an isolation transformer. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that V_{DS} does not exceed 675 V at highest input voltage and peak output power.

2. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output power, verify drain current waveforms at start-up for any signs of transformer saturation and excessive leading edge current spikes. LinkSwitch has a minimum leading edge blanking time of 200 ns to prevent premature termination of the on-cycle. Verify that the leading edge current spike event is below current limit at the end of the 200 ns blanking period.

3. Thermal check – At peak output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for LinkSwitch, transformer, output diode and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of LinkSwitch as specified in the data sheet. Under low line, peak power, a maximum LinkSwitch SOURCE pin temperature of 100 °C is recommended to allow for these variations.

4. Centered output characteristic – Using a transformer with nominal primary inductance and at an input voltage midway between low and high line, verify that the peak power point occurs at the desired nominal output current, with the correct output voltage. If this does not occur then the design should be refined to ensure the overall tolerance limits are met.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations website: www.power.com.

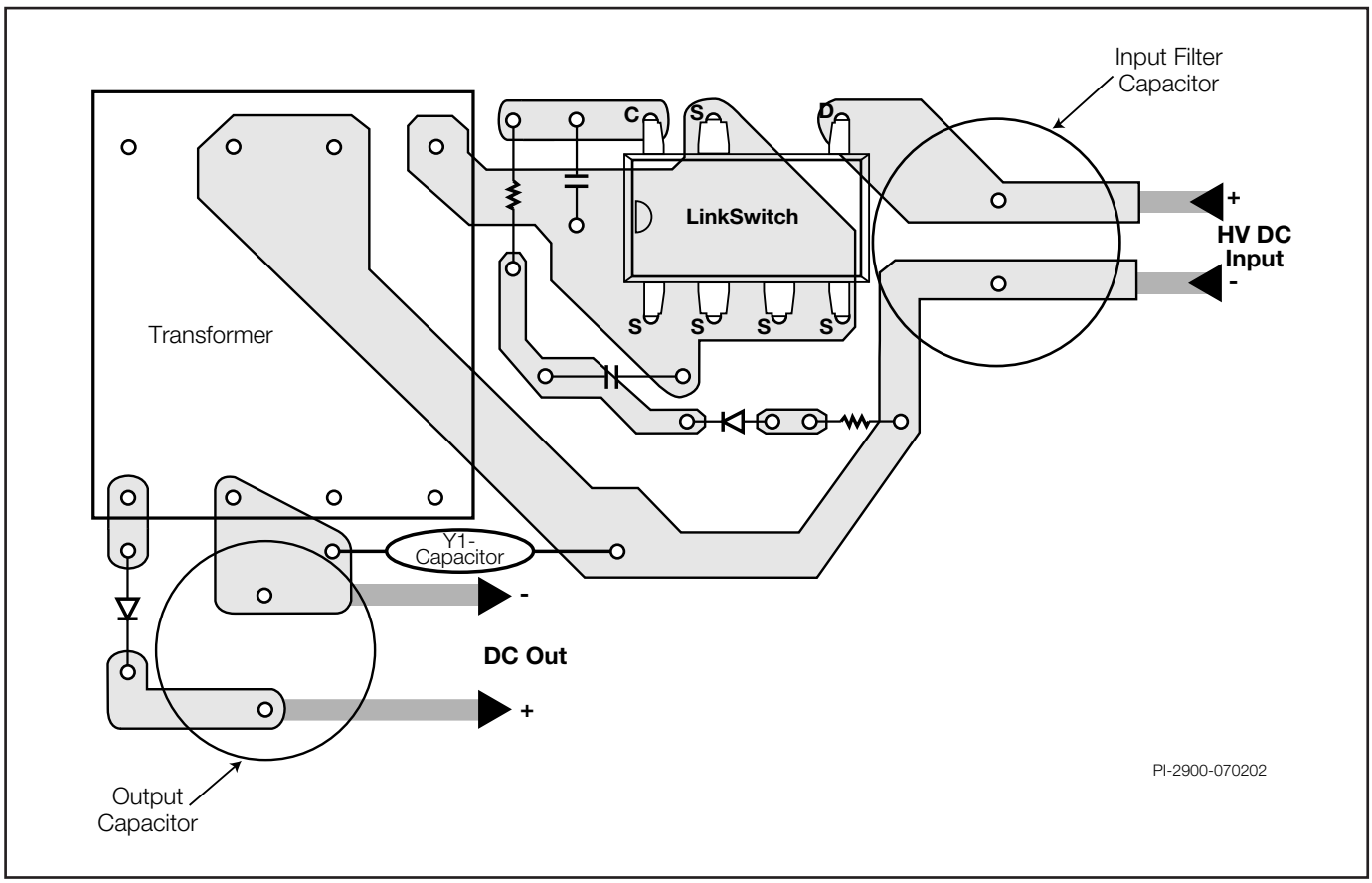


Figure 11. Recommended Circuit Board Layout for LinkSwitch using P Package.

ABSOLUTE MAXIMUM RATINGS(1,4)

DRAIN Voltage ..... -0.3 V to 700 V
DRAIN Peak Current ..... 400 mA
CONTROL Voltage ..... -0.3 V to 9 V
CONTROL Current (not to exceed 9 V) ..... 100 mA
Storage Temperature ..... -65 °C to 150 °C
Operating Junction Temperature(2) ..... -40 °C to 150 °C
Lead Temperature(3) ..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16 in. from case for 5 seconds.
4. Maximum ratings specified may be applied, one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

THERMAL IMPEDANCE

Thermal Impedance: P or G Package:
(θ_{JA}) ..... 70 °C/W(2); 55 °C/W(3)
(θ_{JC})(1) ..... 11 °C/W

Notes:
1. Measured on pin 2 (SOURCE) close to plastic interface.
2. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
3. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 12 (Unless Otherwise Specified)	Min	Typ	Max	Units
CONTROL FUNCTIONS						
Switching Frequency	f_{OSC}	$I_C = I_{DCT}$, T_J = 25 °C	38	42	46	kHz
Low Switching Frequency	$f_{OSC(LOW)}$	Duty Cycle = DC_{LF} T_J = 25 °C	26	30	34	kHz
Duty Cycle at Low Switching Frequency	DC_{LF}	Frequency Switching from f_{OSC} to $f_{OSC(LOW)}$, T_J = 25 °C	2.4	3.8	5.2	%
Low Frequency Duty Cycle Range	$DC_{(RANGE)}$	Frequency = $f_{OSC(LOW)}$, T_J = 25 °C	1.8	3.15	4.5	%
Maximum Duty Cycle	DC_{MAX}	I_C = 1.5 mA	74	77	80	%
PWM Gain	DC_{REG}	$I_C = I_{DCT}$, T_J = 25 °C	-0.45	-0.35	-0.25	%/µA
CONTROL Pin Current at 30% Duty Cycle	I_{DCT}	T_J = 25 °C See Figure 4	2.24	2.30	2.36	mA
CONTROL Pin Voltage	$V_{C(IDCT)}$	$I_C = I_{DCT}$	5.5	5.75	6	V
Dynamic Impedance	Z_C	$I_C = I_{DCT}$, T_J = 25 °C	60	90	120	Ω

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 12 (Unless Otherwise Specified)		Min	Typ	Max	Units
SHUTDOWN/AUTO-RESTART							
CONTROL Pin Charging Current	$I_{C(CH)}$	T_J = 25 °C	V_C = 0 V	-4.5	-3.25	-2	mA
			V_C = 5.15 V	-2.3	-1.3	-0.3	
Control/Supply/ Discharge Current	I_{CD1}	T_J = 25 °C	Output MOSFET Enabled	0.95	1.06	1.14	mA
	I_{CD2}	T_J = 25 °C	Output MOSFET Disabled	0.7	0.9	1.1	
Auto-Restart Threshold Voltage	$V_{C(AR)}$				5.6		V
Auto-Restart Hysteresis Voltage	$V_{C(AR)hyst}$				0.9		V
Auto-Restart Duty Cycle	$DC_{(AR)}$	Short Circuit Applied at Power Supply Output			8		%
Auto-Restart Frequency	$f_{(AR)}$	S2 Open C1 = 0.22 µF (See Figure 12)			300		Hz
CIRCUIT PROTECTION							
Self-Protection Current Limit	I_{LIM}	T_J = 25 °C di/dt = 90 mA/µs See Note C		241	254	267	mA
I^2f Coefficient	I^2f	T_J = 25 °C di/dt = 90 mA/µs See Notes C, D		2547	2710	2873	A^2Hz
Current Limit at Auto-Restart	$I_{LIM(AR)}$	$I_C = I_{CD1}$, T_J = 25 °C			158		mA
Power Up Reset Threshold Voltage	$V_{C(RESET)}$			1.5	2.75	4.0	V
Leading Edge Blanking Time	t_{LEB}	$I_C = I_{DCT}$, T_J = 25 °C		200	300		ns
Current Limit Delay	$t_{IL(D)}$	T_J = 25 °C			100		ns
Thermal Shutdown Temperature		$I_C = I_{DCT}$		125	135		°C
Thermal Shutdown Hysteresis					70		°C

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 12 (Unless Otherwise Specified)		Min	Typ	Max	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 25 mA	T_J = 25 °C		28	32	Ω
			T_J = 100 °C		42	48	
OFF-State Drain Leakage Current	I_{DSS}	V_C = 6.2 V V_D = 560 V, T_A = 125 °C				50	µA
Breakdown Voltage	BV_{DSS}	See Note B V_C = 6.2 V, T_A = 25 °C		700			V
DRAIN Supply Voltage		See Note E		36	50		V

NOTES:

A. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

B. Breakdown voltage may be checked against minimum BV_{DSS} specification by ramping the DRAIN pin voltage up to but not exceeding minimum BV_{DSS}.

C. I_C is increased gradually to obtain maximum current limit at di/dt of 90 mA/µs. Increasing I_C further would terminate the cycle through duty cycle control.

D. This parameter is normalized to I_{DCT} to correlate to power supply output current (it is multiplied by I_{DCT}(nominal)/I_{DCT}).

E. It is possible to start up and operate LinkSwitch at DRAIN voltages well below 36 V. However, the CONTROL pin charging current is reduced, which affects start-up time, auto-restart frequency, and auto-restart duty cycle. Refer to the characteristic graph on CONTROL pin charge current (I_C) vs. DRAIN voltage (Figure 13) for low voltage operation characteristics.

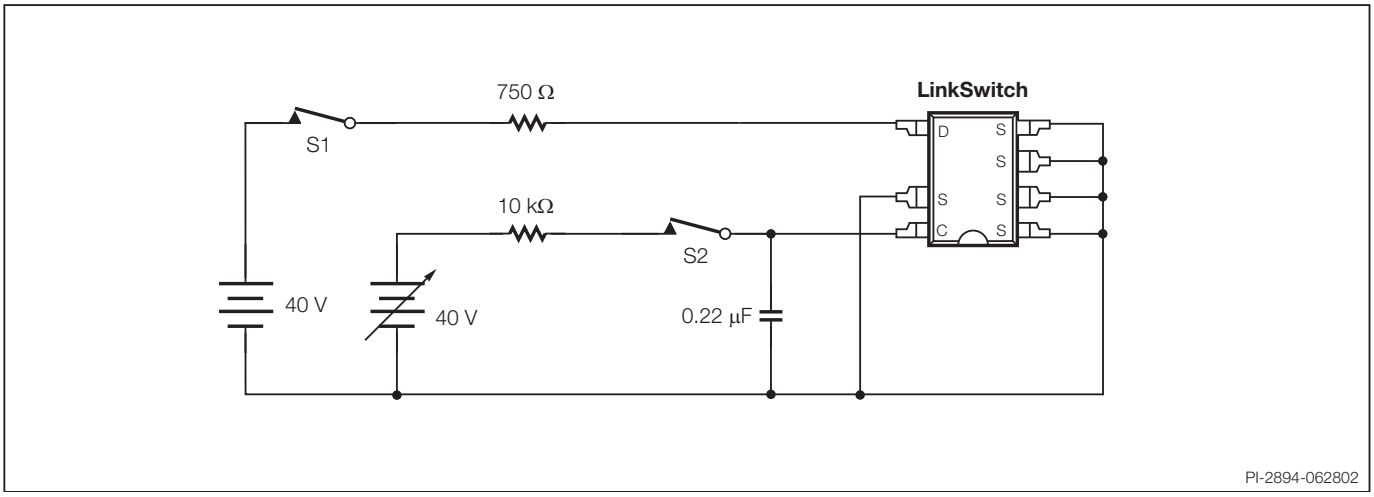


Figure 12. LinkSwitch General Test Circuit.

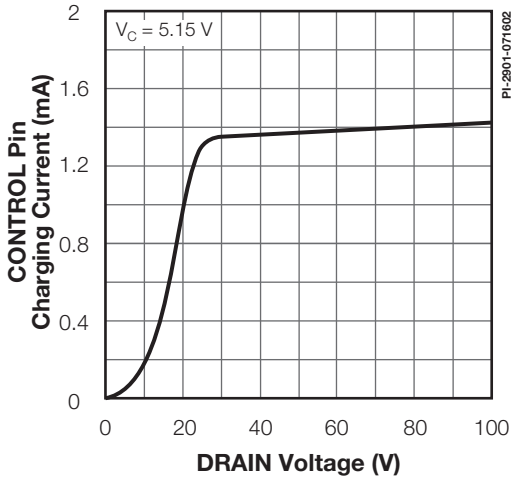


Figure 13. I_C vs. DRAIN Voltage.

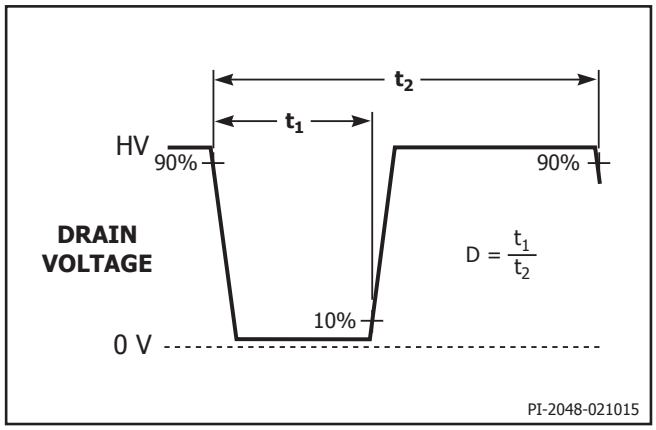


Figure 14. Duty Cycle Measurement.

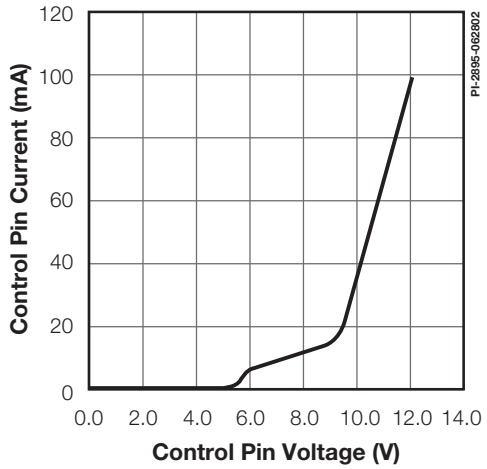


Figure 15. CONTROL Pin I-V Characteristic.

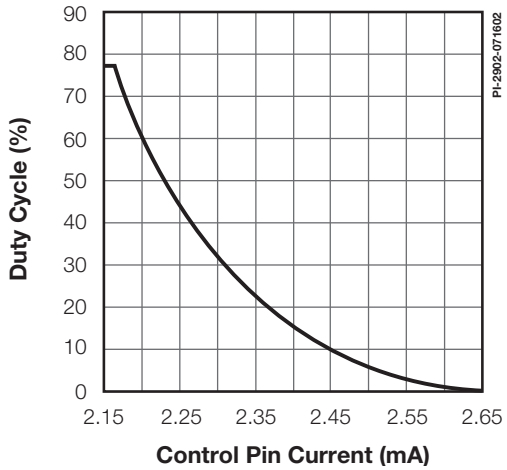


Figure 16. Duty Cycle vs. CONTROL Pin Current.

Typical Performance Characteristics

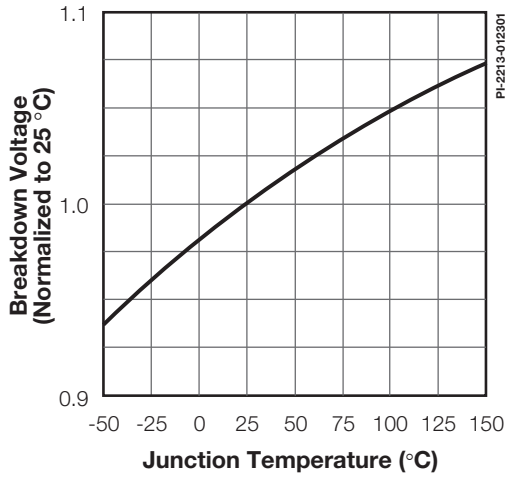


Figure 17. Breakdown Voltage vs. Temperature.

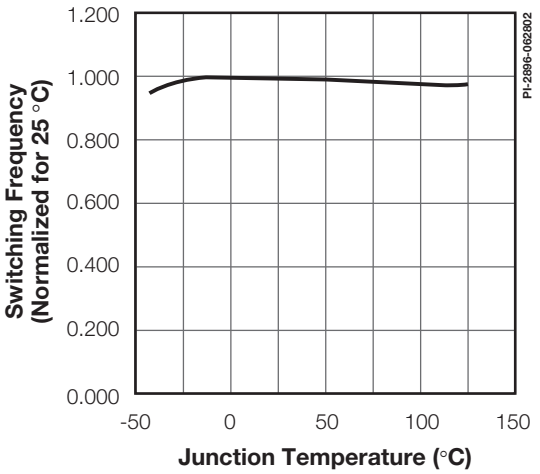


Figure 18. Switching Frequency vs. Temperature.

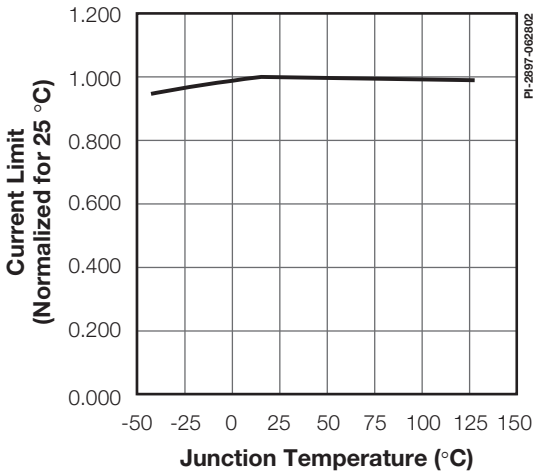


Figure 19. Current Limit vs. Temperature.

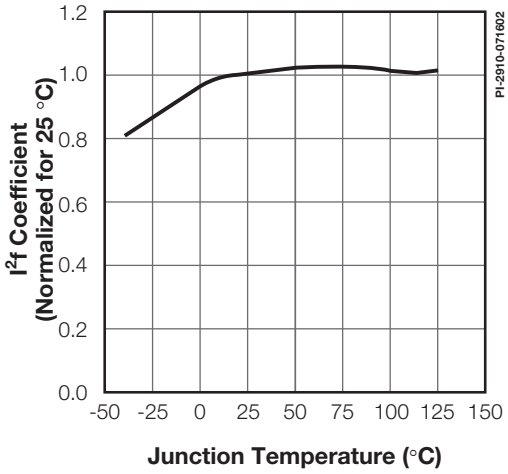


Figure 20. I^2f Coefficient vs. Temperature.

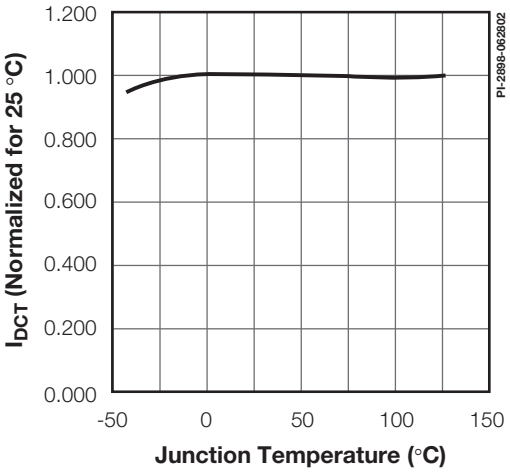


Figure 21. I_{DCT} vs. Temperature.

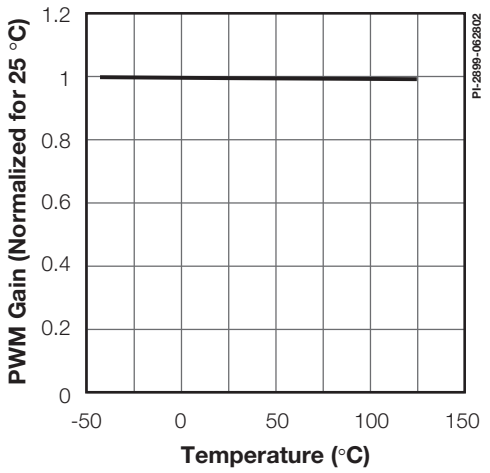


Figure 22. PWM Gain vs. Temperature.

Typical Performance Characteristics (cont.)

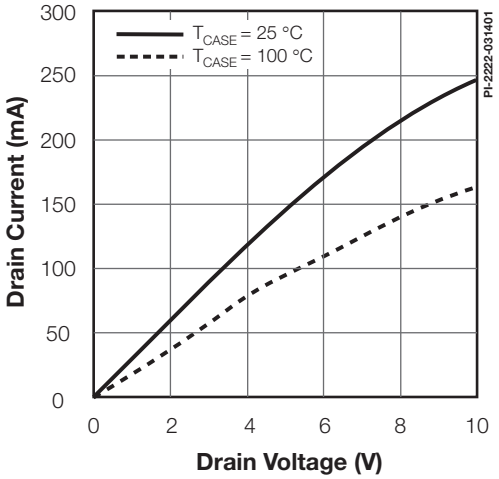
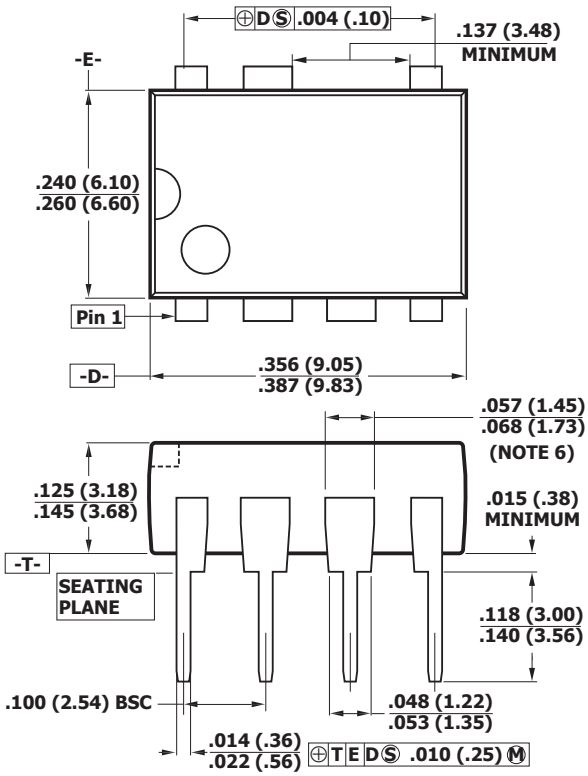
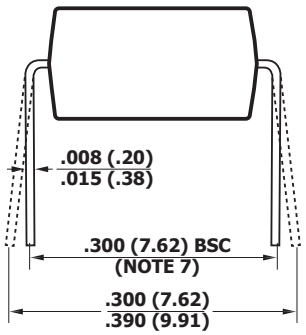


Figure 23. Output Characteristics (DRAIN Current vs. DRAIN Voltage).

PDIP-8B (P Package)





Notes:

1. Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 6 is omitted.
5. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
6. Lead width measured at package body.
7. Lead spacing measured with the leads constrained to be perpendicular to plane T.

P08B

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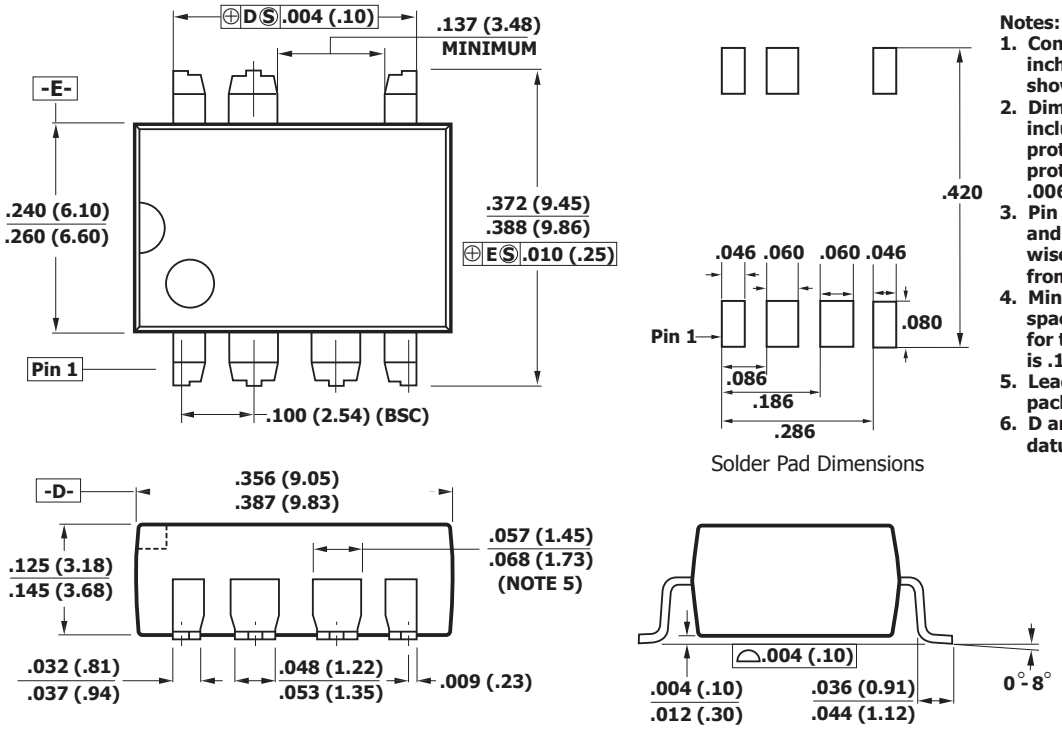
SMD-8B (G Package)



Notes:

1. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
2. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
3. Pin locations start with Pin 1, and continue counter-clock-wise to Pin 8 when viewed from the top. Pin 6 is omitted.
4. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
5. Lead width measured at package body.
6. D and E are referenced datums on the package body.

Part Ordering Information

- **LinkSwitch Product Family**
- **Series Number**
- **Package Identifier**
  - G — Plastic Surface Mount DIP
  - P — Plastic DIP
- **Lead Finish**
  - Blank — Standard (Sn Pb)
  - N — Pure Matte Tin (Pb-Free)
- **Tape & Reel and Other Options**
  - Blank — Standard Configurations
  - TL — Tape & Reel, 1 k pcs minimum, G Package only.

LNK 501 G N - TL

Revision	Notes	Date
D	Released Final Data Sheet.	7/02
E	Enhanced tolerance with optocoupler designs. Updated P and G packages thermal impedance.	8/02
F	Corrected minor errors in text and figures. Updated Figure 6 and text description.	9/02
G	Updated DIP-8B and SMD-8B package descriptions. Updated Table 1 with no-load conditions. Corrected minor errors in text and figures.	4/03
H	Added lead-free ordering information.	12/04
I	Minor error and formatting corrections.	2/05
J	Updated PDIP-8B (P Package) and SMD-8B (G Package) per PCN-16232.	09/16

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