International
IOR Rectifier

IR3508Z

DATA SHEET

XPHASE3™ PHASE IC

DESCRIPTION

The IR3508Z Phase IC combined with any IR *XPhase3*™ Control IC provides a full featured and flexible way to implement a power solution for the latest high performance CPUs and ASICs. The "Control" IC provides overall system control and interfaces with any number of "Phase" ICs which each drive and monitor a single phase of a multiphase converter. The *XPhase3*™ architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

The IR3508Z disables its current sense amplifiers when entering power savings mode. The recommended use for these Phase ICs is for applications without adaptive voltage positioning where two or more power stages will be operating in power savings mode.

FEATURES IR3508Z PHASE IC

- Power State Indicator (PSI) interface provides the capability to maximize the efficiency at light loads.
- Anti-bias circuitry
- 7V/2A gate drivers (4A GATEL sink current)
- Support converter output voltage up to 5.1 V (Limited to VCCL-1.4V)
- Loss-less inductor current sensing
- Phase delay DFF bypassed during PSI assertion mode to improve output ripple performance
- Over-current protection during PSI assertion mode operation
- Feed-forward voltage mode control
- Integrated boot-strap synchronous PFET
- Only four external components per phase
- 3 wire analog bus connects Control and Phase ICs (VID, Error Amp, IOUT)
- 3 wire digital bus for accurate daisy-chain phase timing control without external components
- Debugging function isolates phase IC from the converter
- Self-calibration of PWM ramp, current sense amplifier, and current share amplifier
- Single-wire bidirectional average current sharing
- Small thermally enhanced 20L 4 X 4mm MLPQ package
- RoHS compliant

APPLICATION CIRCUIT

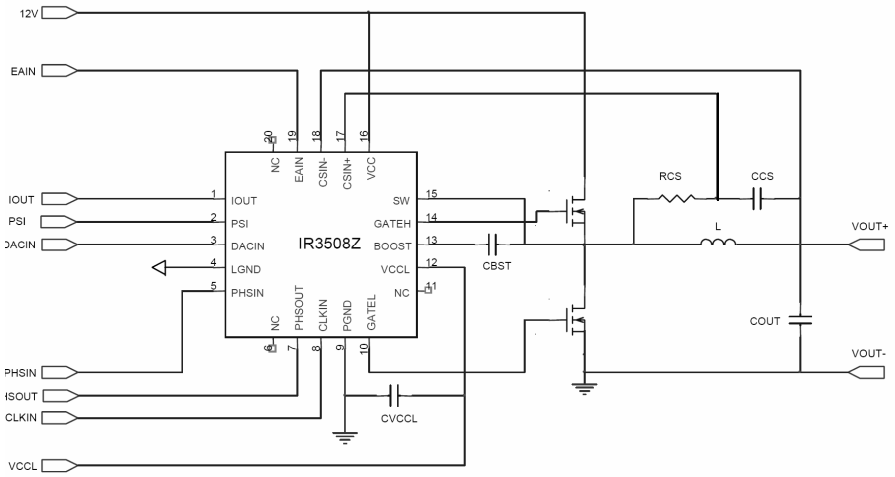


Figure 1 Application Circuit

ORDERING INFORMATION

Part Number	Package	Order Quantity
IR3508ZMTRPBF	20 Lead MLPQ (4 x 4 mm body)	3000 per reel
* IR3508ZMPBF	20 Lead MLPQ (4 x 4 mm body)	100 piece strips

* Samples only

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device, at these or any other conditions, beyond those indicated in the operational sections of the specifications are not implied.

Operating Junction Temperature…….. 0 to 150°C
Storage Temperature Range……-65°C to 150°C
MSL Rating……2
Reflow Temperature…….260°C

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	IOUT	8V	-0.3V	1mA	1mA
2	PSI	8V	-0.3V	1mA	1mA
3	DACIN	3.3V	-0.3V	1mA	1mA
4	LGND	n/a	n/a	n/a	n/a
5	PHSIN	8V	-0.3V	1mA	1mA
6	NC	n/a	n/a	n/a	n/a
7	PHSOUT	8V	-0.3V	2mA	2mA
8	CLKIN	8V	-0.3V	1mA	1mA
9	PGND	0.3V	-0.3V	5A for 100ns, 200mA DC	n/a
10	GATEL	8V	-0.3V DC, -5V for 100ns	5A for 100ns, 200mA DC	5A for 100ns, 200mA DC
11	NC	n/a	n/a	n/a	n/a
12	VCCL	8V	-0.3V	n/a	5A for 100ns, 200mA DC
13	BOOST	40V	-0.3V	1A for 100ns, 100mA DC	3A for 100ns, 100mA DC
14	GATEH	40V	-0.3V DC, -5V for 100ns	3A for 100ns, 100mA DC	3A for 100ns, 100mA DC
15	SW	34V	-0.3V DC, -5V for 100ns	3A for 100ns, 100mA DC	n/a
16	VCC	34V	-0.3V	n/a	10mA
17	CSIN+	8V	-0.3V	1mA	1mA
18	CSIN-	8V	-0.3V	1mA	1mA
19	EAIN	8V	-0.3V	1mA	1mA
20	NC	n/a	n/a	n/a	n/a

Note:
1. Maximum GATEH – SW = 8V
2. Maximum BOOST – GATEH = 8V

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

8.0V ≤ V_{CC} ≤ 28V, 4.75V ≤ V_{CCL} ≤ 7.5V, 0 °C ≤ T_J ≤ 125 °C. 0.5V ≤ V(DACIN) ≤ 1.6V, 500kHz ≤ CLKIN ≤ 9MHz, 250kHz ≤ PHSIN ≤1.5MHz.

ELECTRICAL CHARACTERISTICS

The electrical characteristics table lists the parametric range guaranteed to be within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.
C_{GATEH} = 3.3nF, C_{GATEL} = 6.8nF (unless otherwise specified)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Gate Drivers					
GATEH Source Resistance	BOOST – SW = 7V. Note 1		1.0	2.5	Ω
GATEH Sink Resistance	BOOST – SW = 7V. Note 1		1.0	2.5	Ω
GATEL Source Resistance	VCCL – PGND = 7V. Note 1		1.0	2.5	Ω
GATEL Sink Resistance	VCCL – PGND = 7V. Note 1		0.4	1.0	Ω
GATEH Source Current	BOOST=7V, GATEH=2.5V, SW=0V.		2.0		A
GATEH Sink Current	BOOST=7V, GATEH=2.5V, SW=0V.		2.0		A
GATEL Source Current	VCCL=7V, GATEL=2.5V, PGND=0V.		2.0		A
GATEL Sink Current	VCCL=7V, GATEL=2.5V, PGND=0V.		4.0		A
GATEH Rise Time	BOOST – SW = 7V, measure 1V to 4V transition time		5	10	ns
GATEH Fall Time	BOOST – SW = 7V, measure 4V to 1V transition time		5	10	ns
GATEL Rise Time	VCCL – PGND = 7V, Measure 1V to 4V transition time		10	20	ns
GATEL Fall Time	VCCL – PGND = 7V, Measure 4V to 1V transition time		5	10	ns
GATEL low to GATEH high delay	BOOST = VCCL = 7V, SW = PGND = 0V, measure time from GATEL falling to 1V to GATEH rising to 1V	10	20	40	ns
GATEH low to GATEL high delay	BOOST = VCCL = 7V, SW = PGND = 0V, measure time from GATEH falling to 1V to GATEL rising to 1V	10	20	40	ns
Disable Pull-Down Resistance	Note 1	30	80	130	kΩ
Clock					
CLKIN Threshold	Compare to V(VCCL)	40	45	57	%
CLKIN Bias Current	CLKIN = V(VCCL)	-0.5	0.0	0.5	µA
CLKIN Phase Delay	Measure time from CLKIN<1V to GATEH>1V	40	75	125	ns
PHSIN Threshold	Compare to V(VCCL)	35	50	55	%
PHSOUT Propagation Delay	Measure time from CLKIN > (VCCL * 50%) to PHSOUT > (VCCL *50%). 10pF Load @ 125°C	4	15	35	ns
PHSIN Pull-Down Resistance		30	100	170	kΩ
PHSOUT High Voltage	I(PHSOUT) = -10mA, measure VCCL – PHSOUT	1	0.6		V
PHSOUT Low Voltage	I(PHSOUT) = 10mA		0.4	1	V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
PWM Comparator					
PWM Ramp Slope	Vin=12V	42	52.5	57	mV/ %DC
EAIN Bias Current	0 ≤ EAIN ≤ 3V	-5	-0.3	5	µA
Minimum Pulse Width	Note 1		55	70	ns
Current Sense Amplifier					
CSIN+/- Bias Current		-200	0	200	nA
CSIN+/- Bias Current Mismatch	Note 1	-50	0	50	nA
Input Offset Voltage	CSIN+ = CSIN- = DACIN. Measure input referred offset from DACIN	-1	0	1	mV
Gain	0.5V ≤ V(DACIN) < 1.6V	30.0	32.5	35.0	V/V
Unity Gain Bandwidth	C(IOUT)=10pF. Measure at IOUT. Note 1	4.8	6.8	8.8	MHz
Slew Rate			6		V/µs
Differential Input Range	0.8V ≤ V(DACIN) ≤ 1.6V, Note 1	-10		50	mV
Differential Input Range	0.5V ≤ V(DACIN) < 0.8V, Note 1	-5		50	mV
Common Mode Input Range	Note 1	0		Note2	V
Rout at T_J = 25 °C	Note 1	2.3	3.0	3.7	kΩ
Rout at T_J = 125 °C		3.6	4.7	5.4	kΩ
IOUT Source Current		0.5	1.6	2.9	mA
IOUT Sink Current		0.5	1.4	2.9	mA
Share Adjust Amplifier					
Input Offset Voltage	Note 1	-3	0	3	mV
Gain	CSIN+ = CSIN- = DACIN. Note 1	4	5.0	6	V/V
Unity Gain Bandwidth	Note 1	4	8.5	17	kHz
PWM Ramp Floor Voltage	IOUT Open, Measure relative to DACIN	-116	0	116	mV
Maximum PWM Ramp Floor Voltage	IOUT = DACIN – 200mV. Measure relative to floor voltage.	120	180	240	mV
Minimum PWM Ramp Floor Voltage	IOUT = DACIN + 200mV. Measure relative to floor voltage.	-220	-160	-100	mV
PSI Comparator					
Rising Threshold Voltage	Note 1	520	620	700	mV
Falling Threshold Voltage	Note 1	400	550	650	mV
Hysteresis	Note 1	50	70	120	mV
Resistance		200	500	850	kΩ
Floating Voltage		800		1150	mV

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Body Brake Comparator					
Threshold Voltage with EAIN decreasing	Measure relative to Floor Voltage	-300	-200	-110	mV
Threshold Voltage with EAIN increasing	Measure relative to Floor Voltage	-200	-100	-10	mV
Hysteresis		70	105	130	mV
Propagation Delay	VCCL = 5V. Measure time from EAIN < V(DACIN) (200mV overdrive) to GATEL transition to < 4V.	40	65	90	ns
OVP Comparator					
OVP Threshold	Step V(IOUT) up until GATEL drives high. Compare to V(VCCL)	-1.0	-0.8	-0.4	V
Propagation Delay	V(VCCL)=5V, Step V(IOUT) up from V(DACIN) to V(VCCL). Measure time to V(GATEL)>4V.	15	40	70	ns
Synchronous Rectification Disable Comparator					
Threshold Voltage	The ratio of V(CSIN-) / V(DACIN), below which V(GATEL) is always low.	66	75	86	%
Negative Current Comparator					
Input Offset Voltage	Note1	-16	0	16	mV
Propagation Delay Time	Apply step voltage to V(CSIN+) – V(CSIN-). Measure time to V(GATEL)< 1V.	100	200	400	ns
Bootstrap Diode					
Forward Voltage	I(BOOST) = 30mA, VCCL = 6.8V	360	520	960	mV
Debug Comparator					
Threshold Voltage	Compare to V(VCCL)	-250	-150	-50	mV
General					
VCC Supply Current	8V ≤ V(VCC) < 10V	1.1	4.0	6.1	mA
VCC Supply Current	10V ≤ V(VCC) ≤ 16V	1.1	2.0	4	mA
VCCL Supply Current		3.1	8.0	12.1	mA
BOOST Supply Current	4.75V ≤ V(BOOST)-V(SW)≤ 8V	0.5	1.5	3	mA
DACIN Bias Current		-1.5	-0.75	1	µA
SW Floating Voltage		0.1	0.3	0.4	V

Note 1: Guaranteed by design, but not tested in production
Note 2: V_{CCL}-0.5V or V_{CC} – 2.5V, whichever is lower

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	IOUT	Output of the Current Sense Amplifier is connected to this pin through a 3kΩ resistor. Voltage on this pin is equal to V(DACIN) + 33 [V(CSIN+) – V(CSIN-)]. Connecting all IOUT pins together creates a share bus which provides an indication of the average current being supplied by all the phases. The signal is used by the Control IC for voltage positioning and over-current protection. OVP mode is initiated if the voltage on this pin rises above V(VCCL)- 0.8V.
2	PSI	Logic low is an active low (i.e. low = low power state).
3	DACIN	Reference voltage input from the Control IC. The Current Sense signal and PWM ramp is referenced to the voltage on this pin.
4	LGND	Ground for internal IC circuits. IC substrate is connected to this pin.
5	PHSIN	Phase clock input.
6	NC	No connection.
7	PHSOUT	Phase clock output.
8	CLKIN	Clock input.
9	PGND	Return for low side driver and reference for GATEH non-overlap comparator.
10	GATEL	Low-side driver output and input to GATEH non-overlap comparator.
11	NC	No connection.
12	VCCL	Supply for low-side driver. Internal bootstrap synchronous PFET is connected from this pin to the BOOST pin.
13	BOOST	Supply for high-side driver. Internal bootstrap synchronous PFET is connected between this pin and the VCCL pin.
14	GATEH	High-side driver output and input to GATEL non-overlap comparator.
15	SW	Return for high-side driver and reference for GATEL non-overlap comparator.
16	VCC	Supply for internal IC circuits.
17	CSIN+	Non-Inverting input to the current sense amplifier, and input to debug comparator.
18	CSIN-	Inverting input to the current sense amplifier, and input to synchronous rectification disable comparator.
19	EAIN	PWM comparator input from the error amplifier output of Control IC. Body Braking mode is initiated if the voltage on this pin is less than V(DACIN).
20	NC	No connection.

SYSTEM THEORY OF OPERATION

System Description

The system consists of one control IC and a scalable array of phase converters, each requiring one phase IC. The control IC communicates with the phase ICs using three digital buses, i.e., CLOCK, PHSIN, PHSOUT and three analog buses, i.e., DAC, EA, and IOUT. The digital buses are responsible for switching frequency determination and accurate phase timing control without any external components. The analog buses are used for PWM control and current sharing between interleaved phases. The control IC incorporates all the system functions, i.e., VID, CLOCK signals, error amplifier, fault protections, current monitor, etc. The Phase IC implements the functions required by the converter of each phase, i.e., the gate drivers, PWM comparator and latch, over-voltage protection, phase disable circuit, current sensing and sharing, etc.

PWM Control Method

The PWM block diagram of the *XPhase3*™ architecture is shown in Figure 1. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain and wide-bandwidth voltage type error amplifier is implemented in the controller's design to achieve a fast voltage control loop. Input voltage is sensed by the phase ICs to provide feed-forward control. The feed-forward control compensates the ramp slope based on the change in input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current.

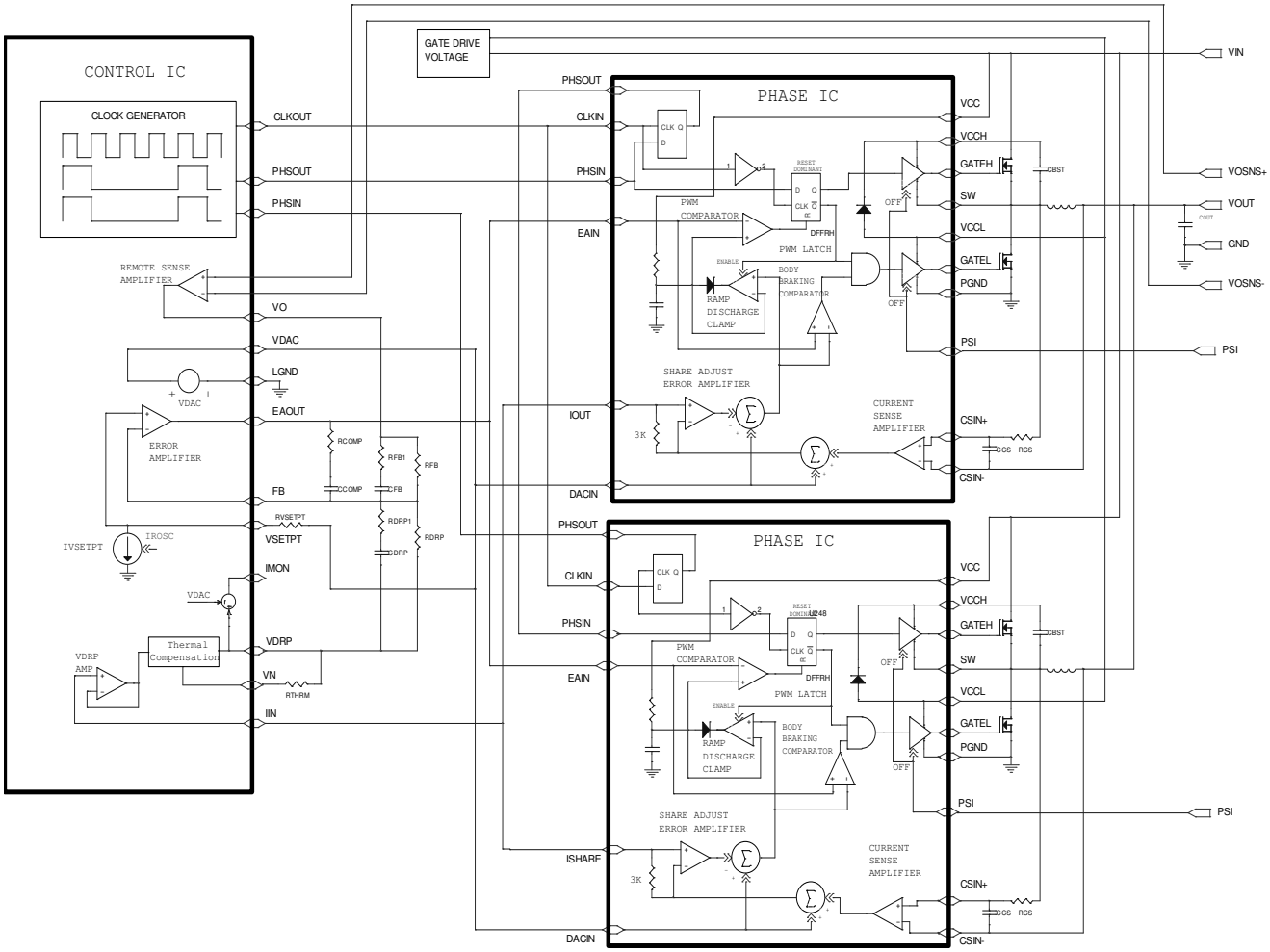


Figure 1: PWM Block Diagram

Frequency and Phase Timing Control

The oscillator is located in the Control IC and the system clock frequency is programmable from 250kHz to 9MHZ by an external resistor. The control IC system clock signal (CLKOUT) is connected to CLKIN of all the phase ICs. The phase timing of the phase ICs is controlled by the daisy chain loop, where the control IC phase clock output (PHSOUT) is connected to the phase clock input (PHSIN) of the first phase IC, and PHSOUT of the first phase IC is connected to PHSIN of the second phase IC, etc. The last phase IC is connected back to PHSIN of the control IC to complete the daisy chain loop. During power up, the control IC sends out clock signals from both CLKOUT and PHSOUT pins and detects the feedback at PHSIN pin to determine the phase number and monitor any fault in the daisy chain loop. When the PSI is asserted (active low), the phases are effectively removed from the daisy chain loop. Figure 2 shows the phase timing for a four phase converter. The switching frequency is set by the resistor ROSC. The clock frequency equals the number of phase times the switching frequency.

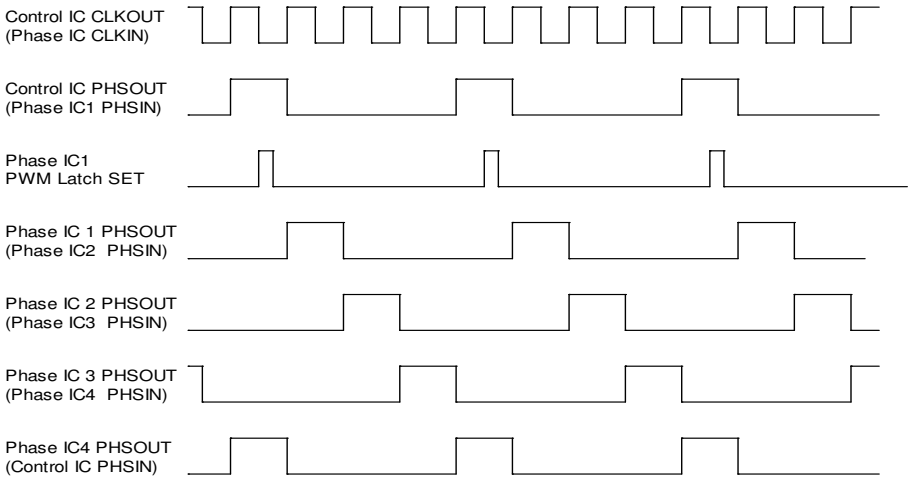


Figure 2: Four Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the phase IC. Upon receiving the falling edge of a clock pulse, the PWM latch is set and the PWM ramp voltage begins to increase. In addition, the low side driver is turned off and the high side driver is turned on after the non-overlap time expires (GATEL < 1V). When the PWM ramp voltage exceeds the error amplifier's output voltage, the PWM latch is reset and the internal ramp capacitor is quickly discharged to the output of the share adjust amplifier and remains discharged until the next clock pulse. This reset latch additionally turns off the high side driver and enables the low side driver after the non-overlap time concludes (Switch Node < 1V).

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go up to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An error amplifier output voltage greater than the common mode input range, of the PWM comparator, results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees that the error amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease, which is appropriate, given that the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide "single cycle transient response." The inductor current will change in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage of the architecture is that differences in ground or input voltage, at the phases, have no effect on operation since the PWM ramps are referenced to VDAC.

Figure 3 depicts PWM operating waveforms under various conditions.

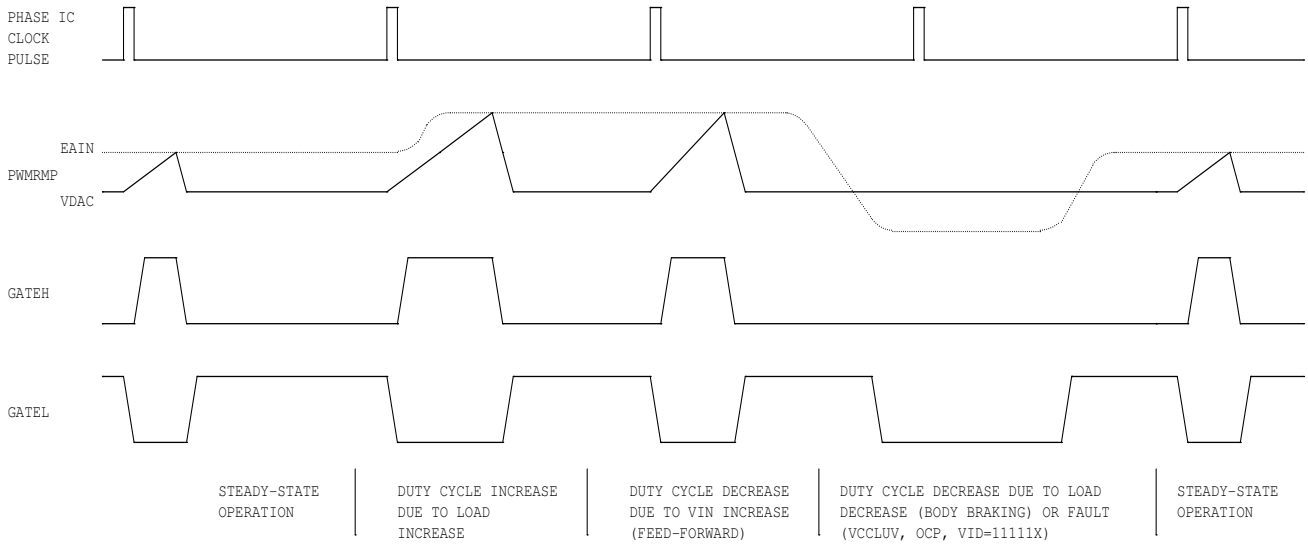


Figure 3: PWM Operating Waveforms

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often comparable to the output voltage, the inductor current slew rate can be increased significantly. This patented technique is referred to as "body braking" and is accomplished through the "body braking comparator" located in the phase IC. If the error amplifier's output voltage drops below the output voltage of the share adjust amplifier in the phase IC, this comparator turns off the low side gate driver.

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 4. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L + sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR (R_L). If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

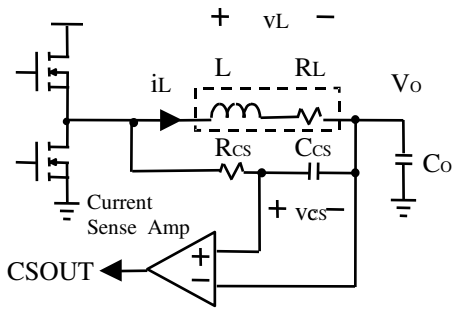


Figure 4: Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the phase IC, as shown in Figure 4. Its gain is nominally 32.5, and the 3850 ppm/ºC increase in inductor DCR should be compensated in the voltage loop feedback path.

The current sense amplifier can accept positive differential input up to 50mV and negative up to -10mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the control IC and other phases through an on-chip 3KΩ resistor connected to the IOUT pin. The IOUT pins of all the phases are tied together and the voltage on the share bus represents the average current through all the inductors and is used by the control IC for voltage positioning and current limit protection. The input offset of this amplifier is calibrated to +/- 1mV in order to reduce the current sense error.

The input offset voltage is the primary source of error for the current share loop. In order to achieve very small input offset error and superior current sharing performance, the current sense amplifier continuously calibrates itself. This calibration algorithm creates ripple on IOUT bus with a frequency of $f_{sw}/896$ in a multiphase architecture.

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each phase IC. The output of the current sense amplifier is compared with the average current at the share bus. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will pull down the starting point of the PWM ramp thereby increasing its duty cycle and output current; if current in a phase is larger than the average current, the share adjust amplifier of the phase will pull up the starting point of the PWM ramp thereby decreasing its duty cycle and output current. The current share amplifier is internally compensated so that the crossover frequency of the current

share loop is much slower than that of the voltage loop and the two loops do not interact. For proper current sharing the output of current sense amplifier should not exceed (VCCL-1.4V) under all operating condition.

IR3508Z THEORY OF OPERATION

Block Diagram

The Block diagram of the IR3508Z is shown in Figure 5, and specific features are discussed in the following sections.

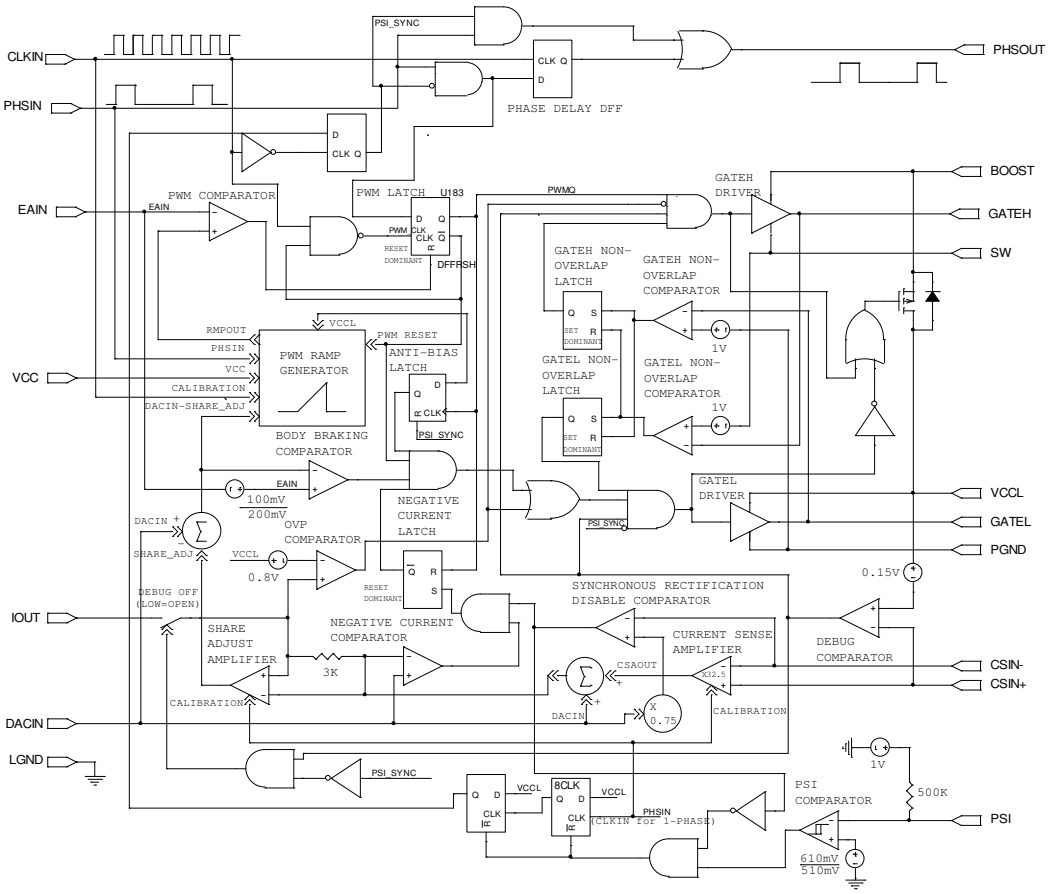


Figure 5: Block diagram

Tri-State Gate Drivers

The gate drivers are design to provide a 2A source and sink peak current (Bottom gate driver can sink 4A). An adaptive non-overlap circuit monitors the voltage on the GATEH and GATEL pins to prevent MOSFET shoot-through current and minimizing body diode conduction. The non-overlap latch is added to eliminate erroneous triggering caused by the switching noise. A fault condition is communicated to the phase IC via the control IC's error amplifier without an additional dedicated signal line. The error amplifier's output is driven low in response to any fault condition detected by the controller, such as VCCL under voltage or output overload, disabling the phase IC and activating Body Braking™. The IR3508Z Body Braking™ comparator detects the low signal at the EAIN and drives the bottom gate output low. This tri-state operation prevents negative inductor current and negative output voltage during power-down.

A synchronous rectification disable comparator is used to detect the converter's CSIN- pin voltage, which represents local converter output voltage. If the voltage is below 75% of VDAC and negative current is detected, GATEL is driven low, which disables synchronous rectification and eliminates negative current during power-up.

The gate drivers are pulled low if the supply voltage falls below the normal operating range. An 80kΩ resistor is connected across the GATEH/GATEL and PGND pins to prevent the GATEH/GATEL voltage from rising due to leakage or other causes under these conditions.

PWM Ramp

Every time the phase IC is powered up, the PWM ramp magnitude is calibrated to generate a 52.5 mV/% ramp (VCC=12V). For example, a 15 % duty ratio will generate a ramp amplitude of 787.5 mV (15 x 52.5 mV) with 12V supply applied to VCC. Feed-forward control is achieved by varying the PWM ramp proportionally with VCC voltage after calibration.

Power State Indicator (PSI) function

From a system perspective, the PSI input is controlled by the system and is forced low when the load current is lower than a preset limit and forced high when load current is higher than the preset limit. IR3508Z can accept an active low signal on its PSI input and force the drivers into tri-state, effectively, forcing the phase IC into an off state. A PSI-assert signal activates three features in the Phase IC. First, it disconnects the IOUT pin from the ISHARE bus (from a system perspective). ISHARE is used to report current and is used for over-current protection. By disconnecting the disabled phase from the ISHARE bus, proper current reporting and over-current protection level are ensured. Secondly, the D Flip-Flop (DFF) is disabled, bypassing the Phase IC from the daisy chain loop. By removing the DFF from the daisy chain, the system ensures that proper phase delay is activated among the active phases. Finally, the gate drivers are forced to tri-state, disabling the phase IC from the power stage. Figure 6 shows the impact of PSI-assert on the gate drivers. After an 8 cycle PHSIN delay followed by a CLK falling edge, the PSI_SYNC goes from 0 to 1. This disables the gate drives and the DFF.

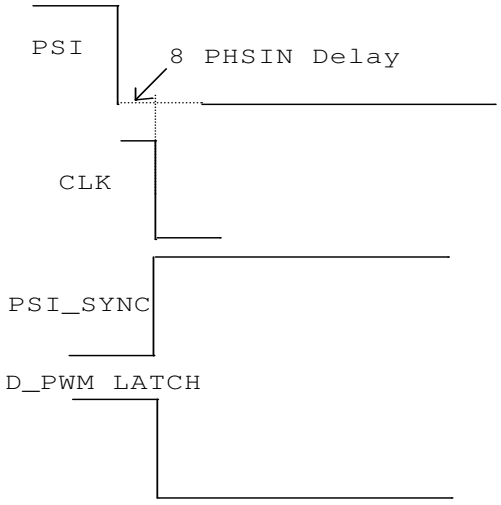


Figure 6: PSI assertion.

Debugging Mode

If the CSIN+ pin is pulled up to VCCL voltage, IR3508Z enters into debugging mode. Both drivers are pulled low and IOUT output is disconnected from the current share bus, which isolates this phase IC from other phases. However, the phase timing from PHSIN to PHSOUT does not change.

Emulated Bootstrap Diode

IR3508Z integrates a PFET to emulate the bootstrap diode. If two or more top MOSFETs are to be driven at higher switching frequency, an external bootstrap diode connected from VCCL pin to BOOST pin may be needed.

Over Voltage Protection (OVP)

The IR3508Z includes over-voltage protection that turns on the low side MOSFET to protect the load in the event of a shorted high-side MOSFET, converter out of regulation, or connection of the converter output to an excessive output voltage. As shown in Figure 7, if IOUT pin voltage is above V(VCCL) – 0.8V, which represents over-voltage condition detected by control IC, the over-voltage latch is set. GATEL drives high and GATEH drives low. The OVP circuit overrides the normal PWM operation and within approximately 150ns will fully turn-on the low side MOSFET, which remains in conduction until IOUT drops below V(VCCL) – 0.8V when over voltage ends. The over voltage fault is latched in control IC and can only be reset by cycling the power to control IC. The error amplifier output (EAIN) is pulled down by control IC and will remain low. The lower MOSFETs alone can not clamp the output voltage however a SCR or N-MOSFET could be triggered with the OVP output to prevent processor damage.

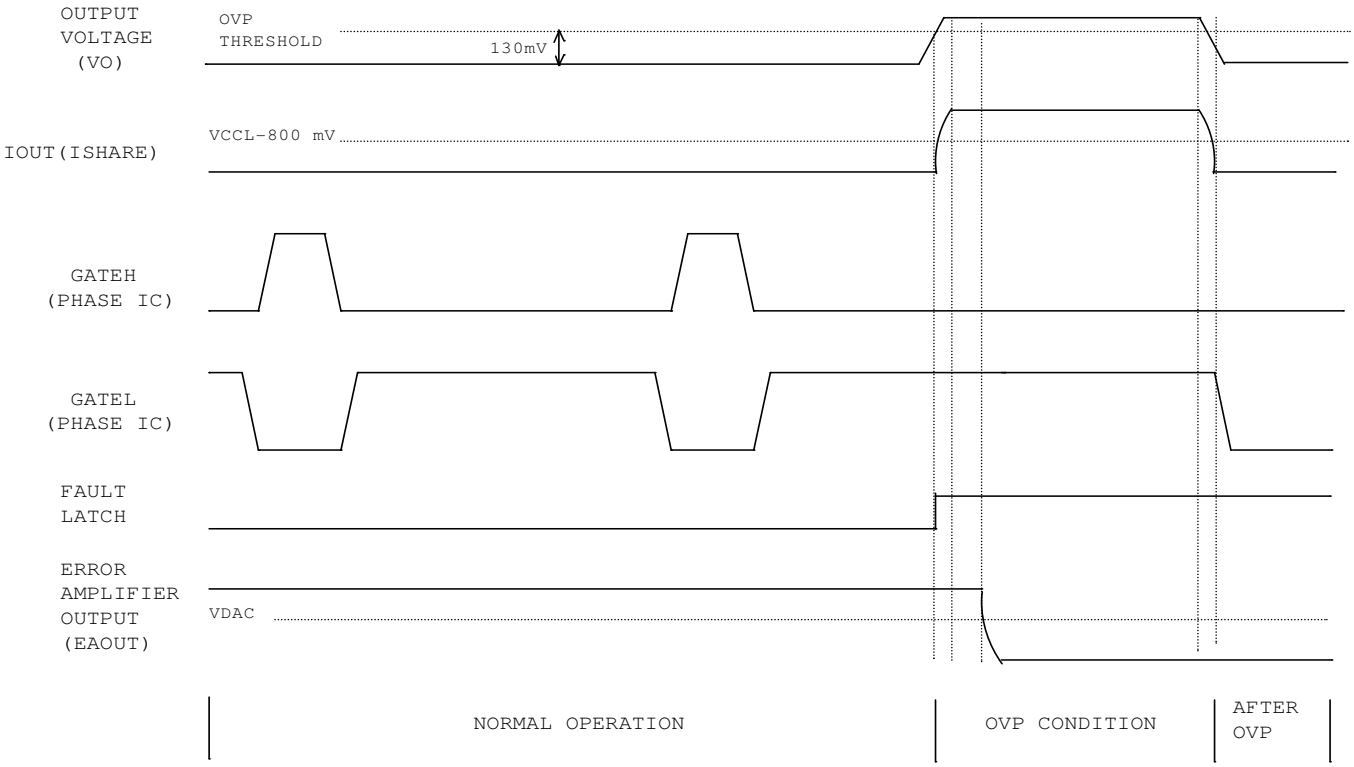


Figure 7: Over-voltage protection waveforms

Operation at Higher Output Voltage

The proper operation of the phase IC is ensured for output voltage up to 5.1V. Similarly, the minimum VCC for proper operation of the phase IC is 8 V. Operating below this minimum voltage, the current sharing performance of the phase IC is affected.

DESIGN PROCEDURES - IR3508Z

Inductor Current Sensing Capacitor *CCS* and Resistor *RCS*

The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor RCS and capacitor CCS in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor CCS represents the inductor current. If the two time constants are not the same, the AC component of the capacitor voltage is different from that of the real inductor current. The time constant mismatch does not affect the average current sharing among the multiple phases, but does affect the current signal IOUT as well as the output voltage during a load current transient if adaptive voltage positioning is being implemented.

Measure the inductance L and the inductor DC resistance RL. Pre-select the capacitor CCS and calculate RCS as follows.

$$R_{CS} = \frac{L/R_L}{C_{CS}} \quad (1)$$

Bootstrap Capacitor *CBST*

Depending on the duty cycle and gate drive current of the phase IC, a capacitor in the range of 0.1uF to 1uF is needed for the bootstrap circuit.

Decoupling Capacitors for Phase IC

A 0.1uF-1uF decoupling capacitor is required at the VCCL pin.

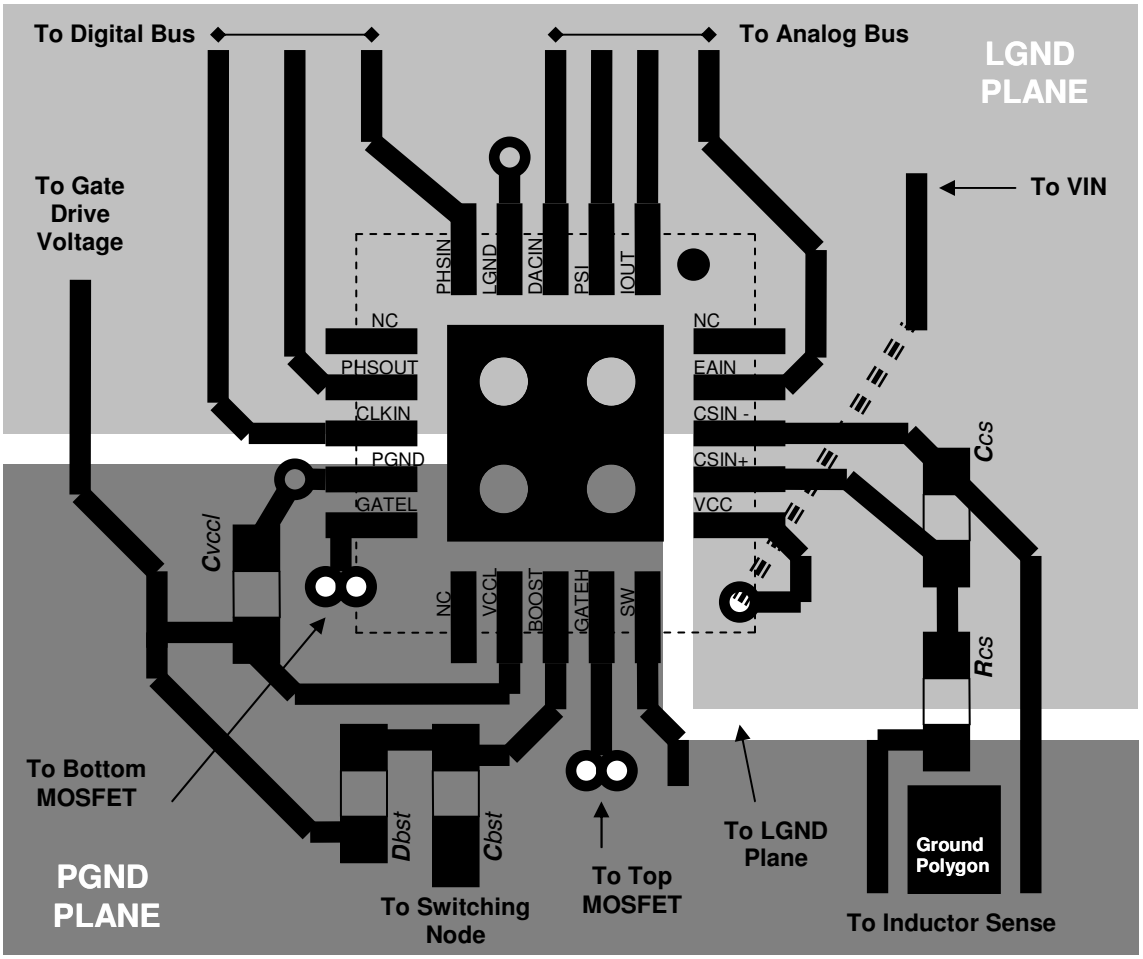
CURRENT SHARE LOOP COMPENSATION

The internal compensation of current share loop ensures that crossover frequency of the current share loop is at least one decade lower than that of the voltage loop so that the interaction between the two loops is eliminated. The crossover frequency of current share loop is approximately 8 kHz.

LAYOUT GUIDELINES

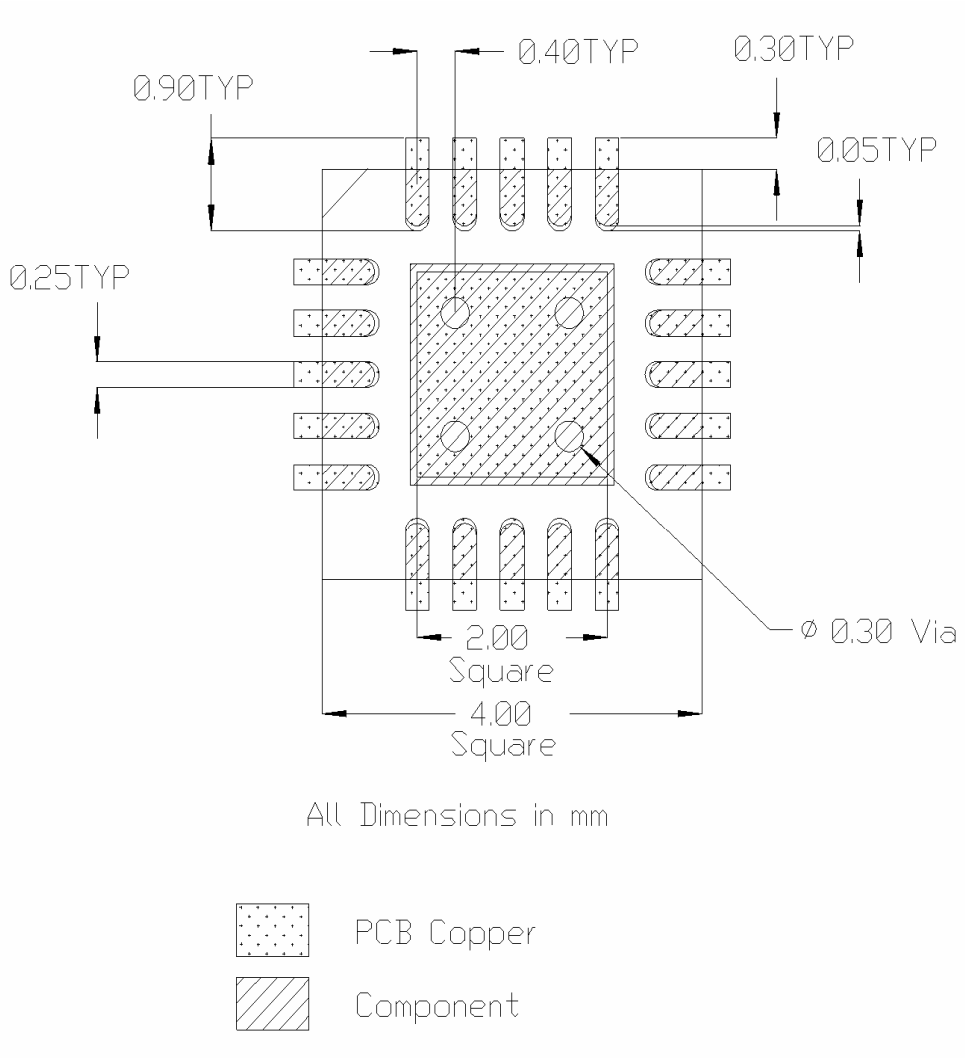
The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout; therefore, minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane, which is then split into signal ground plane (LGND) and power ground plane (PGND).
- Separate analog bus (EAIN, DACIN, and IOUT) from digital bus (CLKIN, PSI, PHSIN, and PHSOUT) to reduce the noise coupling.
- Connect PGND to LGND pins of each phase IC to the ground tab, which is tied to LGND and PGND planes respectively through vias.
- Place current sense resistors and capacitors (R_{CS} and C_{CS}) close to phase IC. Use Kelvin connection for the inductor current sense wires, but separate the two wires by ground polygon. The wire from the inductor terminal to CSIN- should not cross over the fast transition nodes, i.e., switching nodes, gate drive outputs, and bootstrap nodes.
- Place the decoupling capacitors C_{VCC} and C_{VCCL} as close as possible to VCC and VCCL pins of the phase IC respectively.
- Place the phase IC as close as possible to the MOSFETs to reduce the parasitic resistance and inductance of the gate drive paths.
- Place the input ceramic capacitors close to the drain of top MOSFET and the source of bottom MOSFET. Use combination of different packages of ceramic capacitors.
- There are two switching power loops. One loop includes the input capacitors, top MOSFET, inductor, output capacitors and the load; another loop consists of bottom MOSFET, inductor, output capacitors and the load. Route the switching power paths using wide and short traces or polygons; use multiple vias for connections between layers.



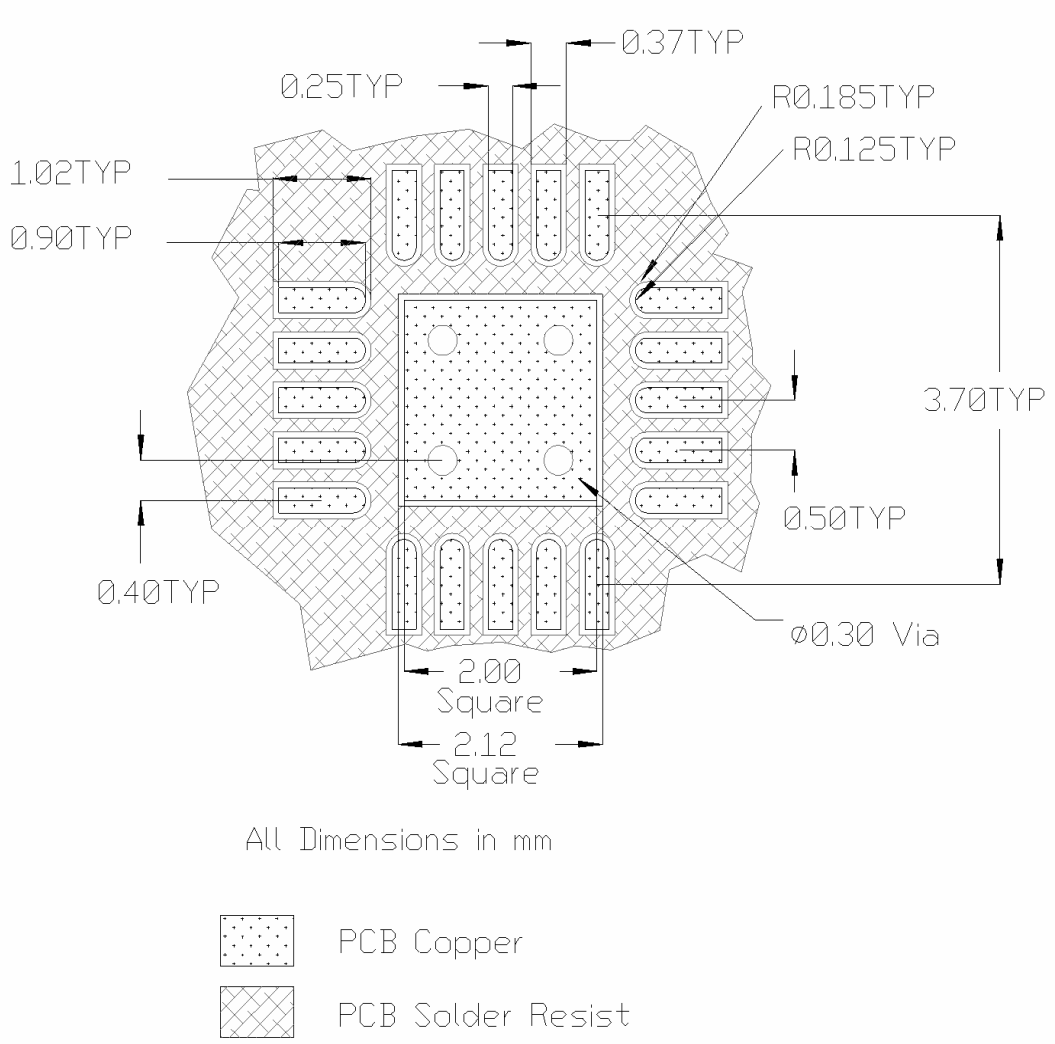
PCB Metal and Component Placement

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- Four 0.3mm diameter vias shall be placed in the pad land spaced at 1.2mm, and connected to ground to minimize the noise effect on the IC and to transfer heat to the PCB.
- No PCB traces should be routed nor vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to rise up from the PCB resulting in poor solder joints to the IC leads.



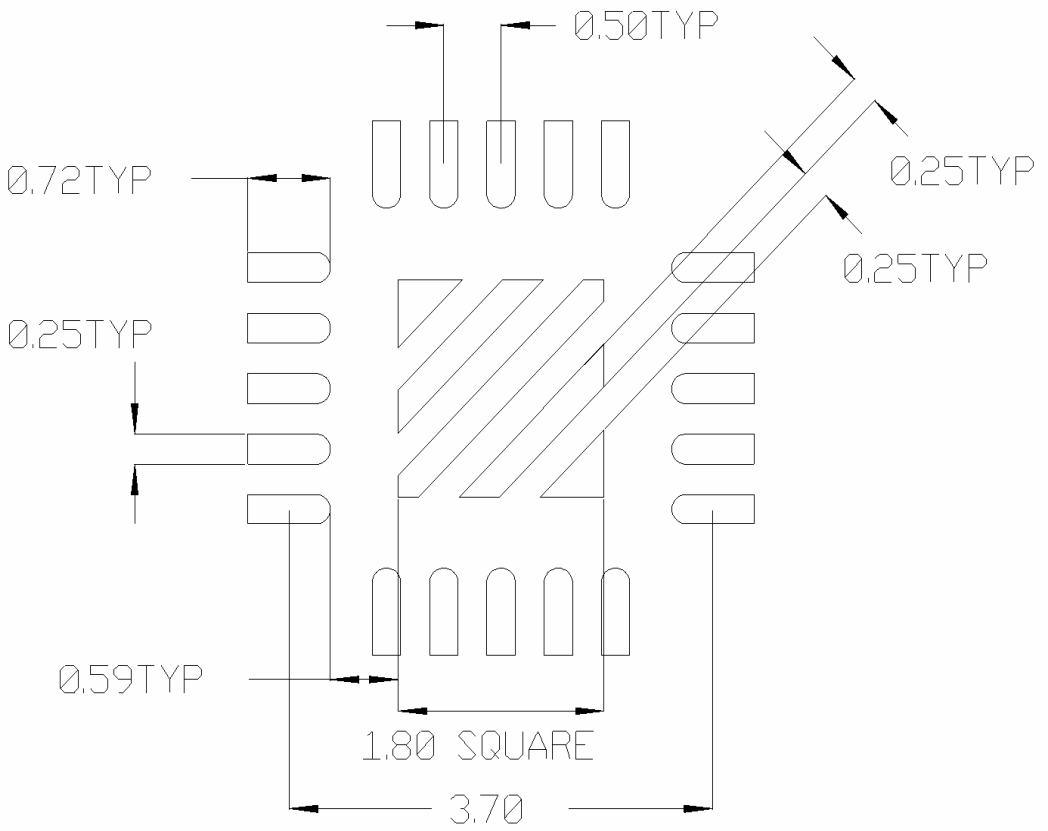
Solder Resist

- The solder resist should be pulled away from the metal lead lands and center pad by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore, pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm. At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The 4 vias in the land pad should be tented with solder resist 0.4mm diameter, or 0.1mm larger than the diameter of the via.



Stencil Design

- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

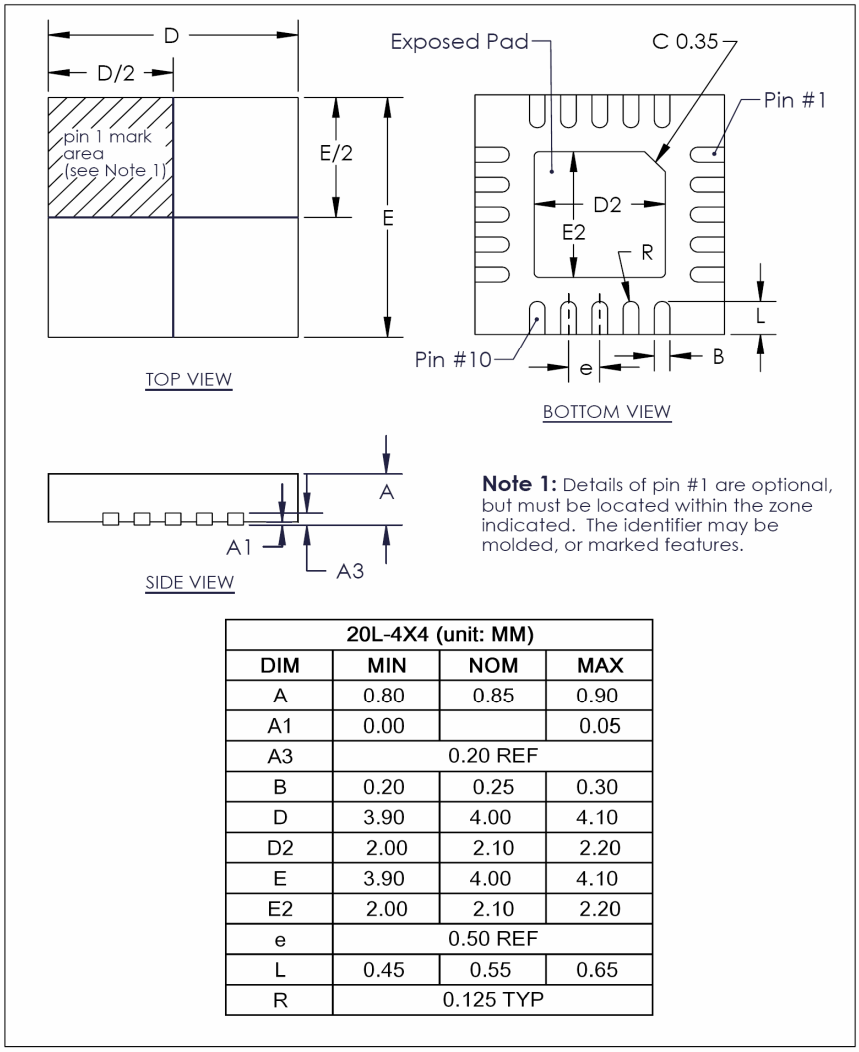


Stencil Aperture

All Dimensions in mm

PACKAGE INFORMATION

20L MLPQ (4 x 4 mm Body) – θ_{JA} = 32°C/W, θ_{JC} = 3°C/W



20L-4X4 (unit: MM)			
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3		0.20 REF	
B	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.00	2.10	2.20
E	3.90	4.00	4.10
E2	2.00	2.10	2.20
e		0.50 REF	
L	0.45	0.55	0.65
R		0.125 TYP	

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