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5D1 H264 Encoder with 4-Channel A/V Decoder & 12 Channels External VD Inputs for Security Applications

TW5864B1

TW5864 is a H.264 encoder solution with integrated 4-channel analog A/V decoders. TW5864 can be used as a low cost single chip solution for 4-channel H.264 hardware compression PC cards, or 16-channel cards by using additional external TW2866 chips. There are 3 versions of TW5864 that can support no external video decoder (TW5864A), 4 channel external video decoders (TW5864B), and 12 channel external video decoders (TW5864C). TW5864 can also be used in embedded DVR applications as an AV front-end chip with H264 encoding capability. It can work with existing H.264 hardcore or DSP based CODECs. In existing H264 CODECs, performance may be limited due to limitation in both memory bandwidth and hardware resources. With the H.264 encoder built in at the front-end, the number of encoding channel supported scales with number of TW5864 chips used. The front-end H264 encoder offloads the processing from the backend CODECs to allow higher port count support and allows DSP resources saved and reserved for product differentiation features such as video analytic intelligence.

TW5864 features H.264 baseline level 3 compliant encoder capable of performing up to 5 D1 equivalent video encoding (125 fps for PAL and 150 fps for NTSC), 17 channel G.726 ADPCM hardware audio encoder with one channel for two way audio communication. The H.264 video encoder supports dual-bitstream compression for both local storage and network port outputs. It also features a motion JPEG encoder for up to 25 frames per second shared among all video channels.

TW5864 integrates 4 A/V decoders. It has 4 CVBS analog inputs fed into four internal high quality NTSC/PAL video decoders. In addition, it has 3 digital BT. 656 input, running up to 108 MHz, capable of receiving up to 12 D1 video channels from external multi-channel video decoders such as TW2866 / TW2867. This allows the TW5864 to support a total of 16 video input channels. The video streams from both on-chip/off-chip video decoders are fed into H.264 encoder as well as to external interfaces for preview purpose. The preview stream can go through either though four BT. 656 video output interfaces or PCI interfaces. The four BT 656 ports support both multi-channel byte or line interleaved output to interface with various external display solutions.

TW5864 has built-in de-interlacers and OSDs before encoding is performed. There are also 16 sets of motion detection / night detection / blind detection engine for channel alarm notification. In addition, the hardware encoder generated motion information of each channel is accessible to the external CPU for analytic purpose. TW5864 also integrates many sets of scalers for each of the H264 encoder, MJPEG, and preview paths. Each of these scalers is independently configured.

TW5864 provides both asynchronous host interface and PCI interface for external CPU control and bitstream upload. The PCI interface can run at 33 or 66 MHz.

Analog Video Decoder

- 4 CVBS analog inputs fed into 4 sets of video decoder accept all NTSC(M/N/4.43) / PAL (B/D/G/H/I/K/L/M/N/60) standards with auto detection
- Integrated video analog anti-aliasing filters and 10 bit CMOS ADCs for each video decoder
- High performance adaptive 4H comb filters for all NTSC/PAL standards
- IF compensation filter for improvement of color demodulation
- Color Transient Improvement (CTI)
- Automatic white peak control
- Programmable hue, saturation, contrast, brightness and sharpness
- Proprietary fast video locking system for non-real-time application
- Noise Reduction to remove impulse noise

Digital Input Ports

- Three BT. 656 ports, each running at 108 MHz, directly interfaced with 3 external TW2866s
- Byte-interleaving supports 4 channels each port
  - Interlaced D1 interface at 60 / 50 fields per second
  - Progressive D1 interface at 30 / 25 frames per second
- Pre-processing
- Per channel triple high performance downscalers of each channel scales independently for H264, JPEG and preview output
- Per channel motion detector with 16 X 12 cells
  - Single Box
  - 1-bit per pixel text
  - 12-bit per pixel bitmap
- Digital Output Ports
- Preview video for external display chips
- Four BT. 656 ports for preview raw video output
- Byte-Interleaving interlaced D1 for all ports at 27 or 108 MHz
- Line-interleaving for the first 2 ports capable of supporting mix of interlaced D1 and CIF format at 27, 54, 81, or 108 MHz

H.264 Video Encoder

- H.264 baseline profile @ level 3 encoding
- Bit rate from 64 kbps up to 10 mbps each channel
- Maximum 125 fps (PAL) or 150 fps (NTSC)
- Real-time 4 D1 / 16 CIF or non-real-time 16 D1 main stream encoding
- Real-time 4 CIF / 16 QCIF or non-real-time 16 CIF secondary stream encoding
- VBR / CBR controllable
- Configurable GOP interval

Digital Audio CODEC

- Hardware G.726 ADPCM encoder
- Encodes maximum of 17 channels, with 1 channel for two way communication
- Decodes 1 channel of audio for playback
- RTC for AV sync

DDR Interface

- Two 16-bit external DDR SDRAM memories
- Running at 166 MHz
- Total 256 MB up to 1 GB
- Auto refresh

Host Interface

- Configurable 32-bit asynchronous host interface / PCI interface
- PCI Interface runs as both initiator and target at 33 / 66 MHz
- Per channel night / blind detections
- Per channel de-interlacer to convert Interlaced video into progressive before compression
- Per channel OSD for information overlay
- Motion vector granularity at full pel, ½ pel, and ¼ pel
- Motion vector ranges [-256, +255.75]
- In-loop de-blocking filter
- CAVLC entropy coding

Video Analytic Interface

- Per MB type / motion information
- 16x12 cells motion detection information
- Accessible through PCI / Async Host Interface

Motion JPEG Encoder

- Maximum of 25 fps, shared among all channels
- Support picture sizes of D1, CIF, and half-D1

Analog Audio CODEC

- Integrated five audio ADCs and one audio DAC providing multi-channel audio mixed analog output
- Supports a standard I2S interface for record output and playback input
- PCM 8/16 bit and u-Law/A-Law 8bit for audio word length
- Programmable audio sample rate that covers popular frequencies of 8/16/32/44.1/48kHz
- Video through PCI supporting various preview resolution such as
  - 2 D1
  - 1 D1 + 4 CIF
  - 9 CIF
  - 16 QCIF
  - 1 D1 + 15 QCIF
- I2C Interface for external Video Decoder chips configuration
- IRQs and GPIOs

System Clock

- Single 27 MHz external crystal clock input
- 3 built-in PLLs for internal clock generation

Package

- 352 BGA