MN101EF63G

8-bit Single-chip Microcontroller

■ Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for in-vehicle body control, in-vehicle AV, camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. MN101EF63 series has an internal 128 KB of ROM and 10 KB of RAM. Peripheral functions include 5 external interrupts, 34 internal interrupts including NMI, 12 timer counters, 4 types of serial interfaces, CAN controller based on CAN 2.0B, A/D converter, LCD driver, 2 types of watchdog timer, and data automatic function. The system configuration is suitable for in-vehicle body control microcontroller such as in-vehicle body control, heater control, relay BOX, or various motor controls.

With 5 oscillation systems (high-speed (internal frequency: 20 MHz), high-speed (crystal/ceramic frequency: max. 10 MHz) / low-speed (internal frequency: 30 kHz), low-speed (crystal/ceramic frequency: 32.768 kHz) and PLL: frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode), PLL input (PLL mode), or to low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has the normal mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in the normal mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode and in the double speed mode when the internal oscillation frc is 20 MHz (PLL is not used) is 50 ns (maximum).The package is 64-pin, TQFP.

■ Product Summary

This datasheet describes the following model.

Model	ROM Size	RAM Size	Classification	Package
MN101EF63G	128 KB	10 KB	Flash EEPROM version	TQFP064-P-1010C TQFP064-P-1010D

■ Features

- ROM capacity: 128 KB
- RAM capacity: 10 KB
- Package:
  TQFP064-P-1010C/TQFP064-P-1010D (10 mm × 10 mm / 0.5 mm pitch)
- Machine Cycle:
  High-speed mode
  0.05 μs / 20 MHz (2.7 V to 5.5 V)
  0.125 μs / 8 MHz (1.8 V to 5.5 V)
  Low-speed mode
  62.5 μs / 32 kHz (1.8 V to 5.5 V)
- Clock Gear Circuit:
  Internal system clock speed is changeable by selecting division ratio of oscillation clock. (Divided by 1, 2, 4, 16, 32, 64, 128)
- Oscillation Circuit: 4 types
  High-speed (Internal oscillation: frc), High-speed (crystal/ceramic: fosc),
  Low-speed (Internal oscillation: frcs), Low-speed (crystal/ceramic: fx)
  High-speed internal oscillation 20 MHz / 16 MHz (selectable)
  Low-speed internal oscillation 30 kHz
- Clock Multiplication Circuit:
  PLL circuit output clock (fpll) fosc multiplied by 2, 3, 4, 5, 6, 8, 10, 1/2 × frc multiplied by 4, 5 enabled
  * When clock multiplication circuit is not used, fpll = fosc or fpll = frc
  * Selectable from high-speed clock for peripheral functions (fpll-div) fpll, fpll divided by 2, 4, 8, 16
- Operation Mode
  NORMAL mode (high-speed mode)
  PLL mode
  SLOW mode (low-speed mode)
  HALT mode
  STOP mode
  and operation clock switching
- Operating Voltage:
  1.8 V to 5.5 V
- Operation ambient temperature:
  –40°C to +85°C (Product guaranteed 105°C is available)

■ Features (continued)

- Interrupt: 35 sets

<Overrun interrupt>
Non-maskable interrupt (NMI)

<Timer interrupt>
Timer 0 interrupt
Timer 1 interrupt
Timer 2 interrupt
Timer 3 interrupt
Timer 4 interrupt
Timer 6 interrupt
Time-base interrupt
Timer 7 interrupt
Timer 7 compare register 2 match interrupt
Timer 8 interrupt
Timer 8 compare register 2 match interrupt
PWM overflow interrupt
PWM under flow interrupt
Timer 9 compare register 2 match interrupt
24H timer interrupt
Alarm match interrupt

<Serial interrupt>
CAN interrupt
Serial 0 interrupt
Serial 0 UART reception interrupt
Serial 1 interrupt
Serial 1 UART reception interrupt
Serial 2 interrupt
Serial 2 UART reception interrupt
Serial 4 interrupt
Serial 4 stop condition interrupt

<A/D interrupt>
A/D conversion interrupt

<Data automatic transfer interrupt>
ATC1 interrupt

<Low voltage detection interrupt>
Low voltage detection interrupt

<External interrupt>
IRQ0 : Edge selection, noise filter connectable
IRQ1 : Edge selection, noise filter connectable
IRQ2 : Edge selection, noise filter connectable, both edge interrupt
IRQ3 : Edge selection, noise filter connectable, both edge interrupt
IRQ4 : Edge selection, noise filter connectable, both edge interrupt, key scan interrupt

■ Features (continued)

- Timer Counter × 12 sets

General-purpose 8-bit timer × 5 sets
General-purpose 16-bit timer × 2 sets
Motor control 16-bit timer × 1 set
8-bit free-run timer × 1 set
Time-base timer × 1 set
Baud rate timer × 1 set
24H timer × 1 set

Timer 0 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2bit) type PWM output can be output to large current pin TM0IOB, event count, simple pulse width measurement
Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output
Real-time control: Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

Timer 1 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), event count
16-bit cascade connection (connected with timer 0), timer synchronous output
Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 2 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2bit) type PWM output can be output to large current pin TM2IOB, event count, simple pulse width measurement,
24-bit cascade connection (connected with timer 0, 1), timer synchronous output
Double-buffered compare register (×1)
Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output
Real-time control: Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

Timer 3 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), event count
16-bit cascade connection (connected with timer 2), 32-bit cascade connection (connected with timer 0, 1, 2)
Double-buffered compare register (×1)
Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 4 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2bit) type PWM output, event count, simple pulse width measurement
Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 6 (8-bit free-run timer, time-base timer)
8-bit free-run timer
Clock source: fpll-div, fpll-div/2^2, fpll-div/2^3, fpll-div/2^{12}, fpll-div/2^{13}, fs, fslow, fslow/2^2, fslow/2^3, fslow/2^{12}, fslow/2^{13}
Time-base timer
Interrupt generation cycle: fpll-div/2^7, fpll-div/2^8, fpll-div/2^9, fpll-div/2^{10}, fpll-div/2^{13}, fpll-div/2^{15},fslow/2^7,fslow/2^8, fslow/2^9, fslow/2^{10}, fslow/2^{13}, fslow/2^{15}

■ Features (continued)

- Timer Counter (continued)

Timer 7 (General-purpose 16-bit timer)

Clock source:	fpll-div, fs, external clock, timer A output, serial 0 transfer clock output, timer 6 compare match cycle divided by 1, 2, 4, 16
Hardware configuration:	Double-buffered compare register (×2) Double-buffered input capture register (×2) Timer interrupt (×2 vector)
Timer function:	Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable) can be output to large current pin TM7IOB, timer synchronous output, event count, input capture function (both edges operable)
Real-time control:	Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

Timer 8 (General-purpose 16-bit timer)

Clock source:	fpll-div, fs, external clock, timer A output, timer 6 compare match cycle divided by 1, 2, 4, 16
Hardware configuration:	Double-buffered compare register (×2) Double-buffered input capture register (×1) Timer interrupt (×2 vector)
Timer function:	Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable) can be output to large current pin TM8IOB, event count, pulse width measurement, input capture function (both edges operable) 32-bit cascade connection (connected with timer 7), 32-bit PWM output, Input capture is available in 32-bit cascade

Timer 9 (Motor control 16-bit timer)

Clock source:	fpll-div, fs, external clock, Timer A output divided by 1, 2, 4, 16
Hardware configuration:	Double-buffered compare register (×2) Timer interrupt (×3 vector)
Timer function:	Square wave output (Timer pulse output), switchable to large current output, complementary 3-phase PWM output, Triangle wave and saw tooth wave are supported, dead time insertion available, event count
Pin output control:	PWM output control is possible by external interrupt 0 to 4 (IRQ 0 to 4) ("Hi-z", output data fixed)

Timer A (baud rate timer)

Clock output for peripheral functions

Clock source:	fpll-div divided by 1/1, 2, 4, 8, 16, 32, and fs divided by 2, 4

24H timer

Clock source (Usable frequency):	fpll (4 MHz, 4.19 MHz, 5 MHz, 8 MHz, 8.38 MHz, 10 MHz, 16 MHz, 16,77 MHz, 20 MHz) fx (32.768 kHz), frc (20 MHz, 16 MHz), frcs (30 kHz)
Hardware configuration:	0.5 seconds counter, minute counter, hour counter Alarm compare register (in 0.5 seconds, in minutes, in hours) (×1) Timer interrupt (×2 vector)
Timer function:	Interval function (interrupts every 0.5 seconds, 1 second, 1 minute, 1 hour, 24 hours) Alarm function

- Watchdog timer

Overrun detection cycle is selectable from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$

Forced to reset inside LSI by hardware when a software processing error is detected twice

■ Features (continued)

- Watchdog timer2

  Overrun detection cycle is selectable from frcs/2^4, frcs/2^5, frcs/2^6, frcs/2^7, frcs/2^8, frcs/2^9, frcs/2^{10}, frcs/2^{11}, frcs/2^{12}, frcs/2^{13}, frcs/2^{14}, frcs/2^{15}

  Forced to reset inside LSI by hardware when a software processing error is detected twice

- Synchronous output function (Timer synchronous output, interrupt synchronous output)

  Latch data is output from port 8 at the event timing of synchronous output signal of timer 1, timer 2, timer 7, or external interrupt2 (IRQ2)

- A/D converter

  10 bit × 12 channels

- Data automatic transfer 1 system

  ATC1

  Data is automatically transferred in all memory space

  External interrupt activation/internal event activation/software activation

  Max. 255 byte continuous transfer

  Serial continuous transmission and reception is supported

  Burst transfer function (Including interrupt emergency stop)

- CAN Controller

  Channels: 1 channel

  CAN 2.0B specification basis

  Communication method: NRZ (Non-Return to Zero)

  Transmission line: Bidirectional 2-wire serial communication

  Communication speed: Max. 1 Mbps

  Data length: 0 to 8 byte

  Message frame: Standard frame and extended frame are supported

  Standard frame format ID: 11 bits

  Extended frame format ID: 29 bits

  Buffer size: 32 messages (32 x 132 bit)

  Interrupt 1 set

  Interrupt source

  Transition from bus off state to error active state, or back transition

  Transition from warning error condition (error counter indicates 96 or more) to warning error condition released (error counter indicates less than 96) or back transition

  Transmission completion

  Transmission/reception error (Ack/Form/Stuff/Bit1/Bit0/CRC errors)

- Serial Interface: 4 systems

  Serial 0 (Full duplex UART / Synchronous serial interface)

  Synchronous serial interface

  Transfer clock source: fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock

  MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer

  Continuous transmission, continuous reception, continuous transmission and reception are available.

  Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)

  Parity check, overrun error/framing error are detected

  Transfer bits 7 to 8 are selectable

■ Features (continued)

- Serial Interface:(continued)

Serial 1 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

Transfer clock source: fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock

MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer

Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)

Parity check, overrun error/framing error are detected

Transfer bits 7 to 8 are selectable

Serial 2 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

Transfer clock source: fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock

MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer

Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)

Parity check, overrun error/framing error are detected

Transfer bits 7 to 8 are selectable

Serial 4 (Multi master IIC / Synchronous serial interface)

Synchronous serial interface

Transfer clock source: fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/32, fs/2, fs/4,
Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock

MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer

Continuous transmission, continuous reception, continuous transmission and reception are available.

Multi master IIC

7, 10-bit slave address is settable

General call communication mode is supported

- Auto reset circuit
- Low voltage detection circuit
- Clock monitoring function
- LED driver: 6 sets

■ Features (continued)

- LCD driver

LCD driver pins

Segment output: Max. 32 pins (SEG0-31)

SEG0-31 can be switched to I/O port in pins.

(Note) At reset, SEG0-31 are input ports.

Common output pins: 4 pins

COM0-3 can be switched to I/O port in pins.

Display mode selection

Static

1/2 duty, 1/2 bias

1/3 duty, 1/3 bias

1/4 duty, 1/3 bias

LCD driver clock

When source clock is main clock (fpll)

$1/2^{18}$,$1/2^{17}$,$1/2^{16}$,$1/2^{15}$,$1/2^{14}$,$1/2^{13}$,$1/2^{12}$,$1/2^{11}$

When source clock is sub clock (fslow)

$1/2^{9}$,$1/2^{8}$,$1/2^{7}$,$1/2^{6}$

Timer 0 to 4, Timer A output

LCD power

LCD power is separated from V_{DD5} (can be used when $V_{LC1} \leq V_{DD5}$)

Supply voltage can be selected externally.

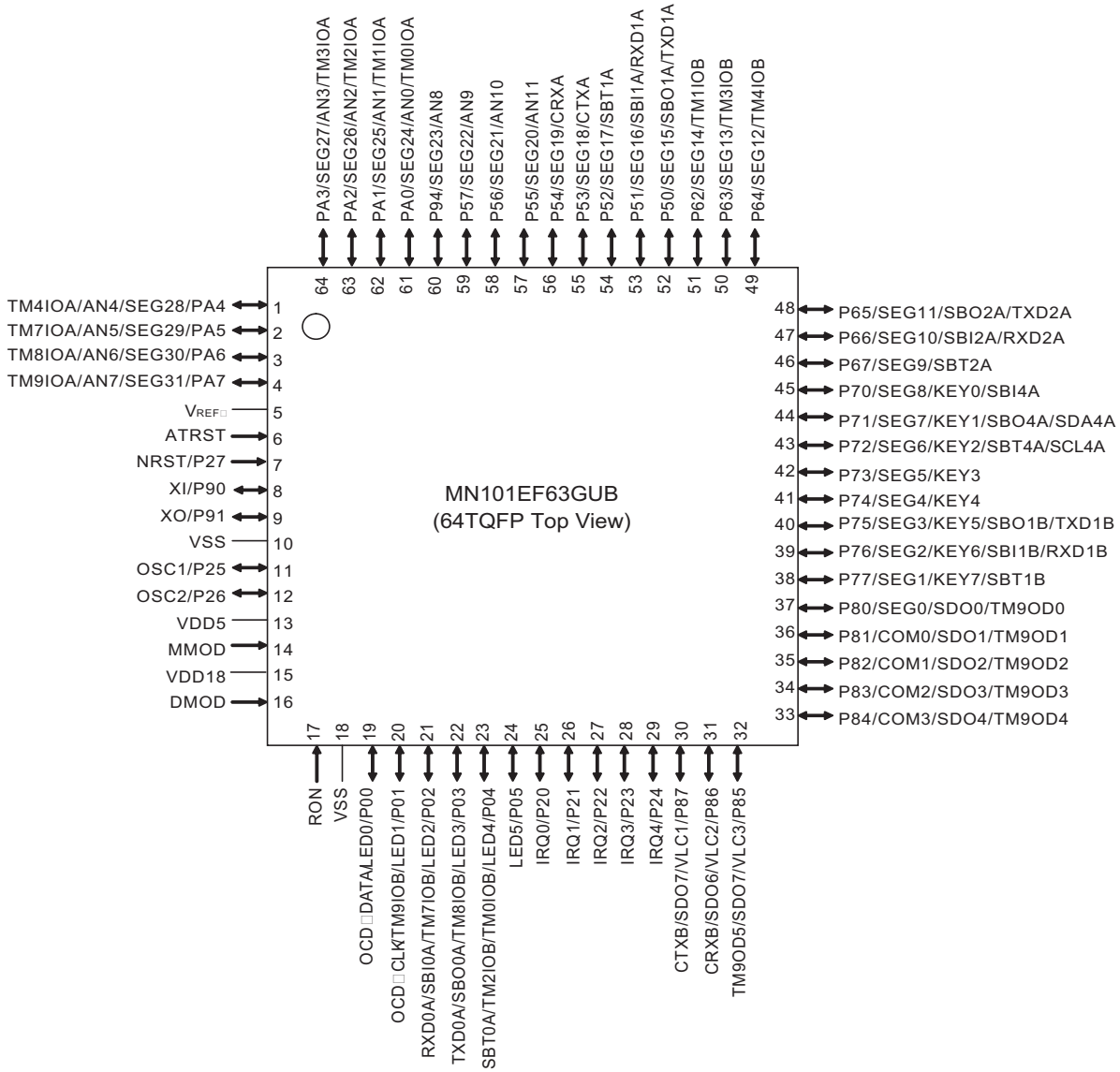
(External supply voltage is supplied from VLC1, VLC2, and VLC3 pins, or can be used by dividing the voltage added to VLC1 pin by internal resistor.)

- Ports

I/O ports	54 pins
LCD segment	32 pins
LCD common	4 pins
CAN	4 pins
Serial	15 pins
Timer I/O	21 pins
A/D input	12 pins
External interrupt	5 pins
LCD power	3 pins
LED (large current) driver	6 pins
High-speed oscillation	2 pins
Low-speed oscillation	2 pins
Special pins	10 pins
Operating mode input pins	3 pins
Reset input pins	1 pin
Analog reference voltage input pin	1 pin
Power pins	4 pins

■ Pin Description

- TQFP064-P-1010C / TQFP064-P-1010D



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