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# LB1945D

Monolithic Digital IC

## PWM Current Control Stepping Motor Driver

### Overview

The LB1945D is a PWM current control stepping motor driver that uses a bipolar drive technique. It is optimal for use with the carriage and paper feed stepping motors used in printers.

### Functions and Features

- PWM current control (external clock)
- Digital load current selection function (supports 1-2, W1-2, and 2-phase excitation)
- Built-in high and low side diodes
- Simultaneous on state prevention function (through-current prevention)
- Built-in thermal shutdown circuit
- Noise canceling function

### Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	$V_{BB}$ max		30	V
Output peak current	$I_O$ peak	$tW \leq 20\mu\text{s}$	1.0	A
Output continuous current	$I_O$ max		0.8	A
Logic system supply voltage	$V_{CC}$ max		6.0	V
Logic input voltage range	$V_{IN}$		-0.3 to $V_{CC}$	V
Emitter output voltage range	$V_E$		1.0	V
Allowable power dissipation	$P_d$ max	Independent IC	2.8	W
Operating temperature	$T_{opr}$		-20 to +90	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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## Recommended Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	V <sub>BB</sub>		10 to 28	V
Logic system supply voltage	V <sub>CC</sub>		4.75 to 5.25	V
Reference voltage	V <sub>REF</sub>		1.5 to 5.0	V

## Electrical Characteristics at Ta = 25°C, V<sub>BB</sub> = 24V, V<sub>CC</sub> = 5V, V<sub>REF</sub> = 5V

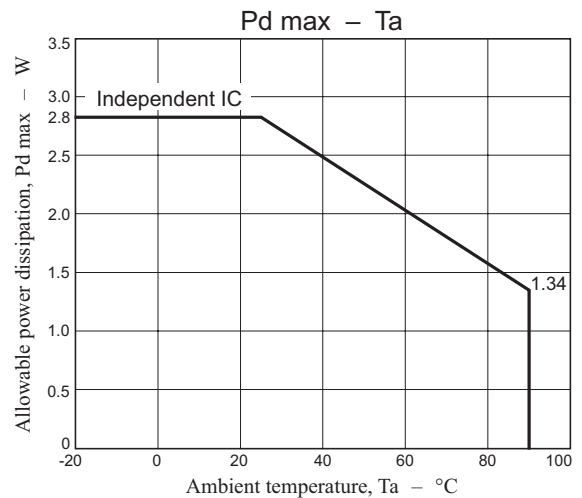
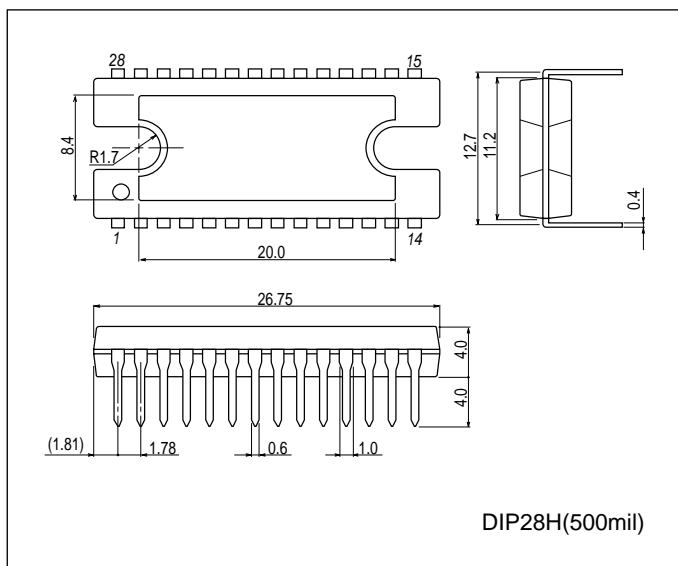
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>Output block</b>						
Output stage supply current	I <sub>BB ON</sub> I <sub>BB OFF</sub>	I <sub>1</sub> = 0.8V, I <sub>2</sub> = 0.8V, ENABLE = 0.8V ENABLE = 3.2V	0.5	1.0	2.0 0.2	mA
Output saturation voltage 1	V <sub>O sat1</sub>	I <sub>O</sub> = +0.5A, sink side		0.3	0.5	V
Output saturation voltage 2	V <sub>O sat2</sub>	I <sub>O</sub> = +0.8A, sink side		0.5	0.7	V
Output saturation voltage 3	V <sub>O sat3</sub>	I <sub>O</sub> = -0.5A, source side		1.6	1.8	V
Output saturation voltage 4	V <sub>O sat4</sub>	I <sub>O</sub> = -0.8A, source side		1.8	2.0	V
Output leakage current	V <sub>O1(leak)</sub> V <sub>O2(leak)</sub>	V <sub>O</sub> = V <sub>BB</sub> , sink side V <sub>O</sub> = 0V, source side	-50		50	μA
Output sustain voltage	VSUS	L = 3.9mH, I <sub>O</sub> = 1.0A*	30			V
<b>Logic block</b>						
Logic supply current	I <sub>CC ON</sub> I <sub>CC OFF</sub>	I <sub>1</sub> = 0.8V, I <sub>2</sub> = 0.8V, ENABLE = 0.8V ENABLE = 3.2V	50 7	70.0 10.0	92 13	mA
Input voltage	V <sub>IH</sub> V <sub>IL</sub>		3.2		1.8	V
Input current	I <sub>IH</sub> I <sub>IL</sub>	V <sub>IH</sub> = 3.2V V <sub>IL</sub> = 0.8V	35 7	50 10	65 13	μA
Set current control threshold value	V <sub>REF</sub> / V <sub>SEN</sub>	I <sub>1</sub> = 0.8V, I <sub>2</sub> = 0.8V I <sub>1</sub> = 3.2V, I <sub>2</sub> = 0.8V I <sub>1</sub> = 0.8V, I <sub>2</sub> = 3.2V	9.5 13.5 25.5	10 15 30	10.5 16.5 34.5	
Reference current	I <sub>REF</sub>	V <sub>REF</sub> = 5.0V, I <sub>1</sub> = 0.8V, I <sub>2</sub> = 0.8V	17.5	25	32.5	μA
CR pin current	I <sub>CR</sub>	CR = 1.0V	-1.0			μA
Thermal shutdown temperature	TS			170		°C
Thermal shutdown hysteresis	TSHY			40		°C

\*: The design specification items are design guarantees and are not measured.

## Package Dimensions

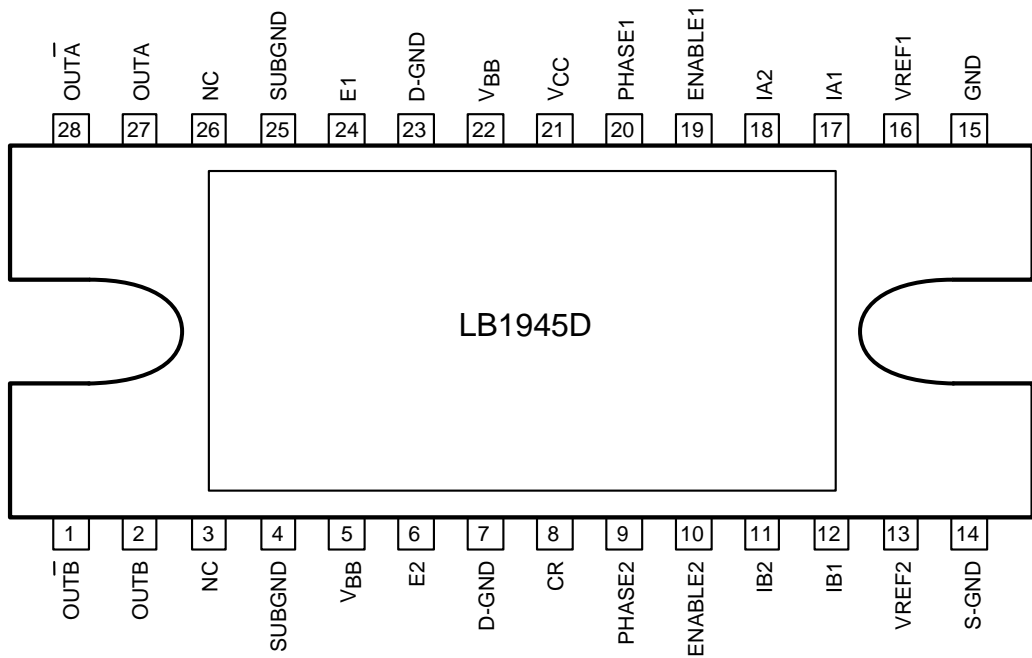
unit:mm (typ)

3147C



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## Pin Assignment



Top view

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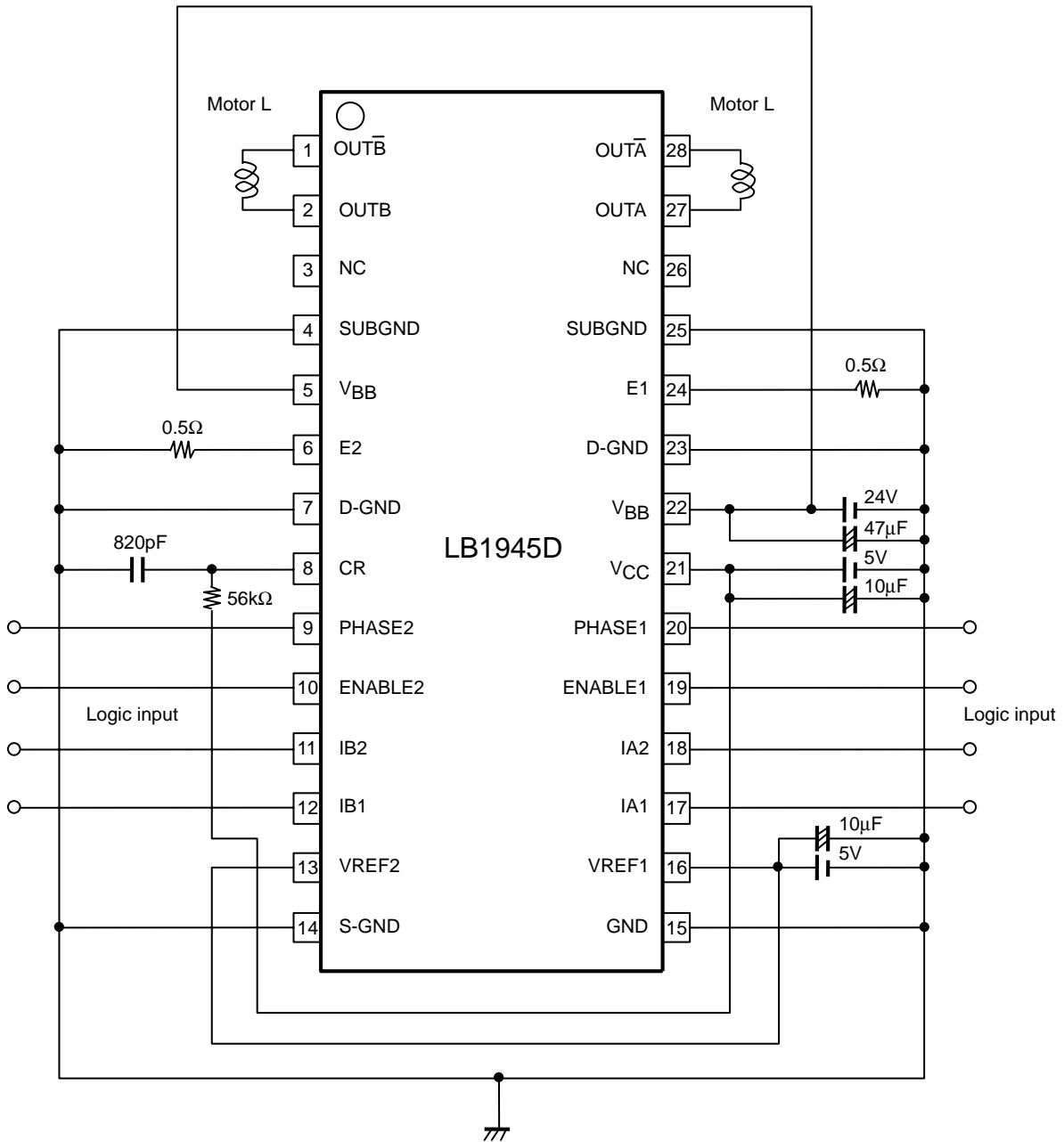
## Pin Functions

Pin No.	Pin	Description
22	V <sub>BB1</sub>	Output stage power supply voltage
5	V <sub>BB2</sub>	High side diode cathode connection
24	E1	The set current is controlled by inserting resistors R <sub>E</sub> between these pins and ground.
6	E2	
27	OUTA	Output pins
28	OUTA <sup>̄</sup>	
2	OUTB	
1	OUTB <sup>̄</sup>	
15	GND	Ground
14	S-GND	Sense ground
4, 25	SUBGND	IC sub-ground
23	D-GND	Low side built-in diode ground (anode side)
7		
8	CR	Chopping is performed at the period of a triangle wave set by the RC circuit connected to this pin. The triangle wave off time is the noise cancellation time.
16	VREF1	Output current settings. (The output current is determined by providing an input in the range 1.5V to 5V.)
13	VREF2	
20	PHASE1	Output phase switching inputs High-level input: OUTA = high, OUTA <sup>̄</sup> = low Low-level input: OUTA = low, OUTA <sup>̄</sup> = high
9	PHASE2	
19	ENABLE1	Output on/off control inputs High-level input: Output off Low-level input: Output on
10	ENABLE2	
17, 18	IA1, IA2	Output current setting digital inputs. The output current is set to 1/3, 2/3 or 1 by input high/low levels to these pins.
12, 11	IB1, IB2	
21	V <sub>CC</sub>	Logic block power supply voltage



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## Application circuit



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**Truth Table**

ENABLE	PHASE	OUTA	OUT $\bar{A}$
Low	High	High	Low
Low	Low	Low	High
High	-	OFF	OFF

I <sub>1</sub>	I <sub>2</sub>	Output current
Low	Low	$V_{ref}/(10 \times R_E) = I_{OUT}$
High	Low	$V_{ref}/(15 \times R_E) = I_{OUT} \times 2/3$
Low	High	$V_{ref}/(30 \times R_E) = I_{OUT} \times 1/3$
High	High	0

Note: The output is turned off when ENABLE is high or in the I<sub>1</sub> = I<sub>2</sub> = high state.

**Clockwise/counterclockwise Operating Sequence**  
2-phase excitation drive

Clockwise rotation

IA1 = IA2 = IB1 = IB2 = 0

No.	PHASE1	OUTA	OUT $\bar{A}$	PHASE2	OUTB	OUT $\bar{B}$
0	0	0	1	0	0	1
1	1	1	0	0	0	1
2	1	1	0	1	1	0
3	0	0	1	1	1	0

Counterclockwise rotation

IA1 = IA2 = IB1 = IB2 = 0

No.	PHASE1	OUTA	OUT $\bar{A}$	PHASE2	OUTB	OUT $\bar{B}$
0	0	0	1	1	1	0
1	1	1	0	1	1	0
2	1	1	0	0	0	1
3	0	0	1	0	0	1

**Control Sequence**  
2-phase excitation

Table 1

ENABLE1 = ENABLE2 = 0

NO	Phase A				Phase B			
	PH1	IA2	IA1	Current value	PH2	IB2	IB1	Current value
0	0	0	0	1	0	0	0	1
1	1	0	0	1	0	0	0	1
2	1	0	0	1	1	0	0	1
3	0	0	0	1	1	0	0	1

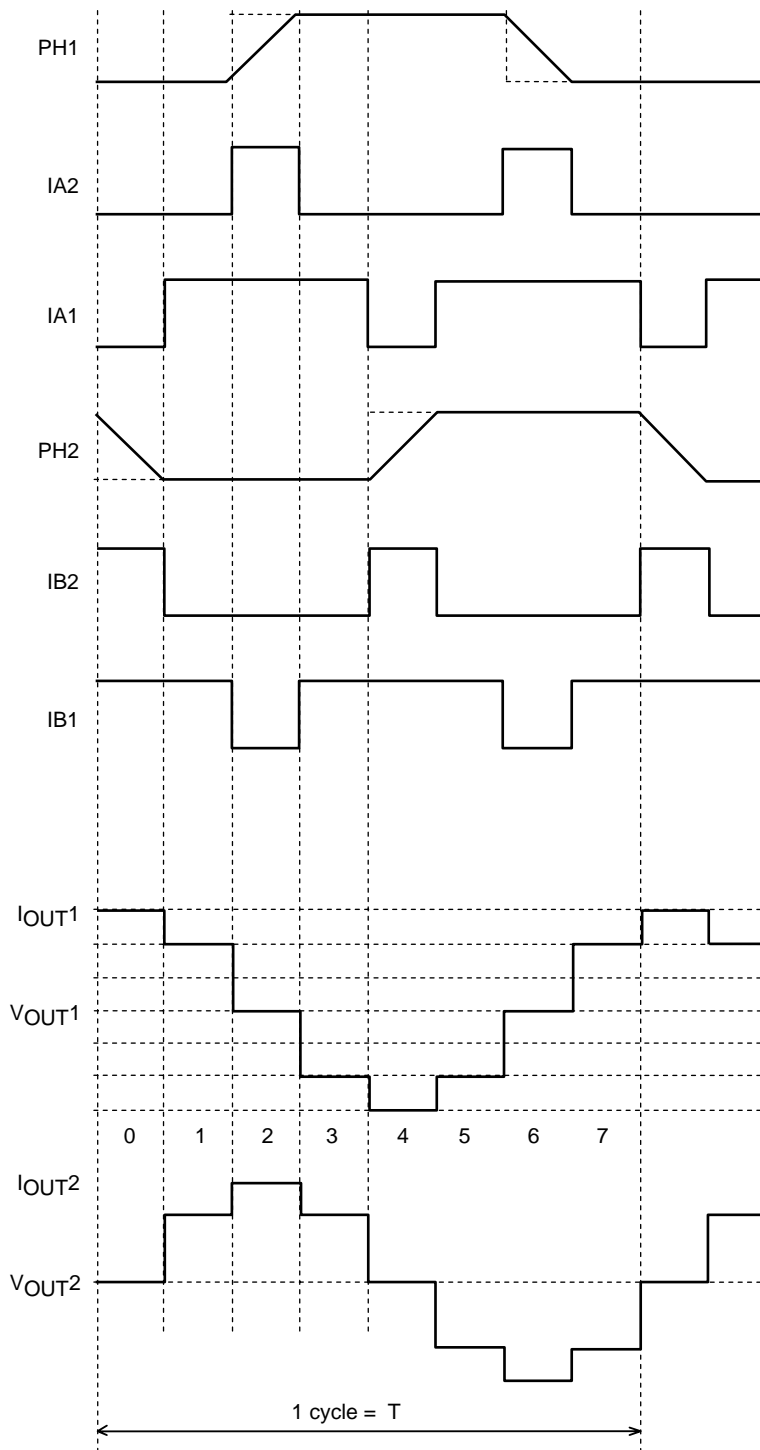
**1-2 phase excitation - 1/2 step**

Table 2

ENABLE1 = ENABLE2 = 0

No.	Phase A				Phase B			
	PH1	IA2	IA1	Current value	PH2	IB2	IB1	Current value
0	0	0	0	1	*	1	1	0
1	0	0	1	2/3	0	0	1	2/3
2	*	1	1	0	0	0	0	1
3	1	0	1	2/3	0	0	1	2/3
4	1	0	0	1	*	1	1	0
5	1	0	1	2/3	1	0	1	2/3
6	*	1	1	0	1	0	0	1
7	0	0	1	2/3	1	0	1	2/3

1-2 phase Excitation Timing Chart



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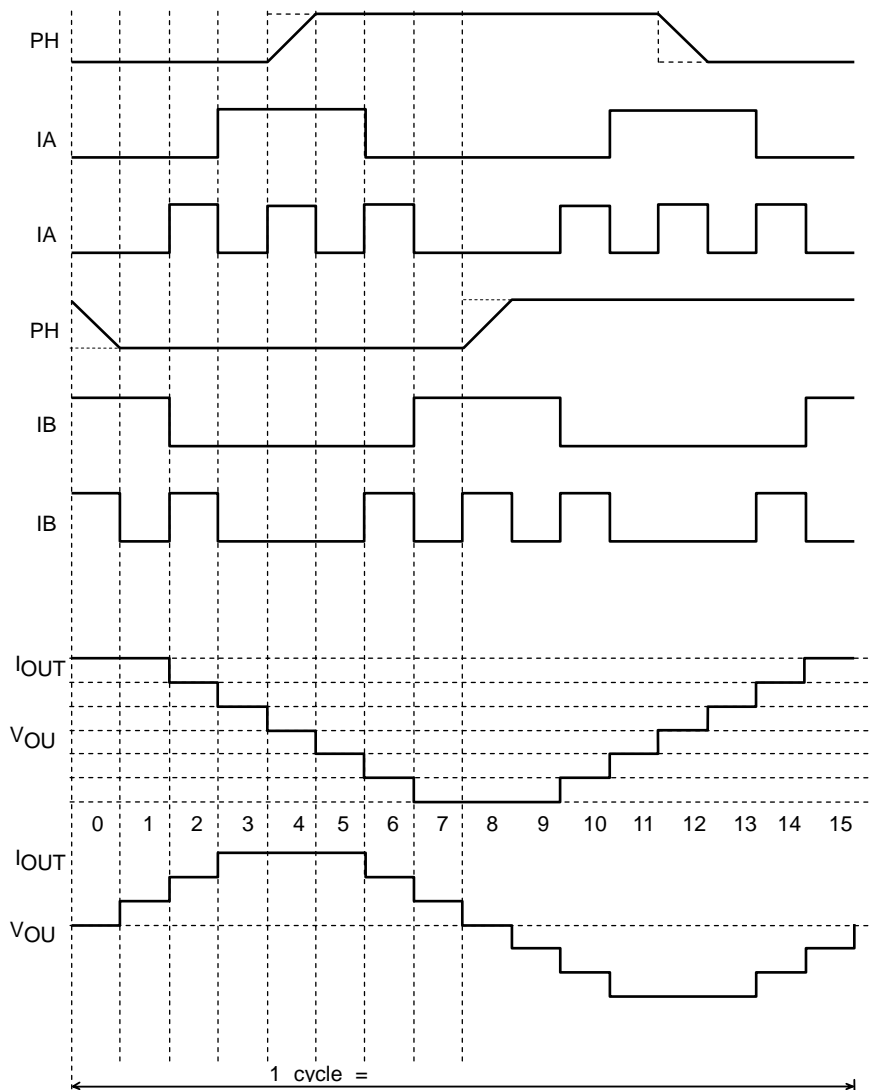
W1-2 phase excitation - about 1/4 step

Table 3

ENABLE1 = ENABLE2 = 0

NO	Phase A				Phase B			
	PH1	IA2	IA1	Current value	PH2	IB2	IB1	Current value
0	0	0	0	1	*	1	1	0
1	0	0	0	1	0	1	0	1/3
2	0	0	1	2/3	0	0	1	2/3
3	0	1	0	1/3	0	0	0	1
4	*	1	1	0	0	0	0	1
5	1	1	0	1/3	0	0	0	1
6	1	0	1	2/3	0	0	1	2/3
7	1	0	0	1	0	1	0	1/3
8	1	0	0	1	*	1	1	0
9	1	0	0	1	1	1	0	1/3
10	1	0	1	2/3	1	0	1	2/3
11	1	1	0	1/3	1	0	0	1
12	*	1	1	0	1	0	0	1
13	0	1	0	1/3	1	0	0	1
14	0	0	1	2/3	1	0	1	2/3
15	0	0	0	1	1	1	0	1/3

## W1-2 phase Excitation Timing Chart



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## Simplified Equations for Determining RC Component Values

The equations for setting the RC oscillator circuit rise time (T1) and fall time (T2) are shown below.

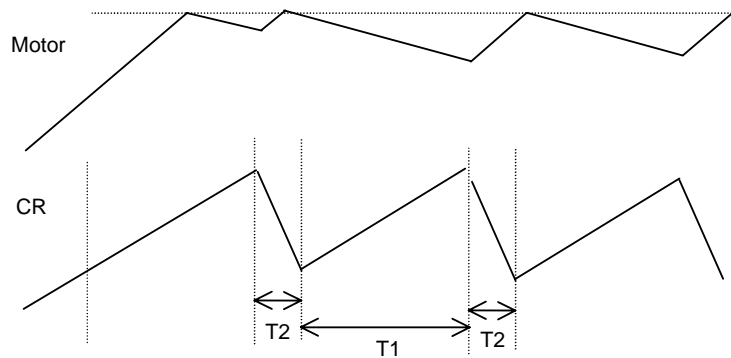
$$T1 \approx 0.44C \times R \text{ (s)}$$

$$T2 \approx 0.72 \times (C \times R \times 1000) / (R + 1000) \text{ (s)}$$

(C:220 to 4700pF, R = 10 to 150kΩ)

The oscillator frequency must be set using the simplified equations shown above.

Note that the triangle wave fall time (T2) is also used as the noise canceller time.



## Usage Notes

### 1. VREF

Since the VREF pin is the input pin for the reference voltage that sets the current, applications must be designed so that noise does not appear on this pin.

### 2. Ground pins

Since this IC switches high currents, the following points concerning grounding must be observed.

- The fins on the package rear surface, pins 7 and 8, and pins 21 and 22 must all be grounded.
- Sections of the circuit that carry large currents must be implemented with wide lines in the printed circuit pattern, and must be physically separated from the small signal system.
- The E pin sense resistor (RE) must be position as close as possible to the IC ground (pin 14).
- The capacitors between VCC and ground and between VBB and ground must be positioned as close as possible to the VCC and VBB pins on the printed circuit pattern.

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