PCA9618

Single channel Fm+ I²C-bus repeater

Rev. 1 — 13 January 2016 Product data sheet

1. General description

The PCA9618 is a CMOS integrated circuit that provides Fast-mode Plus (Fm+) I²C-bus or SMBus buffering of either the SCL or SDA line or can be used in any single bit applications that require buffering. While retaining all the operating modes and features of the I²C-bus system, it also permits extension of the I²C-bus by providing bidirectional buffering, thus enabling buses of 540 pF at 1 MHz or up to 4000 pF at lower speeds. Using the PCA9618 enables the system designer to isolate two halves of a bus for capacitance. The DATAA and DATAB pins are overvoltage tolerant and are high-impedance when the PCA9618 is unpowered.

The PCA9618 can be used to delay the SDA path by at least the minimum propagation delay, thereby providing an effective data hold time for applications that require an SDA hold time with respect to SCL. The PCA9618 includes an internal glitch filter, so that it will ignore glitches rather than expand them, this also means that the minimum propagation delay is on the order of 46 ns and is reasonably stable over temperature and supply voltage. Although this is not sufficient to provide the SDA delay requirement of the SMBus hold time specification of 300 ns, many parts that cannot be used with the 0 ns hold time of the I²C-bus specification only require a few ns of hold time to work correctly in a system. For these applications, the PCA9618 is an effective solution.

The PCA9618 can also be used as a buffer on a 1-wire bus similar to how the PCA9617A is used for the I²C-bus or to buffer the master (microcontroller's I/O) if the master's output is not strong enough to drive the 1-wire bus.

The 2.2 V to 5.5 V bus port B driver has the static level offset, while the port A driver eliminates the static offset voltage. This results in a LOW on the port B translating into a nearly 0 V LOW on the port A. This static offset voltage prevents the PCA9618 from latching into a steady state LOW when driven LOW.

The static offset design of the port B PCA9618 I/O driver prevents it from being connected to the static or incremented offset sides of other bus buffers. Port A of two or more PCA9618s can be connected together, also, to allow a star topography with port A on the common bus. Port A can be connected directly to any other buffer with static or incremented offset outputs. Multiple PCA9618s can be connected in series, port A to port B, with no build-up in offset voltage with only time of flight delays to consider.

The output pull-down on the port B internal buffer LOW is set for approximately 0.55 V, while the input threshold of the internal buffer is set about 90 mV lower (0.45 V). When the port B I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a latching condition from occurring. The output pull-down on port A drives a hard LOW and the input level is set at $0.35V_{CC}$.

2. Features and benefits

- 1 channel, bidirectional buffer isolates capacitance and allows 540 pF on either side of the device at 1 MHz and up to 4000 pF at lower speeds
- Operating supply voltage range of 2.2 V to 5.5 V
- Data pins are 5 V tolerant, allowing voltage translation applications
- 0 Hz to 1000 kHz clock frequency (the maximum system operating frequency may be less than 1000 kHz because of the delays added by the repeater)
- Open-drain input/outputs
- Latching free operation
- Accommodates Standard-mode, Fast-mode and Fast-mode Plus I²C-bus devices, SMBus (standard and high power mode), PMBus and multiple masters
- Powered-off high-impedance I²C-bus pins
- ESD protection exceeds 5500 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: WLCSP4

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9618UK	•8[1]	WLCSP4	wafer level chip-scale package; 4 bumps; body 0.78 × 0.83 × 0.53 mm	PCA9618UK

[1] Line A marking includes dot as pin 1 indication.

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9618UK	PCA9618UKZ	WLCSP4	Reel 13” Q1/T1 *Special mark chips dry pack	10000	T_{amb} = –40 °C to +85 °C

4. Functional diagram

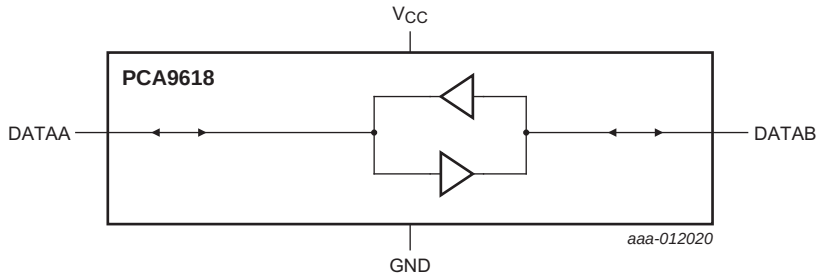


Fig 1. Functional diagram

5. Pinning information

5.1 Pinning

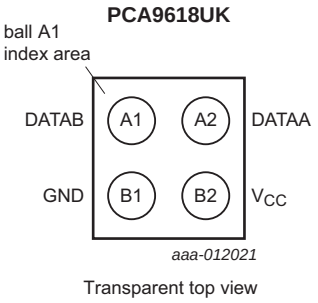


Fig 2. Pin configuration for WLCSP4

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
	WLCSP4	
DATAA	A2	data line, A port with normal voltage levels
n.c.	-	not connected
V_{CC}	B2	port B supply voltage (2.2 V to 5.5 V)
GND	B1	supply ground (0 V)
DATAB	A1	data line, B port with offset voltage levels

6. Functional description

Refer to Figure 1 “Functional diagram”.

All inputs and I/Os are overvoltage tolerant to 5.5 V even when the device is unpowered (V_{CC} = 0 V). The PCA9618 includes a power-up circuit that keeps the output drivers turned off until V_{CC} is above 2.2 V and until after the internal reference circuits have settled ~400 μs. A LOW level on port A (below $0.3V_{CC}$) turns on the port B driver and drives port B down to about 0.55 V. When port A rises above $0.3V_{CC}$, the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below 0.4 V, the port A driver is turned on and port A pulls down to ~0 V. The port A pull-down is not enabled unless the port B voltage goes below 0.4 V. If the port B low voltage goes below 0.4 V, the port B pull-down driver is enabled and port B will only be able to rise to 0.55 V until port A rises above $0.3V_{CC}$, then port B will continue to rise being pulled up by the external pull-up resistor. The V_{CC} supply is used to provide the $0.35V_{CC}$ reference to the port A input comparators and for the power good detect circuit.

6.1 I²C-bus systems

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode, Fast-mode and Fast-mode Plus I²C-bus devices in addition to SMBus devices. Standard mode and Fast-mode I²C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C-bus system where Standard-mode devices, Fast-mode devices and multiple masters are possible. When only Fast-mode Plus devices are used with 30 mA at 5 V drive strength, then lower value pull-up resistors can be used. The B-side RC should not be less than 67.5 ns because shorter RCs increase the turnaround bounce when the B-side transitions from being externally driven to pulled down by its offset buffer.

Please see Application Note *AN255, “I²C/SMBus Repeaters, Hubs and Expanders”* for additional information on sizing resistors and precautions when using more than one PCA9618 in a system or using the PCA9618 in conjunction with other bus buffers.

7. Application design-in information

A typical application is shown in Figure 3. In this example, the system master and slave are running on a 3.3 V I²C-bus. Both buses run at 1000 kHz. Master devices can be placed on either bus.

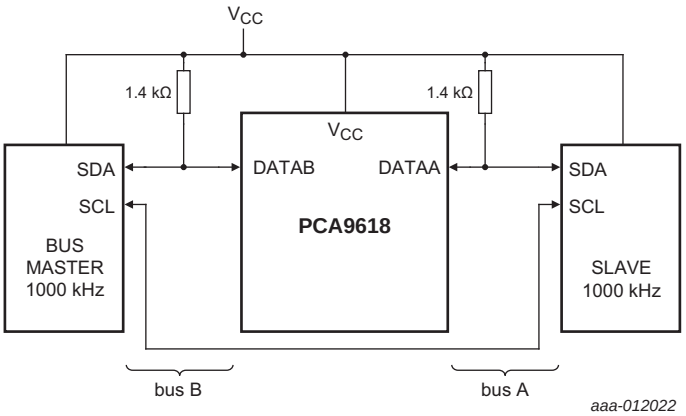


Fig 3. Typical application

When port A of the PCA9618 is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.3V_{CC}$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5 V. When port B of the PCA9618 falls, first comparator detects the falling edge when it goes below 0.4 V and causes the internal driver on port A to turn on and pull the port A pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 7 and Figure 8. If the bus master in Figure 3 were to write to the slave through the PCA9618, waveforms shown in Figure 7 would be observed on the A bus. This looks like a normal I²C-bus transmission except that the turn on and turn off of the acknowledge signals are slightly delayed.

On the B bus side of the PCA9618, the data line would have a positive offset from ground equal to the V_{OL} of the PCA9618. After the eighth clock pulse, the data line will be pulled to the V_{OL} of the slave device which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9618 for a short delay while the A bus side rises above $0.3V_{CC}$ then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the PCA9618 (V_{IL}) be at or below 0.4 V to be recognized by the PCA9618 and then transmitted to the A bus side.

Multiple PCA9618 port A sides can be connected in a star configuration (Figure 4), allowing all nodes to communicate with each other.

Multiple PCA9618s can be connected in series (Figure 5) as long as port A is connected to port B. I²C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

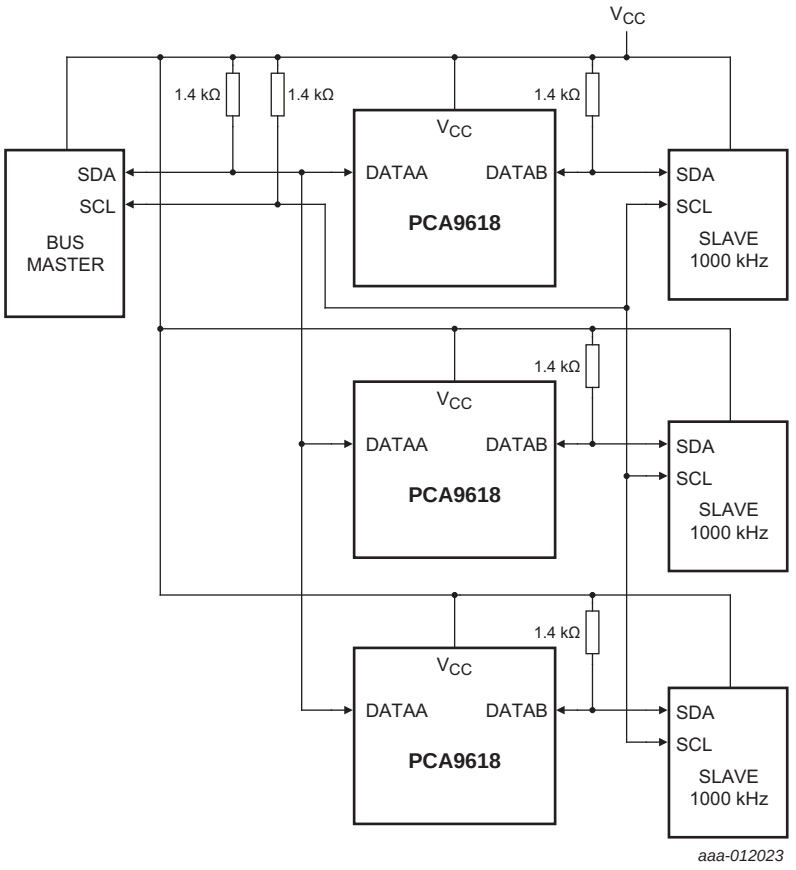
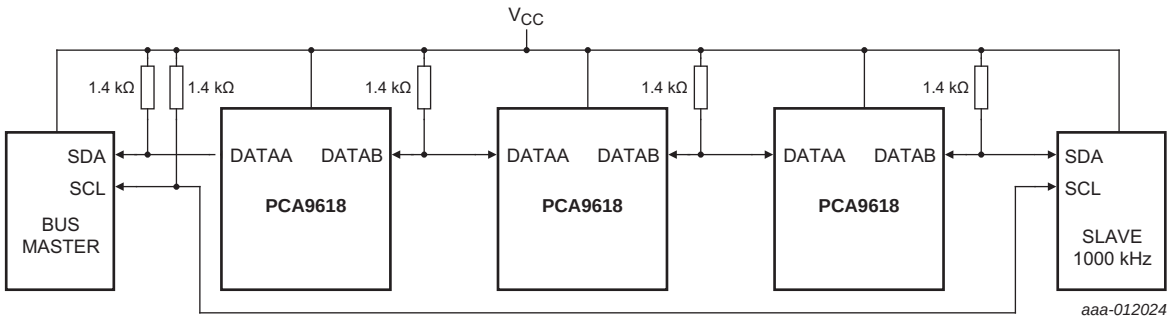


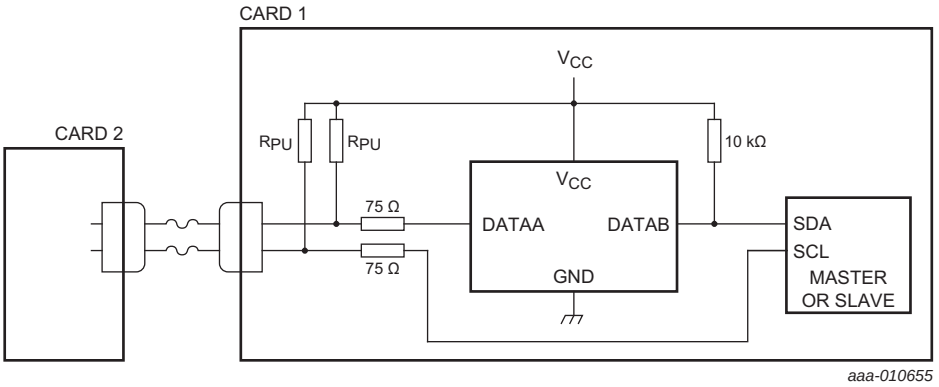
Fig 4. Typical star application

The PCA9618 provides two basic functions. It provides buffering and it provides a delay that can be used to delay the SDA in order to create an artificial hold time bridge the gap between the 0 ns I²C-bus hold time on SCL falling edge and the SMBus 300 ns hold time specification for SMBus slaves that are clocked on the SCL falling edge and not sampled.



Decoupling capacitors not shown for simplicity, but they are required. It is especially important that the decoupling for the PCA9618 V_{CC} be close to the V_{CC} pin.

Fig 5. Typical series application



Decoupling capacitors not shown for simplicity, but they are required. It is especially important that the decoupling for the PCA9618 V_{CC} be close to the V_{CC} pin.

Fig 6. Typical application of PCA9618 driving a short cable

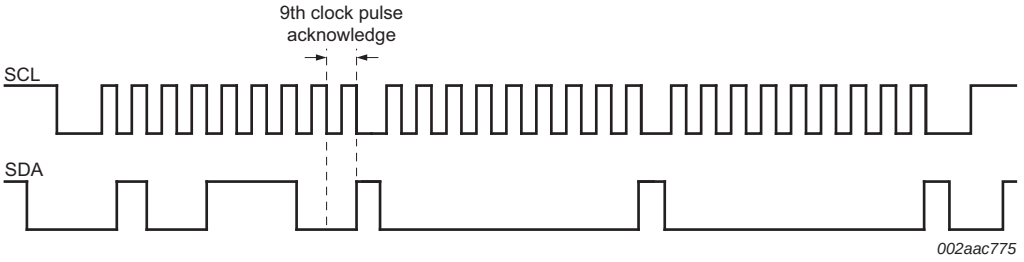


Fig 7. Bus A (2.2 V to 5.5 V bus) waveform

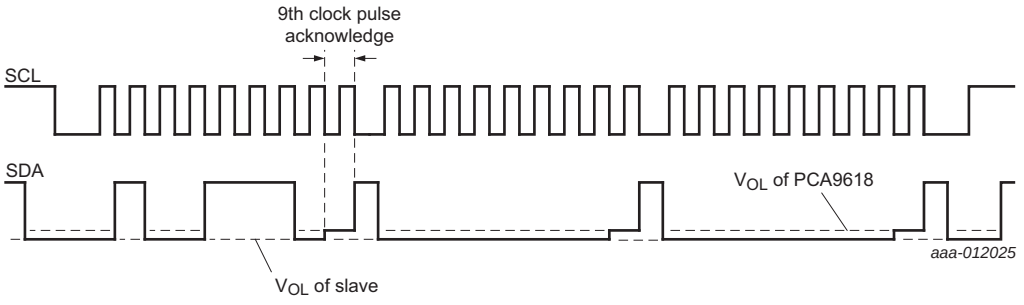


Fig 8. Bus B (2.2 V to 5.5 V) waveform

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
$V_{I/O}$	voltage on an input/output pin	port A and port B	–0.5	+7	V
$I_{I/O}$	input/output current	port A; port B	-	50	mA
I_I	input current	V_{CC}, GND	-	50	mA
P_{tot}	total power dissipation		-	100	mW
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature	operating in free air	–40	+85	°C
T_j	junction temperature		-	+125	°C

9. Static characteristics

Table 5. Static characteristics

V_{CC} = 2.2 V to 5.5 V; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values measured with V_{CC} = 2.5 V at 25 °C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{CC}	supply voltage			2.2	-	5.5	V
I_{CCH}	HIGH-level supply current	V_{CC} = 5.5 V; DATAn = V_{CC}		-	1.5	2.5	mA
I_{CCL}	LOW-level supply current	V_{CC} = 5.5 V; one DATAn = GND; other DATAn with pull-up resistors		-	1.7	2.9	mA
Input and output DATAB							
V_{IH}	HIGH-level input voltage			0.7V_{CC}	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	+0.4	V
V_{IK}	input clamping voltage	I_I = −18 mA		−1.2	-	−0.3	V
I_{LI}	input leakage current	V_I = 5.5 V		-	-	±1	μA
I_{OL}	LOW-level output current	V_O = 0.2 V		−10	-	+120	μA
V_{OL}	LOW-level output voltage	I_{OL} = 150 μA at V_{CC} = 2.2 V	[1]	0.47	-	-	V
		I_{OL} = 13 mA at V_{CC} = 2.2 V	[2]	-	0.54	0.61	V
V_{OL}–V_{IL}	difference between LOW-level output and LOW-level input voltage	V_{OL} at I_{OL} = 1 mA; guaranteed by design		60	90	160	mV
C_{io}	input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V		-	7	10	pF
		V_I = 3 V or 0 V; V_{CC} = 0 V		-	7	10	pF
Input and output DATAA							
V_{IH}	HIGH-level input voltage			0.7V_{CC}	-	5.5	V
V_{IL}	LOW-level input voltage		[3]	−0.5	-	+0.25V_{CC}	V
V_{IK}	input clamping voltage	I_I = −18 mA		−1.2	-	−0.3	V
I_{LI}	input leakage current	V_I = 5.5 V		-	-	±1	μA
I_{IL}	LOW-level input current	V_I = 0.2 V		-	-	10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 13 mA; V_{CC} = 2.2 V		-	0.1	0.2	V
C_{io}	input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V		-	7	10	pF
		V_I = 3 V or 0 V; V_{CC} = 0 V		-	7	10	pF

[1] Pull-up should result in $I_{OL} \geq 150$ μA.

[2] Guaranteed by design and characterization.

[3] V_{IL} for port A with envelope noise must be below 0.3V_{CC} for stable performance.

[4] Power supply decoupling capacitors need to be present for V_{CC} and the 0.1 μF decoupling for V_{CC} needs to be located near the V_{CC} pin.

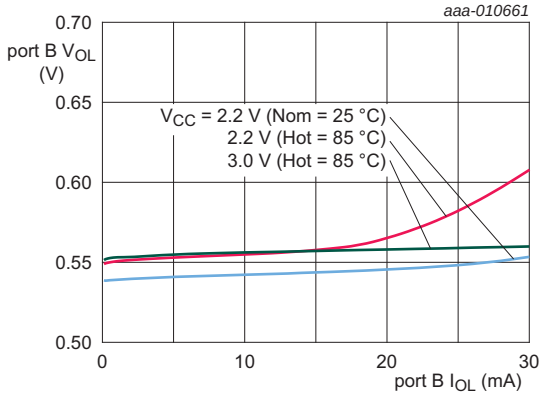


Fig 9. Port B V_{OL} versus I_{OL}

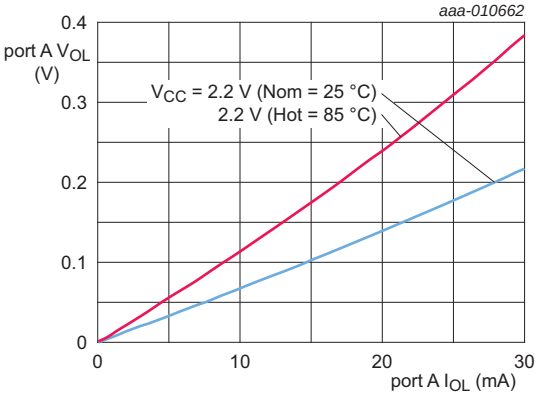
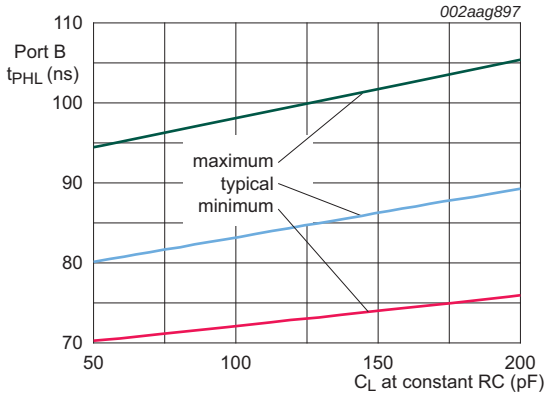


Fig 10. Port A V_{OL} versus I_{OL}



RC = 67.5 ns, V_{CC} = 2.5 V, and T_{amb} = 25 °C.

Fig 11. Nominal port B t_{PHL} with load capacitance at constant RC

10. Dynamic characteristics

Table 6. Dynamic characteristics

V_{CC} = 2.2 V to 5.5 V; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.[1][2]

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	port B to port A; Figure 14		-42	−65	−103	ns
t_{PLH2}	LOW to HIGH propagation delay 2	port B to port A; Figure 14	[4]	67	94	130	ns
t_{PHL}	HIGH to LOW propagation delay	port B to port A; Figure 12		46	76	152	ns
t_{TLH}	LOW to HIGH output transition time	port A; Figure 12	[5]	-	60	-	ns
SR_f	falling slew rate	port A; $0.7V_{CC}$ to $0.3V_{CC}$		0.022	0.037	0.11	V/ns
t_{PLH}	LOW to HIGH propagation delay	port A to port B; Figure 13	[6]	40	60	102	ns
t_{PHL}	HIGH to LOW propagation delay	port A to port B; Figure 13	[6]	63	80	173	ns
t_{TLH}	LOW to HIGH output transition time	port B; Figure 13	[5]	-	60	-	ns
SR_f	falling slew rate	port B; $0.7V_{CC}$ to $0.3\ V_{CC}$		0.029	0.056	0.09	V/ns

[1] Times are specified with loads of 1.35 kΩ pull-up resistance and 50 pF load capacitance on port A and port B, and a falling edge slew rate of 0.05 V/ns input signals.

[2] Pull-up voltages are V_{CC} on port A and V_{CC} on port B.

[3] Typical values were measured with V_{CC} = 2.5 V at T_{amb} = 25 °C, unless otherwise noted.

[4] The t_{PLH2} delay data from port B to port A is measured at 0.45 V on port B to $0.5V_{CC}$ on port A.

[5] The t_{TLH} of the bus is determined by the pull-up resistance (1.35 kΩ) and the total capacitance (50 pF).

[6] The proportional delay data from port A to port B is measured at $0.5V_{CC}$ on port A to $0.5V_{CC}$ on port B.

10.1 AC waveforms

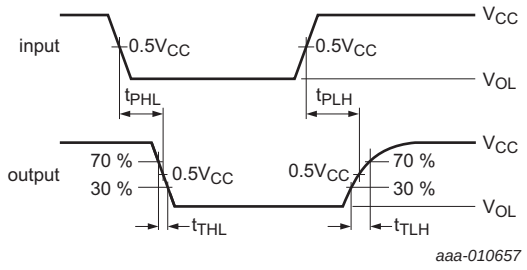


Fig 12. Propagation delay and transition times; port B to port A

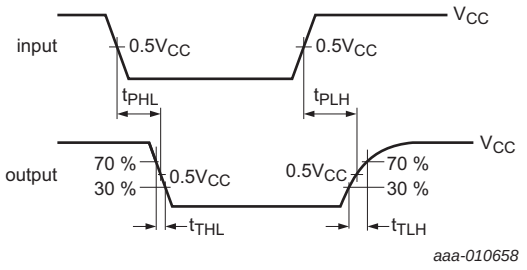


Fig 13. Propagation delay and transition times; port A to port B

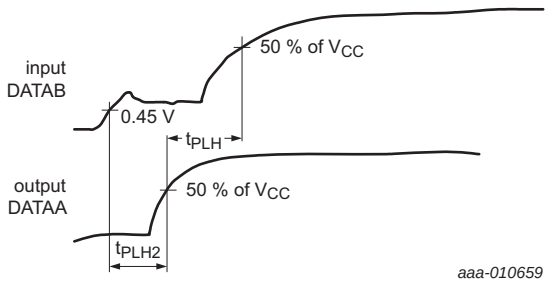
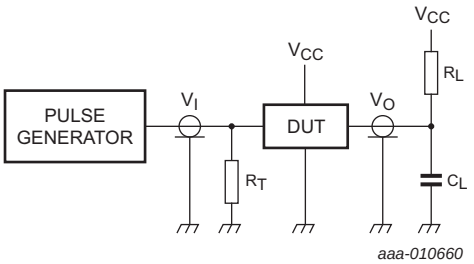


Fig 14. Propagation delay

11. Test information



R_L = load resistor; 1.35 kΩ on port A and port B.

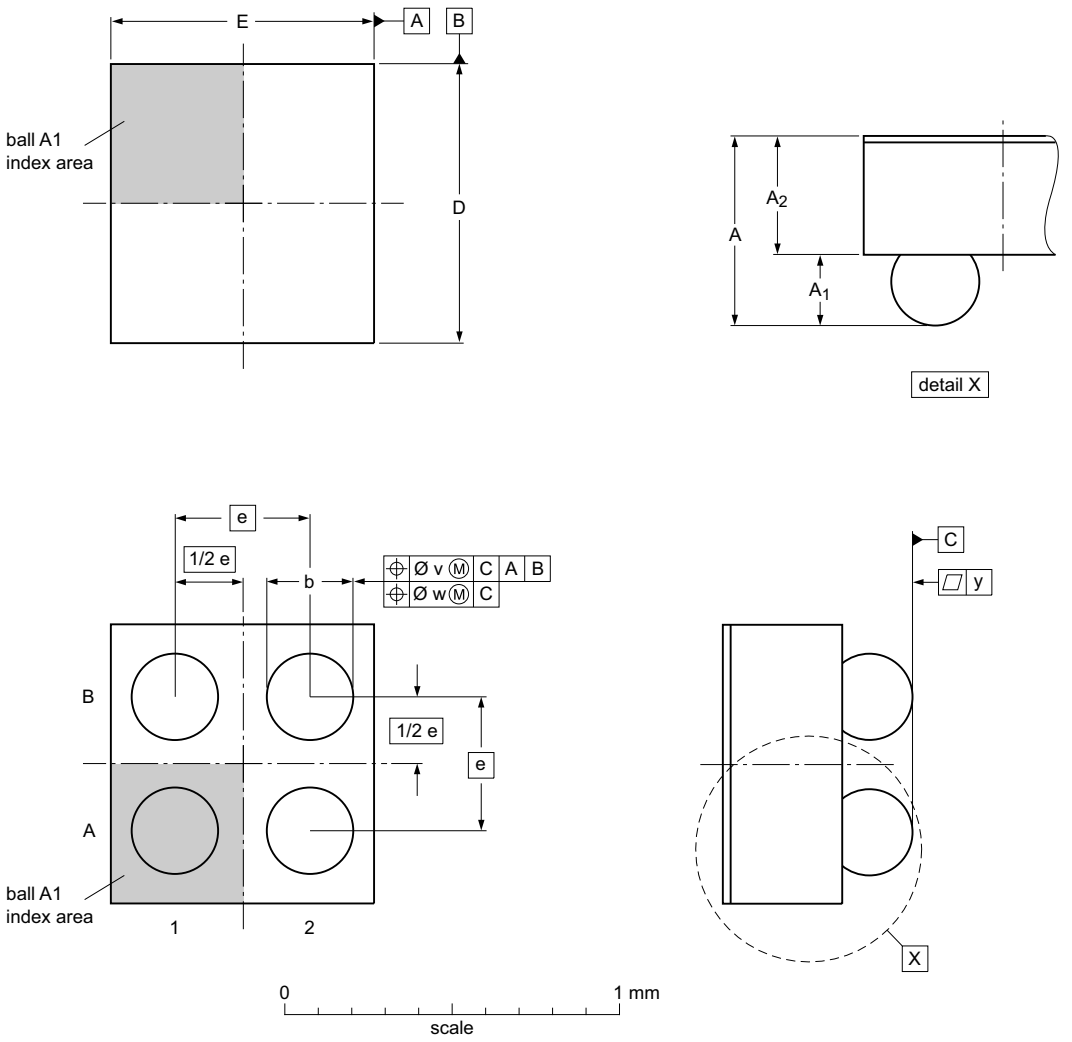
C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance should be equal to Z_o of pulse generators

Fig 15. Test circuit for open-drain outputs

12. Package outline

WLCSP4: wafer level chip-scale package; 4 bumps; 0.83 x 0.78 x 0.53 mm (backside coating included) **SOT1375-3**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	v	w	y
mm	max	0.577	0.240	0.338	0.310	0.855	0.805				
	nom	0.530	0.210	0.322	0.260	0.830	0.780	0.4	0.02	0.015	0.03
	min	0.483	0.180	0.306	0.233	0.805	0.755				

wlcsp4_pca9618uk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1375-3						~~14-02-05~~ 15-10-01

Fig 16. Package outline PCA9618UK (WLCSP4)

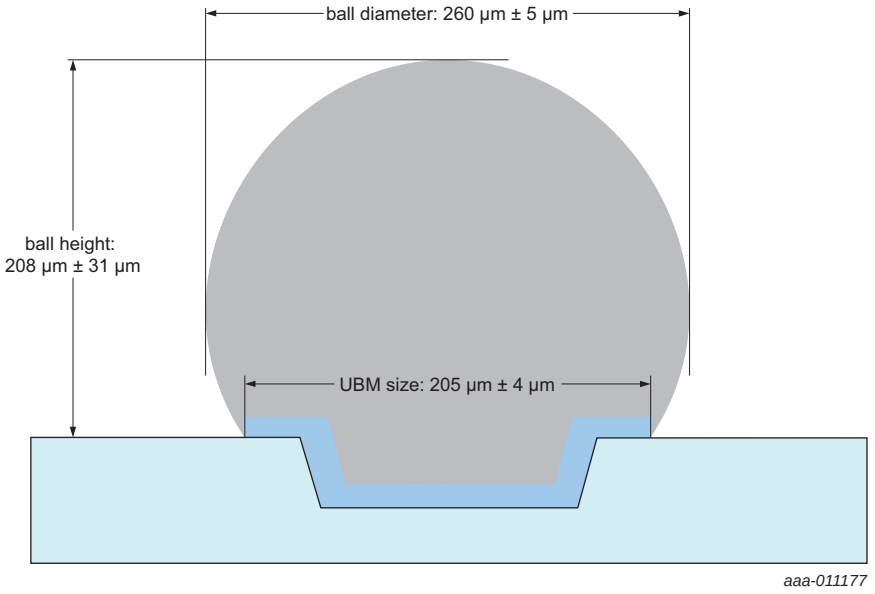


Fig 17. Ball structure

13. Soldering of WLCSP packages

13.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

13.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

13.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board

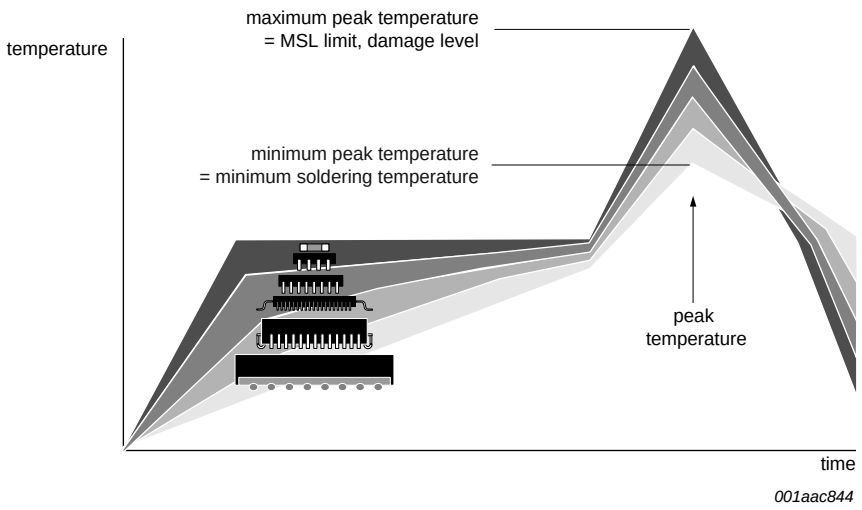
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7.

Table 7. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

13.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

13.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

13.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 “Surface mount reflow soldering description”*.

13.3.4 Cleaning

Cleaning can be done after reflow soldering.

14. Soldering: PCB footprints

Footprint information for reflow soldering of WLCSP4 package **PCA9618_SMD**

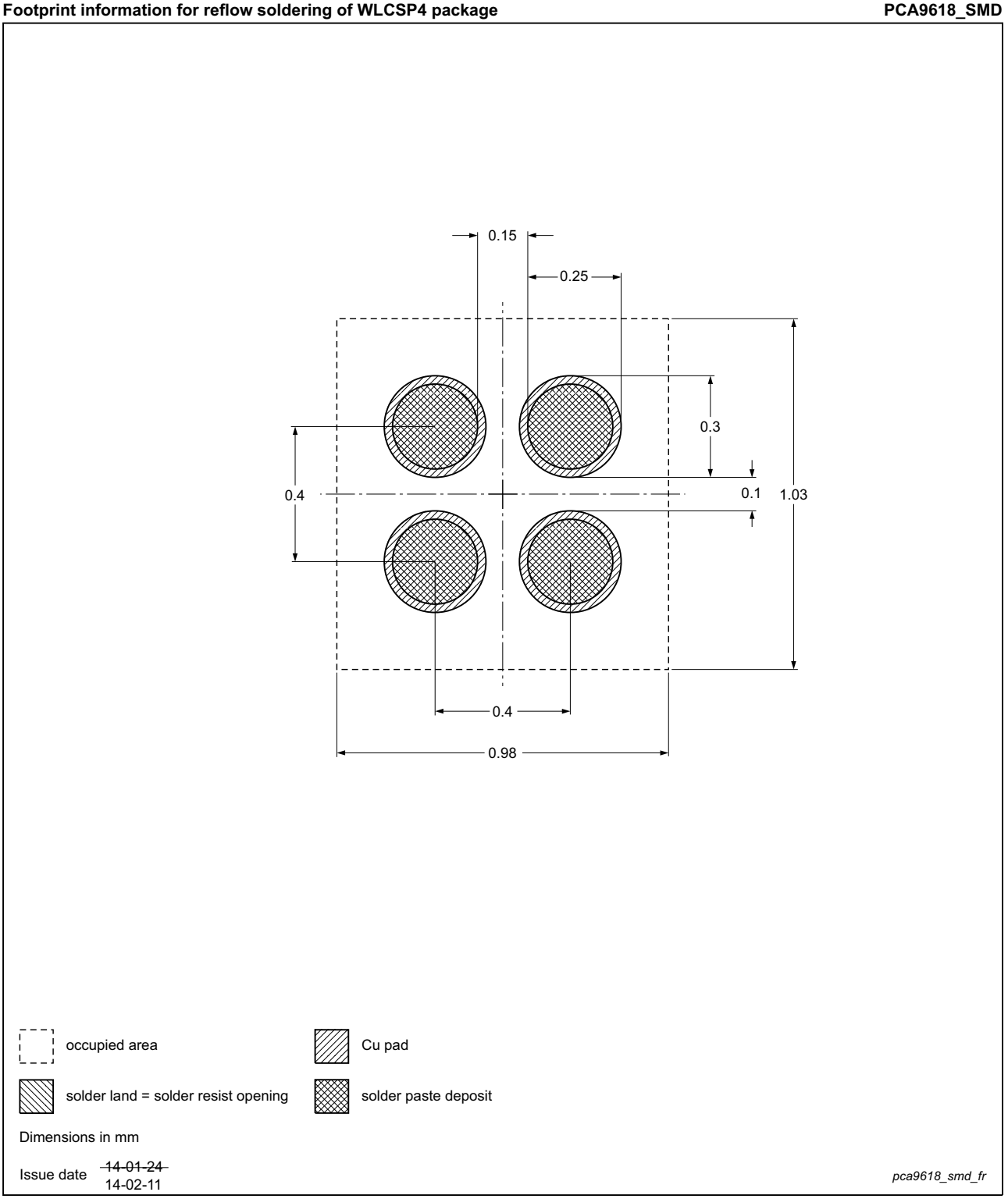
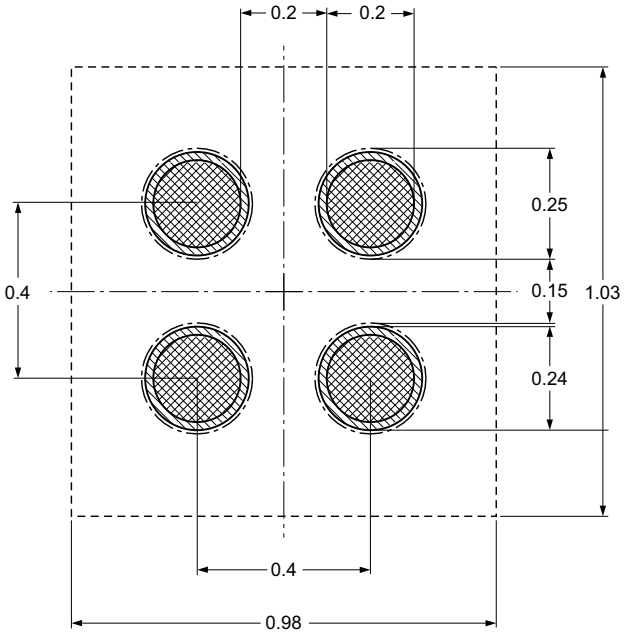


Fig 19. PCB footprint for PCA9618UK (WLCSP4); reflow soldering; Solder Mask Defined (SMD)

Footprint information for reflow soldering of WLCSP4 package **PCA9618_NSMD**



occupied area

solder resist

solder land = Cu pad

solder paste deposit

Dimensions in mm

Issue date ~~14-01-24~~ 14-02-11

pca9618_nsmd_fr

Fig 20. PCB footprint for PCA9618UK (WLCSP4); reflow soldering; Non-Solder Mask Defined (NSMD)

15. Abbreviations

Table 8. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
PMBus	Power Management Bus
RC	Resistor-Capacitor network
SMBus	System Management Bus

16. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9618 v.1	20160113	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents

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