

## Evaluation Board for the **ADG888** CMOS, Dual DPDT Switch in the WLCSP Package

### FEATURES

Evaluation board for the **ADG888**  
Various linking options

### INTRODUCTION

The [EVAL-ADG888EBZ](#) evaluation board was designed to test the **ADG888** dual, double pole, double throw (DPDT), CMOS switch with a minimum of effort.

The **ADG888** is a low voltage dual, DPDT CMOS device available in WLCSP, TSSOP, and LFCSP packages. It has been optimized for high performance audio switching, and due to its low power and small physical size, it is ideal for portable devices.

This device has ultralow on resistance of less than  $0.8 \Omega$  over the full temperature range and exhibits break-before-make switching action.

Full data on the **ADG888** is available in the **ADG888** data sheet available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

### EVALUATION BOARD PICTURE

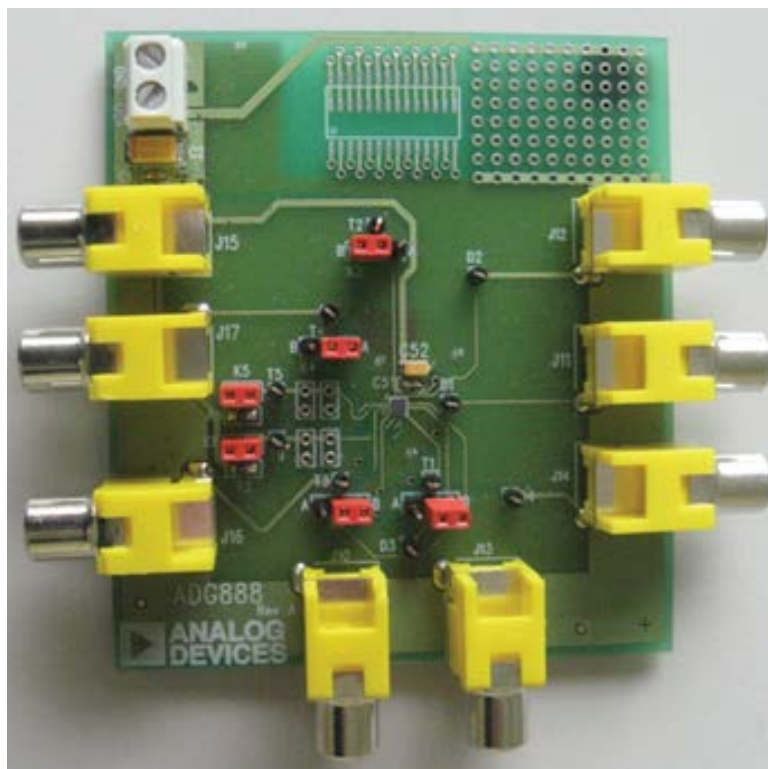


Figure 1.

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**REVISION HISTORY**

8/12—Revision 0: Initial Version

## EVALUATION BOARD HARDWARE

The [EVAL-ADG888EBZ](#) evaluation board has been designed for testing the functionality of the device. Test points have been placed on each audio jack to measure the voltage level at each pin.

### OPERATING THE [EVAL-ADG888EBZ](#) EVALUATION BOARD

#### Power Supplies

The [EVAL-ADG888EBZ](#) evaluation board has one analog power supply connector. VDD can vary from 1.8 V to 5.5 V, and GND must be connected to ground on the power supply.

V<sub>DD</sub> is decoupled to ground via a 10 μF tantalum capacitor (C2) and a 0.1 μF ceramic capacitor (C1) at the input to the evaluation board.

#### Source and Drain Pins

There are eight audio jacks available on the [EVAL-ADG888EBZ](#) evaluation board to test the capabilities of the [ADG888](#) chip. Four of the jacks (J10, J15, J16, and J17) connect to the eight source pins on the [ADG888](#), and four of the jacks (J11, J12, J13, and J14) connect to the four drain pins. The chip is bidirectional; therefore, each jack can function as either an input or an output.

The four link connections, K1 to K4, on the board are associated with the four source jacks and determine which source pins are connected to the jacks. In Position A, the first DPDT source pins, controlled by IN1, are connected to the jacks. In Position B, the second DPDT source pins, controlled by IN2, are connected to the jacks. Table 1 shows the options for these links.

**Table 1. Source Jack Link Options**

Link Number	Source Jack	Function	
		Position A	Position B
K1	J10	Selects S1A	Selects S3A
K2	J15	Selects S1B	Selects S3B
K3	J16	Selects S2A	Selects S4A
K4	J17	Selects S2B	Selects S4B

#### IN Pins

The remaining two links, K5 and K9, control the logic inputs, IN1 and IN2, respectively, of the [ADG888](#). The input is set logic high by removing the link header, and the input is set logic low by inserting the link header.

The connections between source and drain audio jacks are detailed in Table 2.

**Table 2. Audio Jack Connections**

Source Link Position	IN Link State	ADG888 Switch States		Board Connections
Position A (K1, K2, K3, K4)	K5 (inserted)	S1A, S2A (off)	S1B, S2B (on)	J15 to J11, J17 to J12
	K5 (removed)	S1A, S2A (on)	S1B, S2B (off)	J10 to J11, J16 to J12
Position B (K1, K2, K3, K4)	K9 (inserted)	S3A, S4A (off)	S3B, S4B (on)	J15 to J13, J17 to J14
	K9 (removed)	S3A, S4A (on)	S3B, S4B (off)	J10 to J13, J16 to J14

EVALUATION BOARD SCHEMATICS AND ARTWORK

10828-001

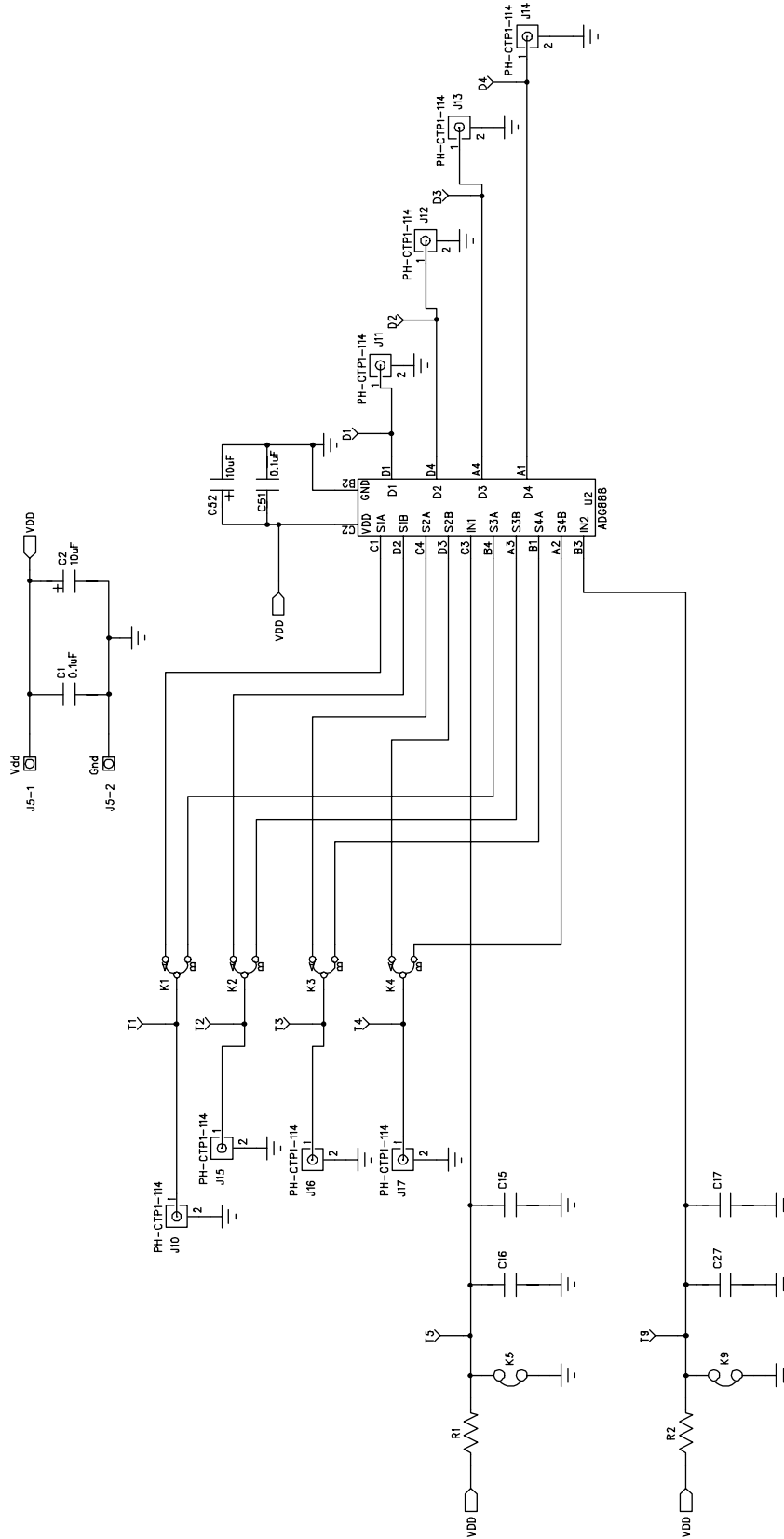


Figure 2. EVAL-ADG888EBZ Evaluation Board Schematic

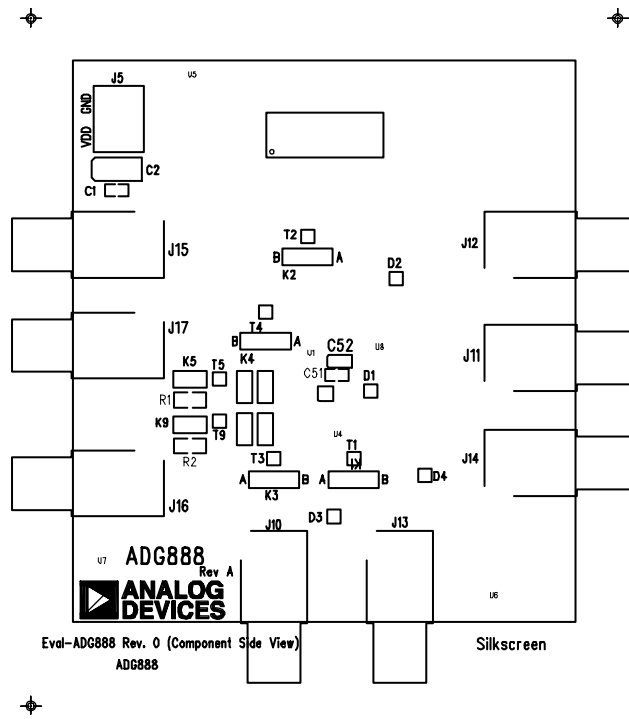


Figure 3. EVAL-ADG888EBZ Evaluation Board, Component Placement Drawing

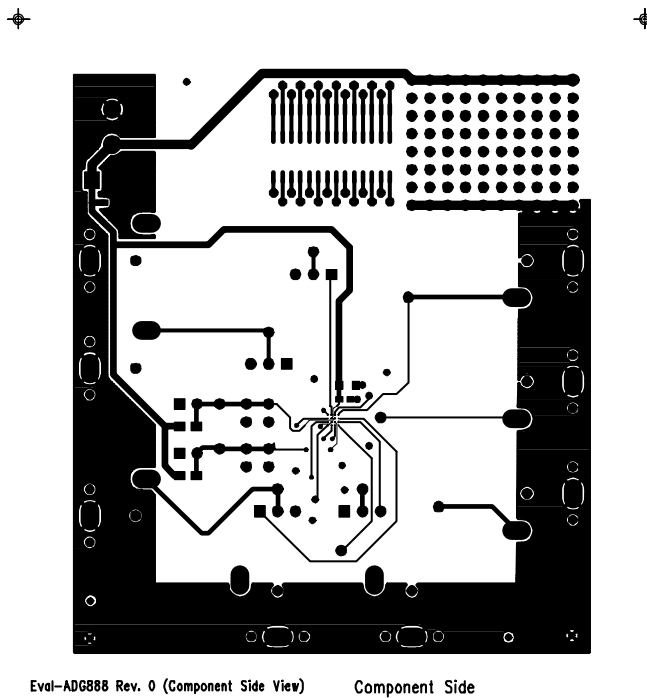
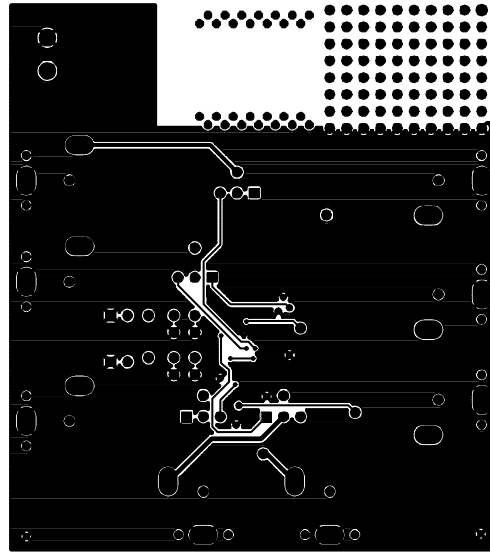


Figure 4. EVAL-ADG888EBZ Evaluation Board, Component Side Printed Circuit Board (PCB) Drawing



Eval-ADG888 Rev. 0 (Component Side View)

Solder Side

10828-004



Figure 5. [EVAL-ADG888EBZ](#) Evaluation Board, Solder Side PCB Drawing

**COMPONENT LIST**

Table 3.

Item	Quantity	Reference	Description	Supplier Number
1	2	C1, C51	0.1 $\mu$ F capacitors	FEC 753-567
2	1	C2	10 $\mu$ F capacitor	FEC 197-518
3	4	C15, C16, C17, C27	CAP\MR04	Low profile sockets
4	1	C52	10 $\mu$ F capacitor, CAP\TAJ_A	FEC 197-130
5	4	D1 to D4	Test points	FEC 873-1128
6	1	J5	CON\POWER	FEC 151-789
7	6	J10 to J17	Phono sockets	PH-CTP1-114
8	4	K1 to K4	Link-3P_TEXT_INV	FEC 1022248 and FEC 150-412
9	2	K5, K9	SIP-2P	FEC 1022247 and FEC 150-411
10	2	R1, R2	10 k $\Omega$ resistors	FEC 9333720
10	6	T1 to T5, T9	Test points	FEC 873-1128
11	1	U2	<a href="#">ADG888</a> , 16-ball WLCSP	<a href="#">ADG888BCBZ</a>
12	1	U3	SO28WB_NB	Pads to be kept free of solder

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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