MityDSP™
Document

Document: MityDSP-L138, MitySOM-1808, MitySOM-1810, MityDSP-6748 Carrier Board Design Guide

Revision: 1.7

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1 Overview

1.1 Fast Facts for Getting Started

Facts	MityDSP-L138, MitySOM-1808, MitySOM-1810, MityDSP-6748
Required socket connector	FCI 10033853-152FSLF, FCI 10116658-152FSLF or equivalent
Voltages required	3.3V
Supported I/O standards	LVCMOS33
SOC Peripherals*	3x UART, 2x SPI, EMAC (MII or RMII), 2x I2C, McASP, 2x McBSP
*SOC peripherals share pins, see SOC datasheet for specific pin-multiplexing options	

1.2 Introduction

The MityDSP-L138, MitySOM-1808, MitySOM-1810 and MityDSP-6748 modules are System On Modules (SOMs) designed to be easy to integrate into an end-user embedded system. The modules integrate many crucial elements of an embedded system, and do so with an established design framework utilizing a common set of core libraries. End-user design of the application PCB is also intended to be as simple as possible, allowing the PCB designer to concentrate on the custom I/O interfaces – especially analog & mixed-signal – instead of getting distracted with the learning curve of designing a brand new embedded digital system from scratch.

1.3 MityDSP-L138 Family Modules

The MityDSP-L138, MitySOM-1808, and MityDSP-6748 family of modules represents a 3rd generation SOM in the MityDSP product line. These modules are based on a Texas Instruments OMAP-L138, Sitara-1808, Sitara-1810 and the TMS320C6748 System On Chip (SOC) modules, respectively. Each of these SOC modules are pin compatible devices that employ one or both of an ARM 9 core and a DSP 674x floating point DSP core according to the table below.

Core	OMAP-L138	AM1808	TMS320C6748
ARM926EJ-S 300/375/456 MHz	Y	Y	N
DSP 674X Floating Point DSP 300/375/456 MHz	Y	N	Y

Each module includes power management, DDR2 SDRAM, NAND and NOR Flash memories, and is interfaced by a 200-pin low-profile SO-DIMM card-edge connector. Carrier board design for these types of MityDSP is the main focus of this document.

The 2nd generation module, the MityDSP-Pro (MityDSP-6455), is based on a Texas Instruments TMS320C645x DSP, includes DDR2 SDRAM and Flash memories, and is interfaced by the same 200-pin SO-DIMM card-edge connector and a 100-pin high-density, low-profile Hirose connector. The module integrates a large Xilinx Spartan3 FPGA for implementing required on-board logic and I/O interfaces, but primarily for end-user customizable logic and I/O interfaces. The module also incorporates a number of high bandwidth I/O interfaces including: PCI/HPI, Serial RapidIO, and Gigabit Ethernet interfaces provided by the DSP; and DDR SDRAM dedicated to the FPGA.

The 1st generation family of modules, the MityDSP and MityDSP-XM (MityDSP-6711 and MityDSP-6711XM), are based on a Texas Instruments TMS3206711 DSP, include SDRAM and Flash memories, and are interfaced using a 144-pin SO-DIMM card edge connector. The module integrates a Xilinx Spartan 3 FPGA for implementing required on-board logic and I/O interfaces.

All types of MityDSP are available with options for speed grade, memory size, FPGA size (or complete removal), operating temperature ranges, and RoHS / non-RoHS compliance. Please contact Critical Link for the current list of MityDSP and MitySOM variants.

1.4 MityDSP-L138F Family Modules (With FPGA)

An available option to the MityDSP-L138 family of modules is a module that includes a Spartan6 FPGA. This unit is slightly larger than the non-FPGA module, and it requires slightly more power to run. Many of the IO pins previously reserved for SoC functions have been instead routed to FPGA pins, but those functions are still available by passing them through the FPGA. The difference in the part name is the addition of the “F” at the end. See the datasheets and design guide for these parts for pin-out information.

1.5 Module Dimensions

A dimensioned drawing of module is included below in Figure 1.

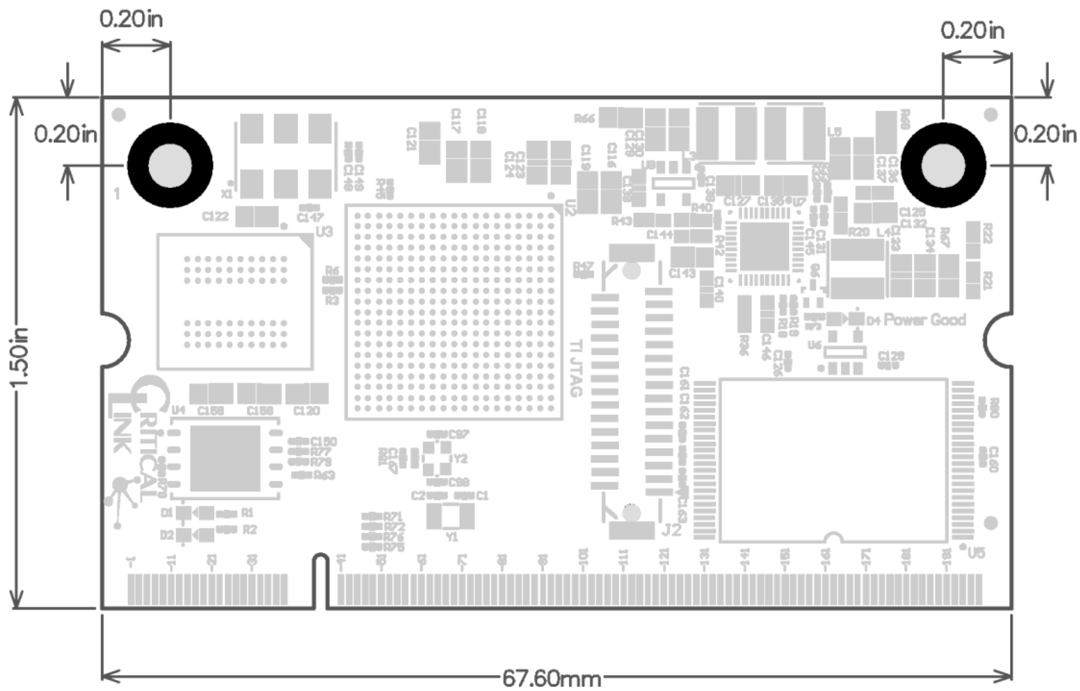

Figure 1: MityDSP-L138, MitySOM-1808, MitySOM-1810 MityDSP-6748 Mechanical Drawing

2 Connectors

All types of MityDSP utilize SO-DIMM style edge-connectors for main connectivity with the end user application PCB. These connectors were chosen for their high density, compact size, ease of procurement, and low cost. With edge connectors, a physical socket component is only required on one side – the main PCB side. The SO-DIMM standard also allows the MityDSP module to lay flat, in parallel with the main PCB, as they were intended for use by memory modules in compact equipment, such as laptops.

2.1 Card-edge compatibility

The MityDSP-L138 family of SOMs is designed to plug into a 200-pin SO-DIMM DDR2 RAM socket. These sockets are used for memory on PC laptop systems. Please note that the MityDSP is NOT electrically compatible with the DDR2 socket standard, and intermixing modules/sockets from the two standards would very possibly cause permanent damage to one or both sides.

2.2 Module Pin-out

The SO-DIMM card edge interface contains 4 classes of signals:

Power (PWR)
Dedicated signals mapped to the processor (D)
Dedicated signals when NAND memory is populated on the module (D*)
Multi-function signals mapped to the processor (M)

Table 1: MityDSP-L138, MitySOM-1808, MitySOM-1810 and MityDSP-6748 Card-edge (J100) Pin-out

Pin	Ball	Type	I/O	Signal	Pin	Ball	Type	I/O	Signal
1	-	PWR	-	+3.3 V in	2	-	PWR	-	+3.3 V in
3	-	PWR	-	+3.3 V in	4	-	PWR	-	+3.3 V in
5	-	PWR	-	+3.3 V in	6	-	PWR	-	+3.3 V in
7	-	PWR	-	GND	8	-	PWR	-	GND
9	-	PWR	-	GND	10	-	PWR	-	GND
11	K14	D	I	RESET_IN#	12	-	D	I	EXT_BOOT#
13	J1	D	O	SATA_TX_P	14	A4	M	I/O	GP0_7
15	J2	D	O	SATA_TX_N	16	A3	M	I/O	GP0_10
17	L1	D	I	SATA_RX_P	18	A2	M	I/O	GP0_11
19	L2	D	I	SATA_RX_N	20	A1	M	I/O	GP0_15
21	P16	D	I	USB0_ID	22	B4	M	I/O	GP0_6
23	P18	D	I/O	USB1_D_N	24	B1	M	I/O	GP0_14
25	P19	D	I/O	USB1_D_P	26	B2	M	I/O	GP0_12
27	N19	D	O	USB0_VBUS	28	B3	M	I/O	GP0_5
29	M18	D	I/O	USB0_D_N	30	C2	M	I/O	GP0_13
31	M19	D	I/O	USB0_D_P	32	C3	M	I/O	GP0_1

Pin	Ball	Type	I/O	Signal	Pin	Ball	Type	I/O	Signal
33	K18	D	O	USB0_DRVVBUS	34	C4	M	I/O	GP0_4
35	-	D	-	3V RTC Battery	36	C5	M	I/O	GP0_3
37	-	PWR	-	+3.3 V in	38	-	PWR	-	+3.3 V in
39	-	PWR	-	+3.3 V in	40	-	PWR	-	+3.3 V in
41	-	PWR	-	GND	42	-	PWR	-	GND
43	H17	D	I/O	SPI1_MISO	44	D4	M	I/O	GP0_2
45	G17	D	I/O	SPI1_MOSI	46	E4	M	I/O	GP0_0
47	H16	D	I/O	SPI1_ENA	48	F4	M	I/O	GP0_8
49[1]	G19	D	I/O	SPI1_CLK	50	D5	M	I/O	GP0_9
51	F18	M	I/O	SPI1_SCS[1]	52	A12	M	I/O	MMCSD0_DAT[7]
53	-	D	-	Reserved	54	C11	M	I/O	MMCSD0_DAT[6]
55[2]	G16	D	I/O	I2C0_SCL	56	E12	M	I/O	MMCSD0_DAT[5]
57[2]	G18	D	I/O	I2C0_SDA	58	B11	M	I/O	MMCSD0_DAT[4]
59	F16	M	I/O	UART2_TXD / I2C1_SDA	60	E11	M	I/O	MMCSD0_DAT[3]
61	F17	M	I/O	UART2_RXD / I2C1_SCL	62	C10	M	I/O	MMCSD0_DAT[2]
63	-	PWR	-	GND	64	-	PWR	-	GND
65	F19	M	O	UART1_TXD	66	A11	M	I/O	MMCSD0_DAT[1]
67	E18	M	I	UART1_RXD	68	B10	M	I/O	MMCSD0_DAT[0]
69	E16	M	O	MDIO_CLK	70	A10	M	I/O	MMCSD0_CMD
71	D17	M	I/O	MDIO_D	72	E9	M	O	MMCSD0_CLK
73	D19	M	I	MII_RXCLK	74	D3	M	I	MII_TXCLK
75	C17	M	I	MII_RXDV	76	E3	M	O	MII_TXD[3]
77	D16	M	I	MII_RXD[0]	78	E2	M	O	MII_TXD[2]
79	E17	M	I	MII_RXD[1]	80	E1	M	O	MII_TXD[1]
81	D18	M	I	MII_RXD[2]	82	F3	M	O	MII_TXD[0]
83	C19	M	I	MII_RXD[3]	84	C1	M	O	MII_TXEN
85	-	PWR	-	GND	86	-	PWR	-	GND
87	C18	M	I	MII_CRS	88	D1	M	I	MII_COL
89	C16	M	I	MII_RXER	90	-	D	-	NC
91	A18	M	O	EMA_CS[0]	92	W15	M	I/O	UPP_CHA_START
93	B15	D*	O	EMA_OE	94	V15	M	I	VP_CLKIN1
95	C15	M	O	EMA_BA[0]	96	U18	M	I/O	UPP_D[15] / RMII_TXD[1]
97	A15	M	O	EMA_BA[1]	98	V16	M	I/O	UPP_D[14] / RMII_TXD[0]
99	C14	M	O	EMA_A[0]	100	R14	M	I/O	UPP_D[13] / RMII_TXEN
101	D15	D*	O	EMA_A[1]	102	W16	M	I/O	UPP_D[12] / RMII_RXD[1]
103	B14	D*	O	EMA_A[2]	104	V17	M	I/O	UPP_D[11] / RMII_RXD[0]
105	D14	M	O	EMA_A[3]	106	W17	M	I/O	UPP_D[10] / RMII_RXER
107	-	PWR	-	GND	108	-	PWR	-	GND
109	A14	M	O	EMA_A[4]	110	W18	M	I/O	UPP_D[9] / RMII_REF_CLK
111	C13	M	O	EMA_A[5]	112	W19	M	I/O	UPP_D[8] / RMII_CRS_DV
113	E13	M	O	EMA_A[6]	114	V18	M	I/O	UPP_D[7]

Pin	Ball	Type	I/O	Signal	Pin	Ball	Type	I/O	Signal
115	B13	M	O	EMA_A[7]	116	V19	M	I/O	UPP_D[6]
117	A13	M	O	EMA_A[8]	118	U16	M	I/O	UPP_CHA_ENABLE
119	D12	M	O	EMA_A[9]	120	U19	M	I/O	UPP_D[5]
121	C12	M	O	EMA_A[10]	122	T16	M	I/O	UPP_D[4]
123	B12	M	O	EMA_A[11]	124	R18	M	I/O	UPP_D[3]
125	D13	M	O	EMA_A[12]	126	R19	M	I/O	UPP_D[2]
127	D11	M	O	EMA_A[13]	128	T15	M	I/O	UPP_CHA_WAIT
129	-	PWR	-	GND	130	-	PWR	-	GND
131	E6	D*	I/O	EMA_D[15]	132	R15	M	I/O	UPP_D[1]
133	C7	D*	I/O	EMA_D[14]	134	P17	M	I/O	UPP_D[0]
135	B6	D*	I/O	EMA_D[13]	136	U17	M	I/O	UPP_CHA_CLK
137	A6	D*	I/O	EMA_D[12]	138	J4	M	I/O	UPP_CHB_ENABLE
139	D6	D*	I/O	EMA_D[11]	140	K3	M	O	VP_CLKOUT2
141	A7	D*	I/O	EMA_D[10]	142	H3	M	I	VP_CLKIN2
143	D9	D*	I/O	EMA_D[9]	144	G3	M	I/O	UPP_CHB_WAIT
145	E10	D*	I/O	EMA_D[8]	146	G2	M	I/O	UPP_CHB_START
147	D7	D*	I/O	EMA_D[7]	148	G1	M	I/O	UPP_CHB_CLK
149	C6	D*	I/O	EMA_D[6]	150	W14	M	I	VP_CLKIN0
151	-	PWR	-	GND	152	-	PWR	-	GND
153	E7	D*	I/O	EMA_D[5]	154	P4	M	I/O	LCD_D[15]
155	B5	D*	I/O	EMA_D[4]	156	R3	M	I/O	LCD_D[14]
157	E8	D*	I/O	EMA_D[3]	158	R2	M	I/O	LCD_D[13]
159	B8	D*	I/O	EMA_D[2]	160	R1	M	I/O	LCD_D[12]
161	A8	D*	I/O	EMA_D[1]	162	T3	M	I/O	LCD_D[11]
163	C9	D*	I/O	EMA_D[0]	164	T2	M	I/O	LCD_D[10]
165	C8	M	O	EMA_WEN_DQM[0]	166	T1	M	I/O	LCD_D[9]
167	A5	M	O	EMA_WEN_DQM[1]	168	U3	M	I/O	LCD_D[8]
169	D8	M	O	EMA_SDCKE	170	U2	M	I/O	LCD_D[7]
171[3]	B7	M	O	EMA_CLK	172	U1	M	I/O	LCD_D[6]
173	-	PWR	-	GND	174	-	PWR	-	GND
175	B9	D*	O	EMA_WE	176	G4	M	O	LCD_VSYNC
177	A9	M	O	EMA_CAS	178	H4	M	O	LCD_HSYNC
179	A16	M	O	EMA_RAS	180	V3	M	I/O	LCD_D[5]
181	B17	M	O	EMA_CS[2]	182	F1	M	O	LCD_PCLK
183	F9	M	O	EMA_CS[4]	184	V2	M	I/O	LCD_D[4]
185	B16	M	O	EMA_CS[5]	186	V1	M	I/O	LCD_D[3]
187	T17	D	O	RESET_OUT	188	W3	M	I/O	LCD_D[2]
189	J3	M	I	VP_CLKIN3	190	W2	M	I/O	LCD_D[1]
191	K4	M	O	VP_CLKOUT3	192	W1	M	I/O	LCD_D[0]
193	F2	M	O	LCD_MCLK	194	R5	M	O	LCD_AC_ENB_CS
195	-	PWR	-	GND	196	-	PWR	-	GND

Pin	Ball	Type	I/O	Signal	Pin	Ball	Type	I/O	Signal
197[4]	D10	M	O	EMA_A_RW	198	B18[4]	D*	I	EMA_WAIT[0]
199[4]	A17	D*	O	EMA_CS[3]	200	B19[4]	M	I	EMA_WAIT[1]

Note 1: Pin 49, SPI1_CLK, has a 100K Ohm pull-down resistor on the module
Note 2: Pins 55 and 57 have 4.70K pull-up resistors on the module
Note 3: Pin 171, EMA_CLK, has a 49.9 Ohm resistor in series with the signal on the module
Note 4: Pins 197, 198, 199 and 200 have 1.00K Ohm resistors in series with the signals on the module

The signal group description for the above pins is included in Table 2.

Table 2: MityDSP-L138, MitySOM-1808, MityDSP-6748 Signal Group Description

Signal / Group	Type	Description
3.3 V in	N/A	3.3 volt input power referenced to GND.
EXT_BOOT#	I	Bootstrap configuration pin. Pull low to configure booting from external UART1.
RESET_IN#	I	Manual Reset. When pulled to GND for a minimum of 1 usec, resets the DSP processor.
SPI1_*	I/O	Serial Peripheral Interface 1 pins. These pins are direct connects to the corresponding SPI1_* pins on the OMAP-L138 processor. The SPI1_* function pins are multiplexed with other functions. These include PWM, Timers, UARTs, I2C0, and GPIO. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.
MII_*	I/O	Media Independent Interface (Ethernet) pins. These pins are direct connects to the corresponding MII_* pins on the OMAP-L138 processor. The MII_* function pins are multiplexed with other functions. These include SPI0, PWM, Timers, UART0, MCBSP, MCASP, and GPIO. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.
MDIO_DAT MDIO_CLK	I/O	MII/RMII Management Interface pins. The MDIO_CLK and MDIO_DAT signals are direct connects to the corresponding MDIO_* signals on the OMAP-L138 processor. The MDIO_* function pins are multiplexed with other functions. These include SPI0 and Timer functions. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.

Signal / Group	Type	Description
GP0_*	I/O	General Purpose / multiplexed pins. These pins are direct connects to the corresponding GP0[*] pins on the OMAP-L138 processor. The include support for the McASP, general purpose I/O, UART flow control, and McBSP 1. For details please refer to the OMAP-L138 processor specifications.
SATA_TX_P SATA_TX_N	O	Serial ATA Controller Transmit pins. These pins are direct connects to the corresponding SATA_TX_* pins on the OMAP-L138 processor. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.
SATA_RX_P SATA_RX_N	I	Serial ATA Controller Receive pins. These pins are direct connects to the corresponding SATA_RX_* pins on the OMAP-L138 processor. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.
GND	N/A	System Digital Ground.
EMA_*	I/O	EMIF-A pins. These pins are direct connects to the corresponding EMA_* pins on the OMAP-L138 processor. Alternatively, these pins can be configured as GPIOs. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.
UPP_*	I/O	Universal Parallel Port pins. These pins are direct connects to the corresponding UPP_* pins on the OMAP-L138 processor. The UPP_* function pins are multiplexed with other functions. These include RMII, VP_DIN, MMCSD1, and GPIO. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.
RMII_*	I/O	Reduced Media Independent Interface pins. These pins are direct connects to the corresponding RMII_* pins on the OMAP-L138 processor. The RMII_* function pins are multiplexed with other functions. These include UPP and VP_DIN. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.
LCD_*	I/O	Liquid Crystal Display pins. These pins are direct connects to the corresponding LCD_* pins on the OMAP-L138 processor. The LCD_* function pins are multiplexed with other functions. These include VP_DOUT, UPP, MMCSD1, and GPIO. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.

Signal / Group	Type	Description
VP_*	I/O	Video Port In/Out. These pins are direct connects to the corresponding VP_* pins on the OMAP-L138 processor. The VP_* function pins are multiplexed with other functions. These include UPP, MMCSD1, and GPIO. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.
RESET_OUT	I/O	Reset Output pin. This pin is a direct connect to the RESET_OUT pin on the OMAP-L138 processor. This pin can also be configured as a GPIO. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.
USB0_*, USB1_*	I/O	Universal Serial Bus 0 / 1 pins. These pins are direct connects to the corresponding USB_* pins on the OMAP-L138 processor. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.

3 Electrical Requirements

The following sections describe the various electrical requirements for the MityDSP-L138, MitySOM-1808, MitySOM-1810 and MityDSP-6748 modules.

3.1 Power Supplies

The MityDSP-L138, MitySOM-1808, MitySOM-1810 and MityDSP-6748 module requires only one regulated power supply for the main +3.3V I/O power rail. All other required power rails are generated on-module by a combination of switching and linear, high-efficiency voltage regulators. The main +3.3V power rail can be sourced by either a linear or switching regulator as system requirements dictate. Table 3 describes the specifications of the input voltage, allowed ripple, and current requirements.

Table 3: Module Voltage and Current Specifications

Module	Spec.	Minimum	Typical	Maximum	Units
MityDSP-L138	$V_{3.3}$	3.14	3.3	3.46	V
	$I_{3.3}$	170	300	TBD	mA

3.2 Recommended Capacitance

All MityDSP-L138 family modules include some power supply rail bypass capacitors on-board, however additional capacitance is recommended on the carrier board to minimize the ripple effect caused by changing load currents. It is common practice to place one 10uF tantalum capacitor nearby each power supply pin pair. Please note that this is the minimum recommended amount of additional capacitance, and even more is always better.

3.3 I/O Interfaces

All I/O pins directly connected to the CPU SOC are compliant to only 3.3V I/O standards. The only exceptions to this are the SATA and USB data lines. These are I/Os directly connect to the OMAP-L138's built-in PHY transceivers, and as such are low voltage differential signaling standards.

The following sections describe I/O interfaces that are found on all MityDSP-L138, MitySOM-1808, and MityDSP-6748 types.

3.3.1 Module Reset

On the each module the main 3.3V input supply and all on-module generated power supplies are monitored and will trigger a module hard-reset if any of them fails or becomes unstable. Also included on this module is a manual-reset (MRESET#) input pin that can be connected to carrier board system reset and power supply monitoring circuitry.

3.3.2 Emulator/JTAG

All modules include connectivity for ARM/DSP emulation. There is a dedicated on-module Hirose header that is intended for use with a Critical Link supplied breakout cable/adaptor.

The ARM/DSP emulator connection is used for code download to RAM, and real-time debugging with TI's Code Composer Studio. All on-module signals are directly connected to the processor pins.

3.3.3 McASP Port

All modules include a Multi-Channel Audio Serial Port provided by the SOC. The McASP supports audio generation in Time Division Multiplexed (TDM) mode and Inter-IC Sound (I2S) format for as many as 16 stereo audio channels at standard professional audio sampling rates. The McASP signals are direct connects to the SOC and are configured for 3.3 V I/O logic. For more information, please consult the DSP device datasheets and McASP user guide documents provided by Texas Instruments. The McASP pins are shared with other peripherals on the SOC. Refer to the SOC datasheet for more details.

3.3.4 McBSP Ports

All modules include two Multi-channel Buffered Serial Ports provided by the SOC. These ports support a variety of synchronous serial communication protocols including TDM and SPI types. They can be used for connectivity to a wide array of data converters (DACs and ADCs), other DSPs, and other communications equipment. The signals are connected directly to the CPU SOC device pins and are configured for 3.3 V I/O logic. For more information, please consult the DSP device datasheets and McBSP user guide documents provided by Texas Instruments. The McBSP pins are shared with other peripherals on the SOC. Refer to the SOC datasheet for more details.

3.3.5 Serial UARTs

All modules include support for up to 3 UARTs directly connected to the processor. UART1 should be configured as a UART as that is the factory default console port used to support the bootloading application as well as the console for most higher level operating systems. The other UARTs may be configured per application needs. The UARTs share pins with other peripherals on the SOC processor. Refer to the SOC datasheet for more details.

3.3.6 Serial ATA (SATA)

The SOC device on the MityDSP-L138, MitySOM-1808, MitySOM-1810, and MityDSP-6748 includes a serial ATA bus controller. The bus controller lines have been routed to the edge connector for application use. For details, refer to the SOC datasheet.

3.3.7 SPI Ports

All modules include support for up to 2 SPI ports each having up to 8 chip selects directly controlled by the peripheral and may also use general GPIO pins as chip select pins if necessary. SPI1 chip select 0, however, is reserved in order to support booting from the on-board NOR flash. After bootloading, access to the NOR flash is typically not required, and the SPI port may be used with other chip selects if required. The SPI ports share pins with other peripherals on the SOC processor. Refer to the SOC datasheet for more details.

3.3.8 I2C Ports

All modules include support for up to 2 Inter-Integrated Circuit (I2C) ports. I2C0 is connected to an on-board prom (address 1010XXXb) that is used to hold factory configuration data (serial number, MAC address, etc.) and is therefore dedicated to this function. I2C0 is also connected to an on-board Power Management Integrated Circuit (PMIC), the TPS65023 (address 1001000b). Users may use the I2C0 port however, to interface to other devices having different addresses than those mentioned on this bus. The I2C ports share pins with other peripherals on the SOC processor. Refer to the SOC datasheet for more details.

3.3.9 10/100 Ethernet

Ethernet on the MityDSP-L138, MitySOM-1808, MitySOM-1810, or MityDSP-6748 is available as a MAC core in the CPU SOC. This Ethernet MAC is capable of full and half duplex 10/100 Mbit operation. To complete the interface, the MAC core requires a physical-layer device (PHY), an Ethernet isolation transformer (H1102 or equivalent), and an RJ-45 style connector (RJHSE-5381 or equivalent) on the carrier board. A connector with integrated magnetics and passives may also be used in place of discrete components.

All of the SOCs in this family of MityDSP (OMAP-L138, Sitara-1808, Sitara-1810, and DSP6748) provide support for both standard Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) formats. The MityDSP-L138 family of SOMs expose the RMII SOC interface directly to the edge connector. In general, designs requiring Ethernet should use the MII interface with MityDSP-L138 family SOMS. However, the RMII interface may still be used if the UPP and Video-Port-In functions are not needed.

The PHY IC's commonly used by Critical Link are the TI TLK100, and SMSC LAN87x0 family. It is also possible to connect the MAC core directly to an Ethernet Switch IC, such as the Micrel KS8995, via its standard Ethernet MII port. This option gives the carrier board the flexibility of easily making connections with several other Ethernet devices, without the need for additional networking equipment.

3.3.10 USB

The SOC provides two Universal Serial Bus (USB) interfaces that are mapped directly to the edge connector of the module. One port is capable of running as a host controller using USB 1.1 compliant protocols. The second port is capable of operating using the On-The-Go (OTG) protocol and is USB 2.0 compliant. OTG protocols support dynamic switching from host mode (e.g., for controlling USB mass storage devices such as thumb drives) to client mode (e.g., for interfacing to a PC) based on application software. For details in implementing the USB physical interface, refer to the TI SOC datasheets. The USB functions are not multiplexed with any other interfaces on the module.

3.3.11 EMIFA

All MityDSP-L138, MitySOM-1808, MitySOM-1810, and MityDSP-6748 modules expose the SOC's External Memory Interface-A (EMIFA) bus interface on the SO-DIMM edge connector. This memory interface bus is utilized on-module to support the NAND flash device on chip select 3 (CS3). The memory interface can be used externally to the module for connection to SDRAM, SRAM, flash memories (parallel NAND / NOR), FPGAs, and ASICs. Please refer to the SOC datasheets and user guides for more information on the operation of the EMIF bus.

3.3.12 UPP

All MityDSP-L138, MitySOM-1808, MitySOM-1810, and MityDSP-6748 modules expose the SOC's Universal Parallel Ports. These two ports each consist of a 8/16-bit wide data bus and synchronization and flow control signals. Each port can be configured as input or output, but they are not intended to be used in applications requiring a bi-directional data bus. Instead, one port can be configured as output, the other as input, and both can operate independently and simultaneously. The UPP ports are useful in moving data to/from CODECs (DACs/ADCx), FPGAs, ASICs, and other processors. Please refer to the SOC datasheets and user guides for more information on the operation of the UPP ports.

3.3.13 LCD Controller

All MityDSP-L138, MitySOM-1808, MitySOM-1810, and MityDSP-6748 modules expose the SOC's Liquid Crystal Display (LCD) Controller port. This port consists of a 16-bit data bus, and strobes and clocks necessary to connect to industry standard LCD module interfaces. The controller can operate in raster mode, or asynchronous memory-mapped mode (LIDD). Please refer to the SOC datasheets and user guides for more information on the operation of the LCD Controller.

3.3.14 Video Port Interface

All MityDSP-L138, MitySOM-1808, MitySOM-1810, and MityDSP-6748 modules expose the SOC's Video Port Interface (VPIF). This port consists of two separate data paths – one input and one output. Each is a 16-bit data bus with clock signals. The ports can be used to move TV/video data into and out of the SOC. The port pins are multiplexed with other functions such as the UPP, RMII, and MMCSD1. Please refer to the SOC datasheets and user guides for more information on the operation of the Video Port Interface.

4 Mechanical Requirements

The following sections describe some of the mechanical requirements of incorporating a MityDSP-L138, MitySOM-1808, MitySOM-1810, or MityDSP-6748 module in a board design.

4.1 Module Connectors

The module requires as its main interface the low-profile connector socket P/N 10116658-152FSLF from FCI, which is available from Digi-Key and other vendors. Sockets which are compatible with this industry standard DDR2 memory module socket are also available from other manufacturers and vendors.

The module may also be able to use a higher-profile connector socket that is mechanically compatible, but not necessarily footprint compatible with the connector mentioned above. Please contact Critical Link for a current list of compatible connector sockets for the module.

4.2 Module Clearance

All module types use a SO-DIMM style main interface connector for electrical and mechanical attachment to the carrier board. This style of connector positions the MityDSP module in parallel with the carrier board, and as such there is limited clearance between the MityDSP module and the carrier board. Therefore it is impossible to place high-profile carrier board components underneath the MityDSP module. However, it is possible to utilize most of this space for low-profile components. Please refer to the following diagrams and tables for module-specific clearances.

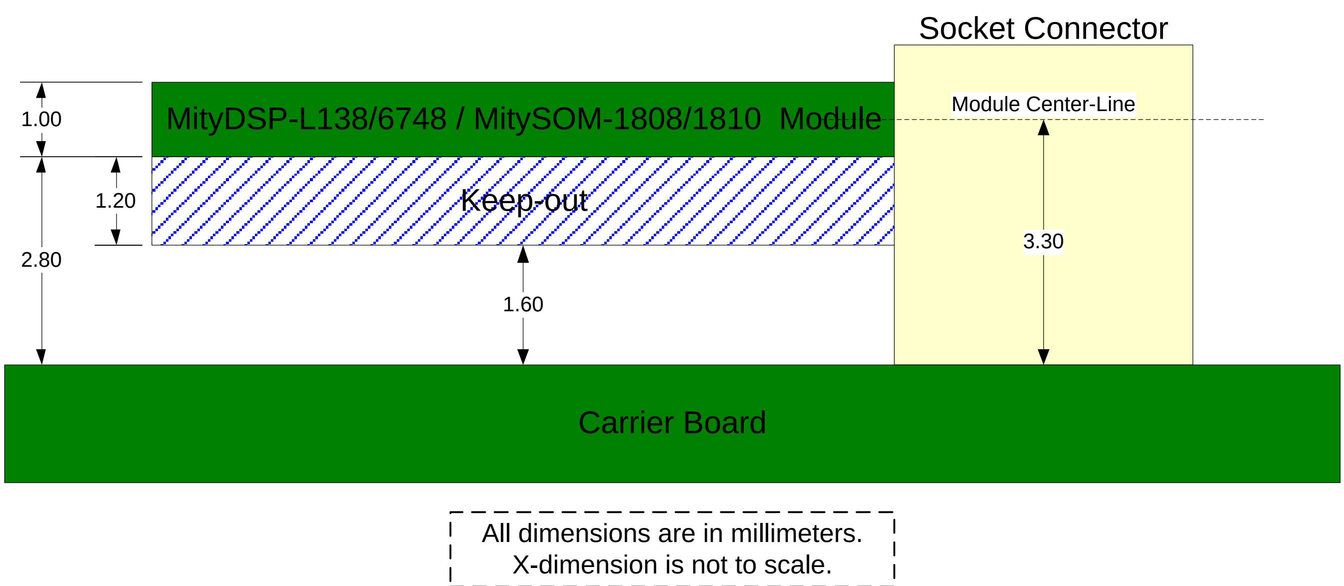

Figure 2: MityDSP-L138, MityDSP-6748, MitySOM-1808, MitySOM-1810 Module Clearance - Side View

4.3 Mounting Methods

The modules feature an additional optional mechanical attachment method. A hard mechanical attachment by board-to-board standoffs and screw hardware may be used to mount the module. The corners of the free-floating edge of the SOMs feature mounting holes that are compatible with 4-40 size mounting hardware. The mechanical drawing in Figure 1 below illustrates the mechanical requirements of this optional attachment method. Another option to secure the module is with the use of a screw, spacer and a self-clinching nut (PEM) that is inserted into the carrier board mounting holes, please contact Critical Link for details about utilizing this option.

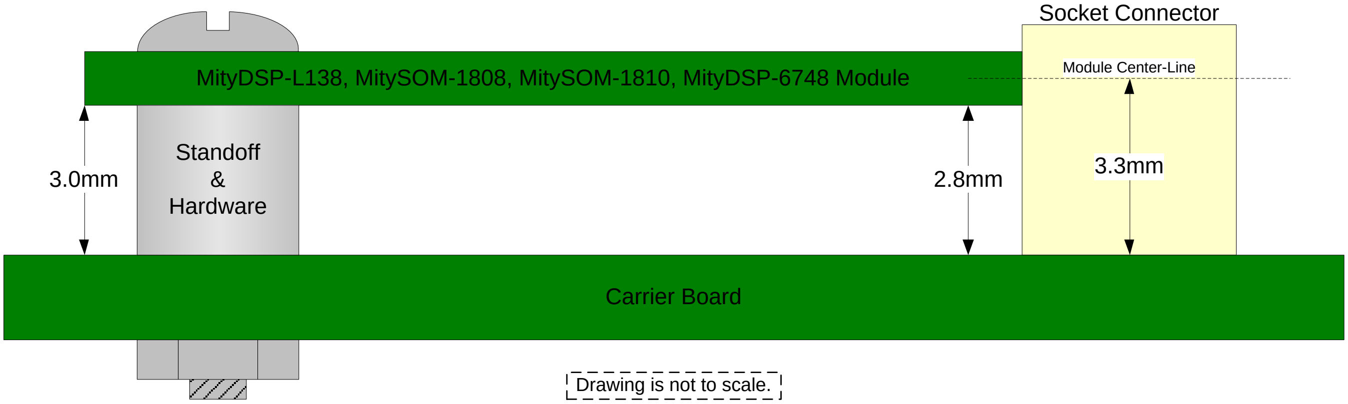

Figure 3: Standoff based Hold Down Concept Drawing

4.4 Shock & Vibration

For customers who are interested in using MityDSP modules in rugged environments, the optional mechanical attachment methods discussed in section 4.3 above enable MityDSP modules to tolerate much greater mechanical shock and vibration forces than without any additional mounting support.

4.5 Thermal Management

The MityDSP-L138 family of SOMs have no specific requirements regarding thermal management. The modules can be operated without heat sinks or air flow, and inside tight enclosures. However, if a module is intended to be used in hot industrial environments, it is advisable to do plenty of testing in the enclosure and environment that the module will be used in. In these cases, it may be necessary to either add thermal management to the enclosure, or lower the operating temperature specification of the end product.

5 Board Layout Recommendations

The following sections discuss topics for successful board layouts incorporating any module.

5.1 Placement

Placement of the module site is crucial to a successful carrier board layout. Because the module connector footprint is fine-pitch and dual-row, it is generally best to place the connector fairly centered in the overall board layout. This placement allows traces to be routed out from both sides of the connector, using mainly top-side copper tracks. The use of less signal layers, and therefore less vias, generally results in a more compact design with better signal integrity than a board using many layers and vias. Of course, ideally central placement is not always possible because of other mechanical constraints.

Mechanically, enough space must be allocated for the full extension of the module. Although it is possible for a module to hang over the edge of its carrier board, this may not be desirable if additional mechanical attachment methods are desired for ruggedness, as discussed in sections 4.3 and 4.4. Another thing to keep in mind with placement on the carrier board and in enclosures is the cam-in action of the MityDSP modules into their respective sockets. The modules are generally installed at an angle of about 25° to 30° before swinging down to locked position. Enclosure designs should accommodate this motion.

5.2 Pin-out and Routing

Care must be taken when routing the SOC high speed interfaces – specifically the USB 1.0 and 2.0 OTG ports and the SATA ports. Please refer to the specific SOC device specification for guidance related to these pins.

5.3 Access issues

Given that it is possible and often desirable to make best use of available space by placing components underneath the MityDSP module (refer to section 4.2), hardware and software engineers who will be debugging code on the platform could find themselves in a tough situation if the component they need to access is blocked by the installed MityDSP module. Because of these situations it is advisable to either not use the space under the MityDSP module for active components that might need live probing with the MityDSP in-circuit, or only place circuits there that are already tried and tested by engineers on other platforms. In the event that an obscured circuit does need to be probed, it may be necessary to solder temporary wires onto probe points. An even better solution would be to design the board with bottom-side test points, at least in the MityDSP region, if this is possible on a given design.

5.4 PCB/PCA Technology

MityDSP modules do not have any specific requirements about the PCB technology used for its carrier board. The required socket connectors are available as RoHS compliant, and may be used in both leaded and lead-free assembly processes. The only recommendation is to fabricate the carrier board thick enough to rigidly support the MityDSP socket connector. In practice, FR-4 with a common finished thickness of 0.062 inches is enough for all types of MityDSP modules.

5.5 PCB Footprints

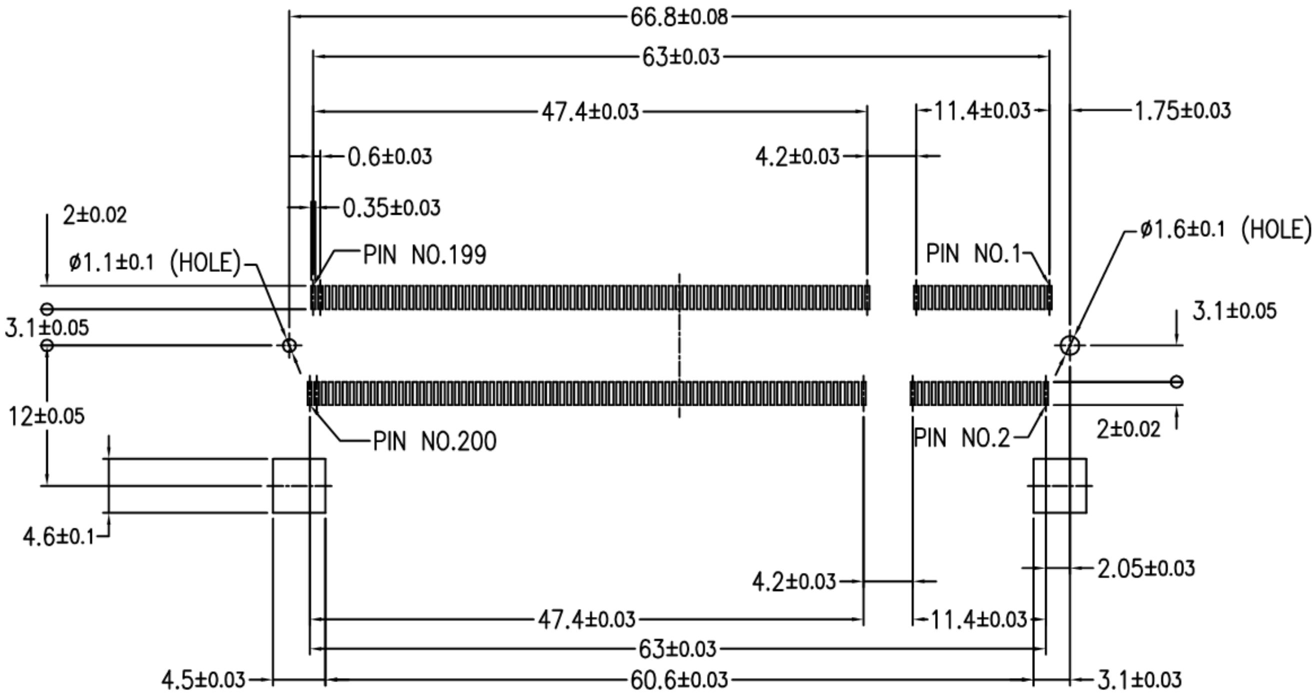

Figure 4: 10033853-152FSLF Recommended PCB Footprint

6 Revision History

Revision	Date	Description of Changes
1.0	11-September-2010	Initial Revision
1.1	11-November-2011	- Added Revision History - Added I2C address for PMIC
1.2	13-February-2012	Fix typo in signal names for pins 79, 81, and 83
1.3	13-February-2012	Fix typo in pinout table, pins 160, 170, and 180 were incorrectly numbered.
1.4	19-April-2012	Remove erroneous references to FPGA in the JTAG description.
1.5	13-August-2012	Fix typos in pinout table for pins 79, 81, 83, and 84
1.6	27-March-2013	Added processor ball numbers to the pin-out table and added 1810 to the datasheet.
1.7	5-March-2014	Update MitySOM product name.