FMS3810/3815

Triple Video D/A Converters

3 x 8 bit, 150 Ms/s

Features

- 8-bit resolution
- 150 megapixels per second
  - 0.2% linearity error
- Sync and blank controls
- 1.0V p-p video into 37.5Ω or 75Ω load
- Internal bandgap voltage reference
- Double-buffered data for low distortion
- TTL-compatible inputs
- Low glitch energy
- Single +5 Volt power supply

Applications

- Video signal conversion
  - RGB
  - YC_BC_R
  - Composite, Y, C
- Multimedia systems
- Image processing
- True-color graphics systems

Description

FMS3810/3815 products are low-cost triple D/A converters that are tailored to fit graphics and video applications where speed is critical. Two speed grades are available:

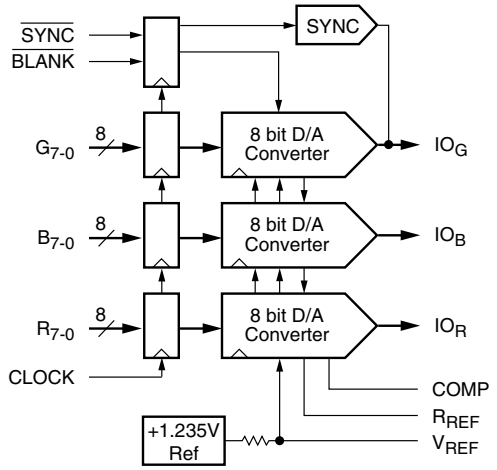
FMS3810	100 Ms/s
FMS3815	150 Ms/s

TTL-level inputs are converted to analog current outputs that can drive 25–37.5Ω loads corresponding to doubly-terminated 50–75Ω loads. A sync current following $\overline{SYNC}$ input timing is added to the I_{OG} output. $\overline{BLANK}$ will override RGB inputs, setting I_{OG}, I_{OB} and I_{OR} currents to zero when $\overline{BLANK}$ = L. Although appropriate for many applications the internal 1.235V reference voltage can be overridden by the V_{REF} input.

Few external components are required, just the current reference resistor, current output load resistors, and decoupling capacitors.

Package is a 48-lead LQFP. Fabrication technology is CMOS. Performance is guaranteed from 0 to 70°C.

Block Diagram



Functional Description

Within the FMS3810/3815 are three identical 10-bit D/A converters, each with a current source output. External loads are required to convert the current to voltage outputs. Data inputs RGB_{7-0} are overridden by the $\overline{BLANK}$ input. $\overline{SYNC}$ = H activates, sync current from I_{OS} for sync-on-green video signals.

Digital Inputs

All digital inputs are TTL-compatible. Data is registered on the rising edge of the CLK signal. Following one stage of pipeline delay, the analog output changes t_{DO} after the rising edge of CLK.

$\overline{SYNC}$ and $\overline{BLANK}$

$\overline{SYNC}$ and $\overline{BLANK}$ inputs control the output level (Figure 1 and Table 1) of the D/A converters during CRT retrace intervals. $\overline{BLANK}$ forces the D/A outputs to the blanking level while $\overline{SYNC}$ = L turns off a current source that is connected to the green D/A converter. $\overline{SYNC}$ = H adds a 40 IRE sync pulse to the green output, $\overline{SYNC}$ = L sets the green output to 0.0 Volts during the sync tip. $\overline{SYNC}$ and $\overline{BLANK}$ are registered on the rising edge of CLK.

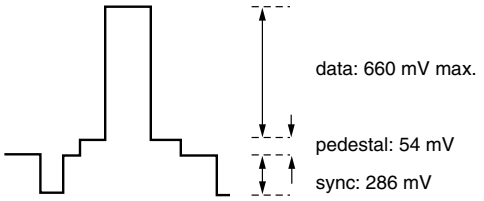


Figure 1. Nominal Output Levels

$\overline{BLANK}$ gates the D/A inputs and sets the pedestal voltage. If $\overline{BLANK}$ = H, the D/A inputs are added to a pedestal which offsets the current output. If $\overline{BLANK}$ = L, data inputs and the pedestal are disabled.

D/A Outputs

Each D/A output is a current source. To obtain a voltage output, a resistor must be connected to ground. Output voltage depends upon this external resistor, the reference voltage, and the value of the gain-setting resistor connected between R_{REF} and GND.

Normally, a source termination resistor of 75 Ohms is connected between the D/A current output pin and GND near the D/A converter. A 75 Ohm line may then be connected with another 75 Ohm termination resistor at the far end of the cable. This “double termination” presents the D/A converter with a net resistive load of 37.5 Ohms.

The FMS3810/3815 may also be operated with a single 75 Ohm terminating resistor. To lower the output voltage swing to the desired range, the nominal value of the resistor on R_{REF} should be doubled.

Voltage Reference

All three D/A converters are supplied with a common voltage reference. Internal bandgap voltage reference voltage is +1.235 Volts with a 3KΩ source resistance. An external voltage reference may be connected to the V_{REF} pin, overriding the internal voltage reference.

A 0.1μF capacitor must be connected between the COMP pin and V_{DD} to stabilize internal bias circuitry and ensure low-noise operation.

Power and Ground

Required power is a single +5.0 Volt supply. To minimize power supply induced noise, analog +5V should be connected to V_{DD} pins with 0.1 and 0.01 μF decoupling capacitors placed adjacent to each V_{DD} pin or pin pair.

High slew-rate of digital data makes capacitive coupling to the outputs of any D/A converter a potential problem. Since the digital signals contain high-frequency components of the CLK signal, as well as the video output signal, the resulting data feedthrough often looks like harmonic distortion or reduced signal-to-noise performance. All ground pins should be connected to a common solid ground plane for best performance.

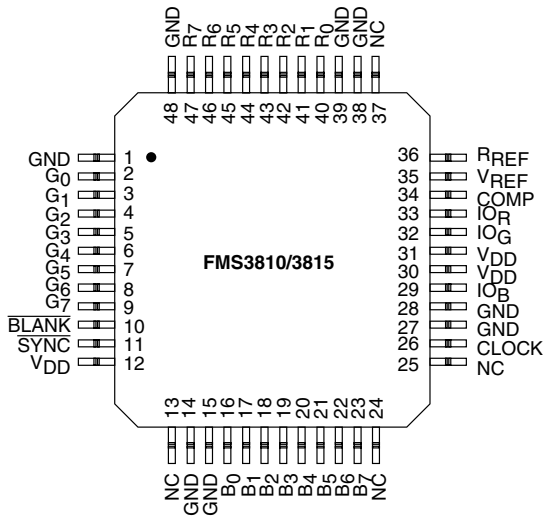
Table 1. Output Voltage versus Input Code, $\overline{SYNC}$ and $\overline{BLANK}$

V_{REF} = 1.235 V, R_{REF} = 590 Ω, R_L = 37.5 Ω

	Blue and Red			Green		
RGB7-0 (MSB…LSB)	$\overline{SYNC}$	$\overline{BLANK}$	V_{OUT}	$\overline{SYNC}$	$\overline{BLANK}$	V_{OUT}
1111 1111	X	1	0.714	1	1	1.000
1111 1111	X	1	0.714	0	1	0.714
1111 1110	X	1	0.711	1	1	0.997
1111 1101	X	1	0.709	1	1	0.995
• •	• •	• •	• •	• •	• •	• •
0000 0000	X	1	0.385	1	1	0.671
1111 1111	X	1	0.383	1	1	0.669
• •	• •	• •	• •	• •	• •	• •
0000 0010	X	1	0.059	1	1	0.345
0000 0001	X	1	0.057	1	1	0.343
0000 0000	X	1	0.054	1	1	0.340
0000 0000	X	1	0.054	0	1	0.054
XXXX XXXX	X	0	0.000	1	0	0.286
XXXX XXXX	X	0	0.000	0	0	0.000
XXXX XXXX	X	1	valid	0	1	valid

Pin Assignments

LQFP Package



Pin Descriptions

Pin Name	Pin Number LQFP	Value	Pin Function Description
Clock and Pixel I/O			
CLK	26	TTL	**Clock Input.** The clock input is TTL-compatible and all pixel data is registered on the rising edge of CLK. It is recommended that CLK be driven by a dedicated TTL buffer to avoid reflection induced jitter, overshoot, and undershoot.
R_{7-0} G_{7-0} B_{7-0}	47-40 9-2 23-16	TTL	**Red, Green, and Blue Pixel Inputs.** TTL-compatible RGB digital inputs are registered on the rising edge of CLK.
Controls			
$\overline{SYNC}$	11	TTL	**Sync Pulse Input.** Bringing $\overline{SYNC}$ LOW, turns off a 40 IRE (7.62 mA) current source which forms a sync pulse on any D/A converter output connected to IO_S. $\overline{SYNC}$ is registered on the rising edge of CLK along with pixel data and has the same pipeline latency as $\overline{BLANK}$ and pixel data. $\overline{SYNC}$ does not override any other data and should be used only during the blanking interval. If the system does not require sync pulses, $\overline{SYNC}$ and IO_S should be connected to GND.
$\overline{BLANK}$	10	TTL	**Blanking Input.** When $\overline{BLANK}$ is LOW, pixel inputs are ignored and the D/A converter outputs are driven to the blanking level. $\overline{BLANK}$ is registered on the rising edge of CLK and has the same two-pipe latency as $\overline{SYNC}$ and Data.
Video Outputs			
IO_R IO_G IO_B	33 32 29	0.714 V_{p-p}	**Red, Green, and Blue Current Outputs.** Current source outputs can drive RS-343A/SMPTE-170M compatible levels into doubly-terminated 75 Ohm lines. Sync pulses may be added to the green output. When $\overline{SYNC}$ is HIGH, the current added to I_{OG} is: $IO_S = 3.64 (V_{REF} / R_{REF})$
Voltage Reference			
V_{REF}	35	+1.235 V	**Voltage Reference Input/Output.** Internal 1.235V voltage reference is available on this pin. An external +1.235 Volt reference may be applied to this pin to override the internal reference. Decoupling V_{REF} to GND with a 0.1µF ceramic capacitor is required.
R_{REF}	36	590 Ω	**Current-setting Resistor.** Full-scale output current of each D/A converter is determined by the value of the resistor connected between R_{REF} and GND. Nominal value of R_{REF} is found from: $R_{REF} = 9.1 (V_{REF}/I_{FS})$ where I_{FS} is the full-scale (white) output current (amps) from the D/A converter (without sync). Sync is 0.4 I_{FS}. D/A full-scale (white) current may also be calculated from: $I_{FS} = V_{FS}/R_L$ Where V_{FS} is the white voltage level and R_L is the total resistive load (ohms) on each D/A converter. V_{FS} is the blank to full-scale voltage.
COMP	34	0.1 µF	**Compensation Capacitor.** A 0.1 µF ceramic capacitor should be connected between COMP and V_{DD} to stabilize internal bias circuitry.

Pin Descriptions (continued)

Pin Name	Pin Number LQFP	Value	Pin Function Description
Power, Ground			
V_{DD}	12, 30, 31	+5 V	**Power Supply.**
GND	1, 14, 15, 27, 28, 38, 39, 48	0.0V	**Ground.**
NC	13, 24, 25, 37	—	**No Connect**

Equivalent Circuits

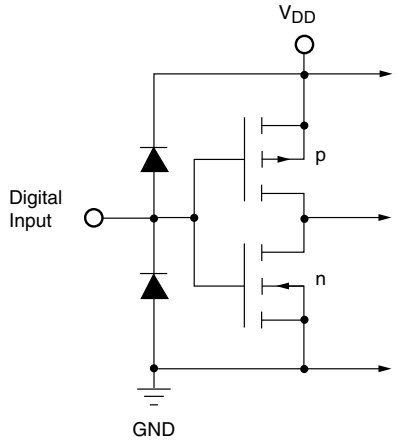


Figure 1. Equivalent Digital Input Circuit

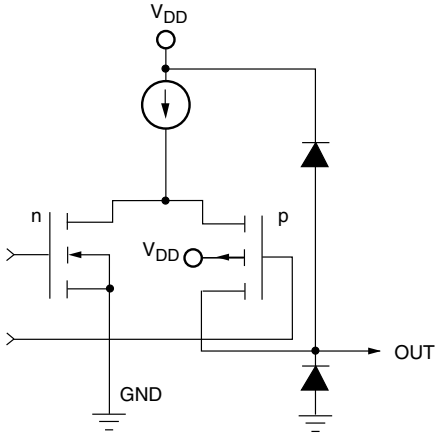


Figure 2. Equivalent Analog Output Circuit

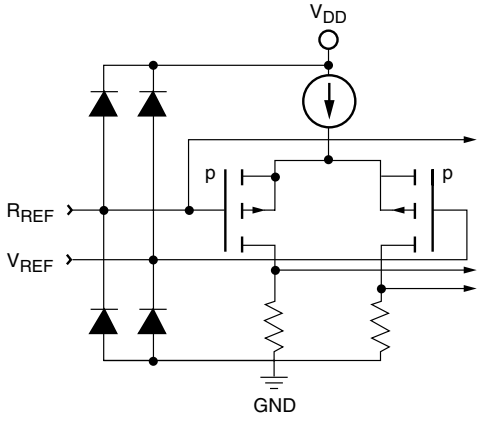


Figure 3. Equivalent Analog Input Circuit

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltage				
V_{DD} (Measured to GND)	-0.5		7.0	V
Inputs				
Applied Voltage (measured to GND)[2]	-0.5		V_{DD} + 0.5	V
Forced Current[3,4]	-10.0		10.0	mA
Outputs				
Applied Voltage (measured to GND)[2]	-0.5		V_{DD} + 0.5	V
Forced Current[3,4]	-60.0		60.0	mA
Short Circuit Duration (single output in HIGH state to ground)			unlimited	sec.
Temperature				
Operating, Ambient	-20		110	°C
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C
Storage	-65		150	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_S	Conversion Rate	FMS3810			100	Msps
		FMS3815			150	Msps
t_{PWH}	CLK Pulsewidth, HIGH	FMS3810	3.1			ns
		FMS3815	2.5			ns
t_{PWL}	CLK Pulsewidth, LOW	FMS3810	3.1			ns
		FMS3815	2.5			ns
t_W	CLK Pulsewidth	FMS3810	10			ns
		FMS3815	6.6			ns
t_s	Input Data Setup Time		1.7			ns
t_h	Input Date Hold Time		0			ns
V_{REF}	Reference Voltage, External		1.0	1.235	1.5	V
C_C	Compensation Capacitor			0.1		µF
R_L	Output Load			37.5		Ω
V_{IH}	Input Voltage, Logic HIGH		2.0		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW		GND		0.8	V
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions[3]	Min	Typ[1]	Max	Units
I_{DD}	Power Supply Current[2]	V_{DD} = Max			125	mA
PD	Total Power Dissipation[2]	V_{DD} = Max			655	mW
R_O	Output Resistance			100		kΩ
C_O	Output Capacitance	I_{OUT} = 0mA			30	pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = 2.4V			-5	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0.4V			5	µA
I_{REF}	V_{REF} Input Bias Current			0	±100	µA
V_{REF}	Reference Voltage Output			1.235		V
V_{OC}	Output Compliance	Referred to V_{DD}	-0.4	0	+1.5	V
C_{DI}	Digital Input Capacitance			4	10	pF

Notes:
1. Values shown in Typ column are typical for V_{DD} = +5V and T_A = 25°C
2. Minimum/Maximum values with V_{DD} = Max and T_A = Min
3. V_{REF} = 1.235V, R_{LOAD} = 37.5Ω, R_{REF} = 590Ω

Switching Characteristics

Parameter		Conditions[2]	Min	Typ[1]	Max	Units
t_D	Clock to Output Delay	V_{DD} = Min		10	15	ns
t_{SKEW}	Output Skew			1	2	ns
t_R	Output Risetime	10% to 90% of Full Scale			3	ns
t_F	Output Falltime	90% to 10% of Full Scale			3	ns

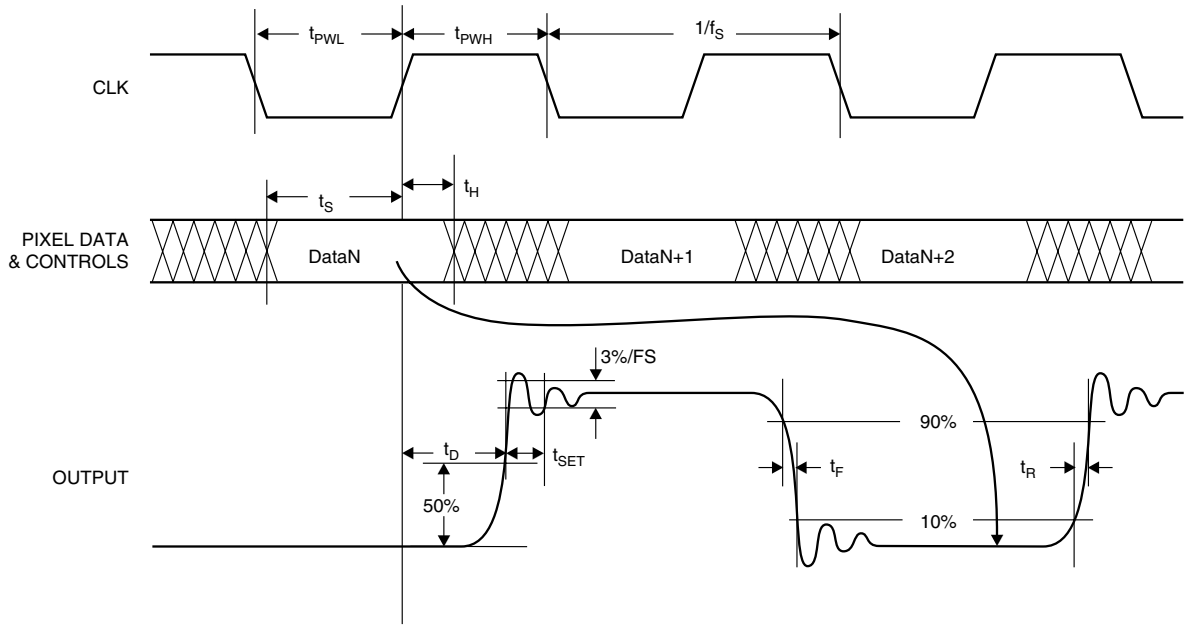
Notes:
1. Values shown in Typ column are typical for V_{DD} = +5V and T_A = 25°C.
2. V_{REF} = 1.235V, R_{LOAD} = 37.5Ω, R_{REF} = 590Ω.

System Performance Characteristics

Parameter		Conditions[2]	Min	Typ[1]	Max	Units
E_{LI}	Integral Linearity Error	V_{DD}, V_{REF} = Nom		±0.2	±0.3	%/FS
E_{LD}	Differential Linearity Error	V_{DD}, V_{REF} = Nom		±0.2	±0.3	%/FS
E_{DM}	DAC to DAC Matching	V_{DD}, V_{REF} = Nom		5	10	%
PSRR	Power Supply Rejection Ratio				0.05	%/%

Notes:
1. Values shown in Typ column are typical for V_{DD} = +5V and T_A = 25°C.
2. V_{REF} = 1.235V, R_{LOAD} = 37.5Ω, R_{REF} = 590Ω.

Timing Diagram



Applications Information

Figure 4 illustrates a typical FMS3810/3815 interface circuit. In this example, an optional 1.2 Volt bandgap reference is connected to the V_{REF} output, overriding the internal voltage reference source.

Grounding

It is important that the FMS3810/3815 power supply is well-regulated and free of high-frequency noise. Careful power supply decoupling will ensure the highest quality video signals at the output of the circuit. The FMS3810/3815 has separate analog and digital circuits. To keep digital system noise from the D/A converter, it is recommended that power supply voltages (V_{DD}) come from the system analog power source and all ground connections (GND) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor D/A conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{REF}, I_{REF}, COMP, IO_S, IO_R, IO_G) as short as possible and as far as possible from all digital signals. The FMS3810/3815 should be located near the board edge, close to the analog output connectors.

2. The power plane for the FMS3810/3815 should be separate from that which supplies the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the FMS3810/3815 is the same as that of the system's digital circuitry, power to the FMS3810/3815 should be decoupled with 0.1μF and 0.01μF capacitors and isolated with a ferrite bead.

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. If the digital power supply has a dedicated power plane layer, it should not be placed under the FMS3810/3815, the voltage reference, or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the FMS3810/3815 and its related analog circuitry can have an adverse effect on performance.

5. CLK should be handled carefully. Jitter and noise on this clock will degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

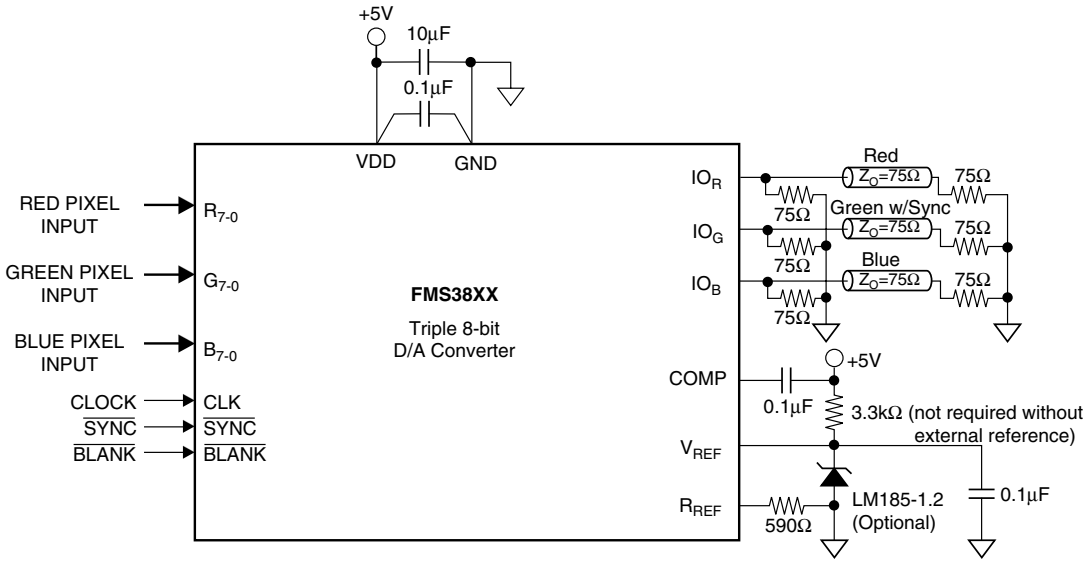


Figure 4. Typical Interface Circuit

Related Products

- FMS3110/3115 Triple 10-bit 250 Msps D/A Converters
- FMS9884A 3 x 8 bit 140 Ms/s A/D Converter

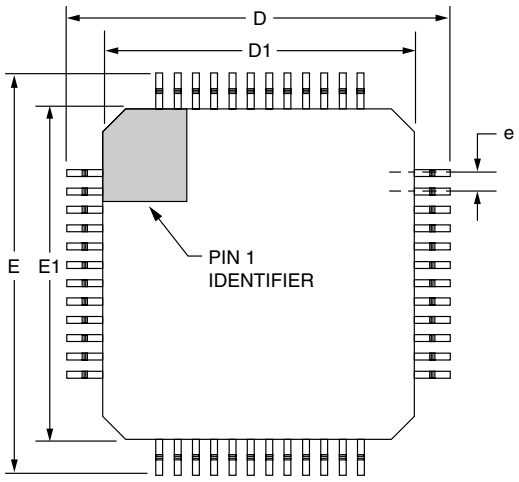
Mechanical Dimensions

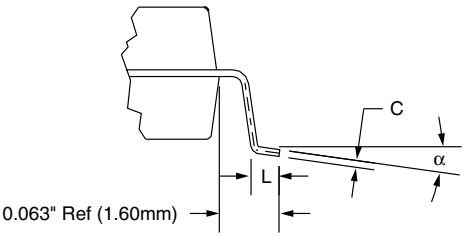
48-Lead LQFP Package

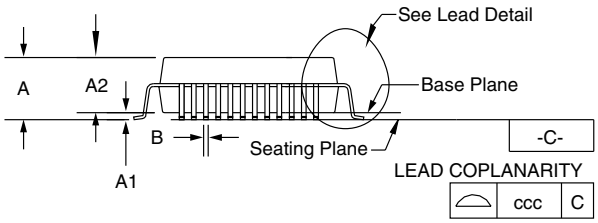
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.055	.063	1.40	1.60	
A1	.001	.005	.05	.15	
A2	.053	.057	1.35	1.45	
B	.006	.010	.17	.27	7
D/E	.346	.362	8.8	9.2	8
D1/E1	.268	.284	6.8	7.2	2
e	.019 BSC		.50 BSC		
L	.017	.029	.45	.75	6
N	48		48		4
ND	12		12		5
α	0°	7°	0°	7°	
ccc	.004		0.08		

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Pin 1 identifier is optional.
4. Dimension ND: Number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum B dimension by more than 0.08mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
8. To be determined at seating place —C—







Ordering Information

Product Number	Conversion Rate	Temperature Range	Screening	Package	Package Marking
FMS3810KRC	100 Ms/s	T_A = 0°C to 70°C	Commercial	48-Lead LQFP	3810KRC
FMS3815KRC	150 Ms/s	T_A = 0°C to 70°C	Commercial	48-Lead LQFP	3815KRC