

74HC166; 74HCT166

8-bit parallel-in/serial out shift register

Rev. 3 — 11 September 2013

Product data sheet

1. General description

The 74HC166; 74HCT166 is an 8-bit serial or parallel-in/serial-out shift register. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and a serial output (Q7). When the parallel enable input (\overline{PE}) is LOW, the data from D0 to D7 is loaded into the shift register on the next LOW-to-HIGH transition of the clock input (CP). When \overline{PE} is HIGH, data enters the register serially at DS with each LOW-to-HIGH transition of CP. When the clock enable input (\overline{CE}) is LOW data is shifted on the LOW-to-HIGH transitions of CP. A HIGH on \overline{CE} disables the CP input. Inputs include clamp diodes which enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Synchronous parallel-to-serial applications
- Synchronous serial input for easy expansion
- Complies with JEDEC standard no. 7A
- Input levels:
 - ◆ For 74HC166: CMOS level
 - ◆ For 74HCT166: TTL level
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

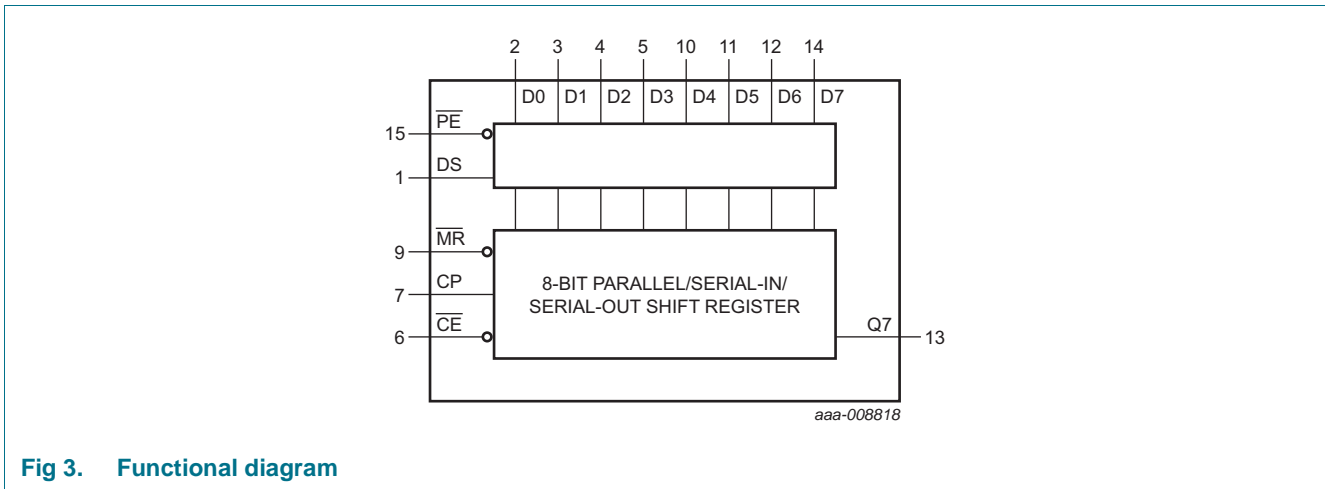
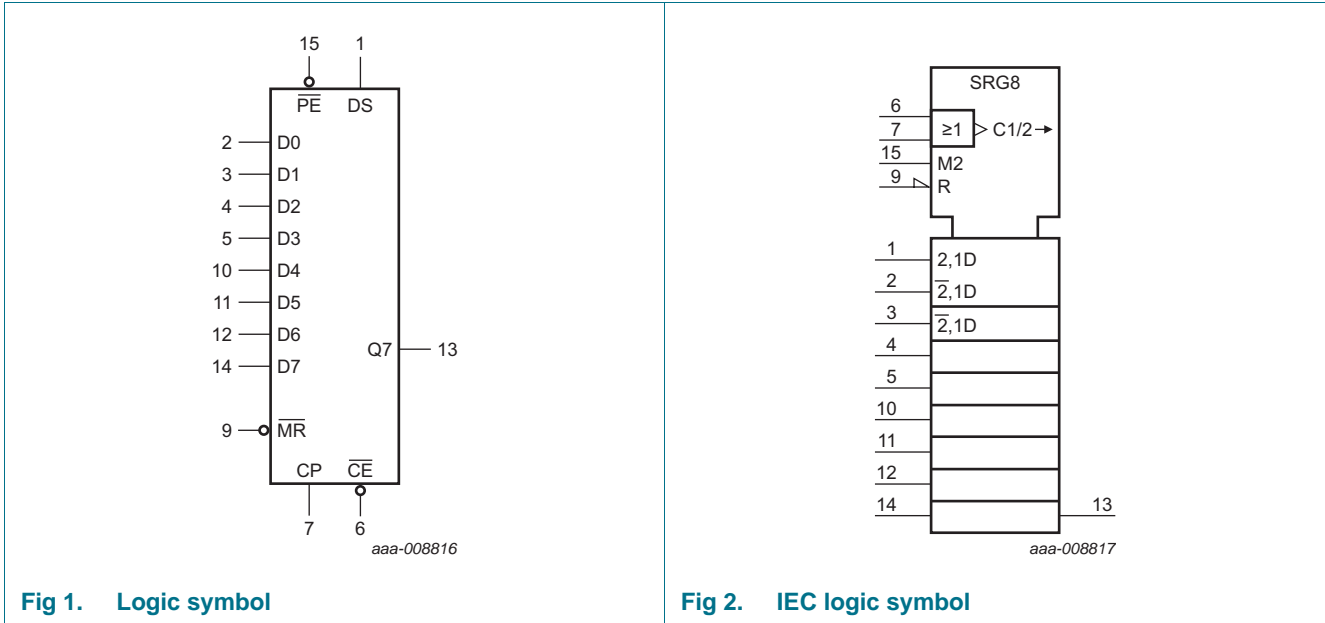
3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|---|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74HC166N | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74HCT166N | | | | |
| 74HC166D | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HCT166D | | | | |
| 74HC166DB | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HCT166DB | | | | |
| 74HC166PW | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |



4. Functional diagram



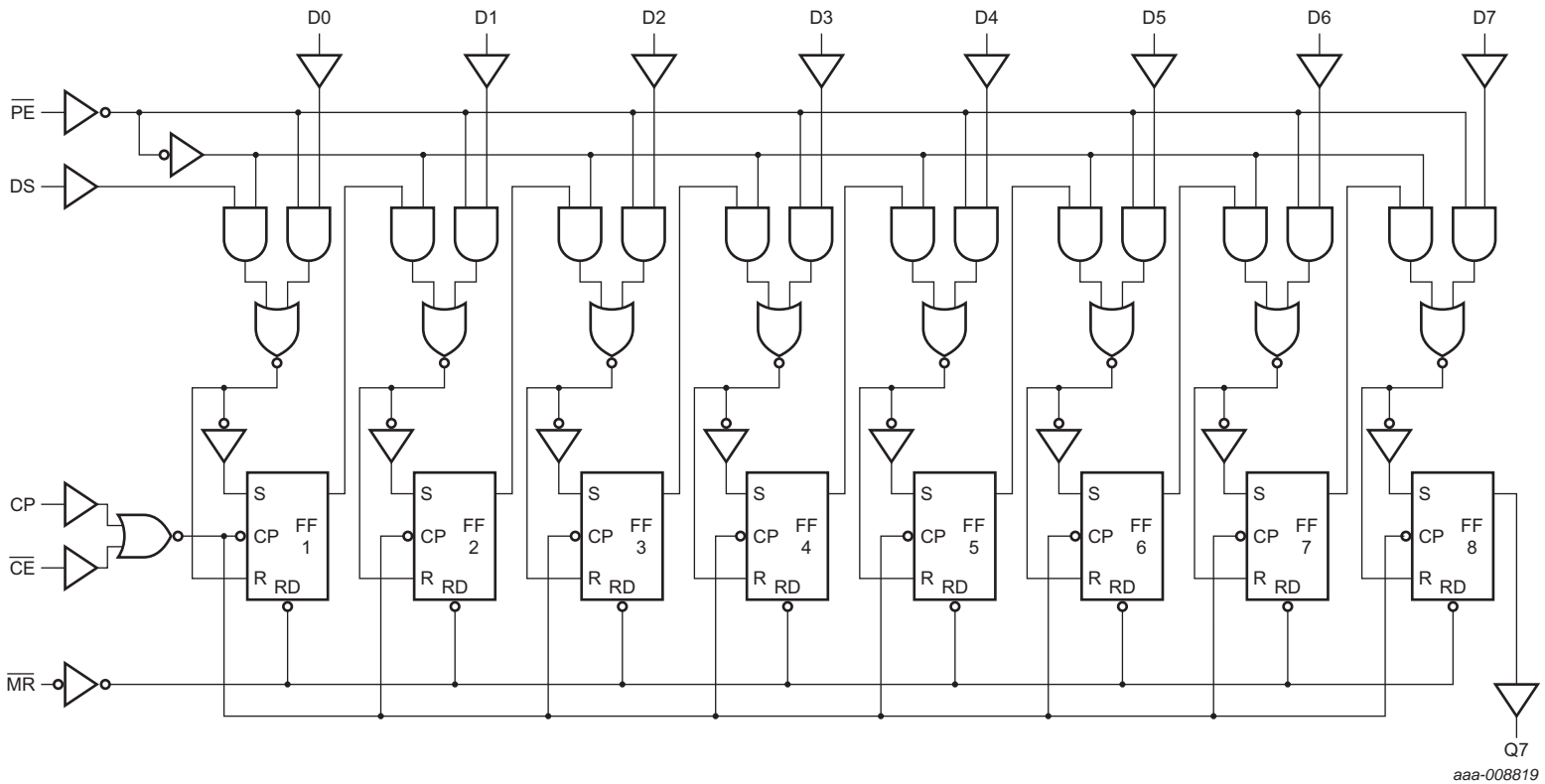


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

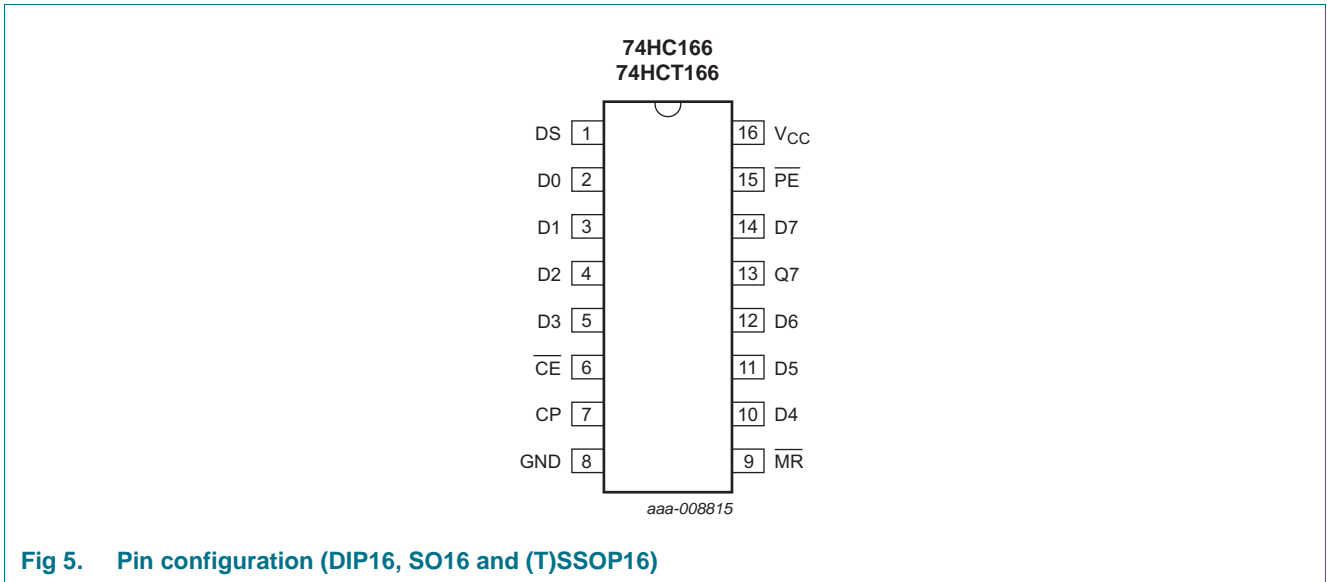


Fig 5. Pin configuration (DIP16, SO16 and (T)SSOP16)

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|------------------------|----------------------------|--|
| DS | 1 | serial data input |
| D0 to D7 | 2, 3, 4, 5, 10, 11, 12, 14 | parallel data inputs |
| $\overline{\text{CE}}$ | 6 | clock enable input (active LOW) |
| CP | 7 | clock input (LOW-to-HIGH edge-triggered) |
| GND | 8 | ground (0 V) |
| $\overline{\text{MR}}$ | 9 | asynchronous master reset (active LOW) |
| Q7 | 13 | serial output from the last stage |
| $\overline{\text{PE}}$ | 15 | parallel enable input (active LOW) |
| V _{CC} | 16 | positive supply voltage |

6. Functional description

Table 3. Function table^[1]

| Operating modes | Inputs | | | | | Qn registers | | Output |
|-------------------|-----------------|-----------------|----|----|----------|--------------|----------|--------|
| | \overline{PE} | \overline{CE} | CP | DS | D0 to D7 | Q0 | Q1 to Q6 | Q7 |
| parallel load | L | L | ↑ | X | L | L | L to L | L |
| | h | L | ↑ | X | h | H | H to H | H |
| serial shift | h | L | ↑ | L | X | L | q0 to q5 | q6 |
| | h | L | ↑ | h | X | H | q0 to q5 | q6 |
| hold "do nothing" | X | H | X | X | X | q0 | q1 to q6 | q7 |

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
 X = don't care;
 ↑ = LOW-to-HIGH clock transition.

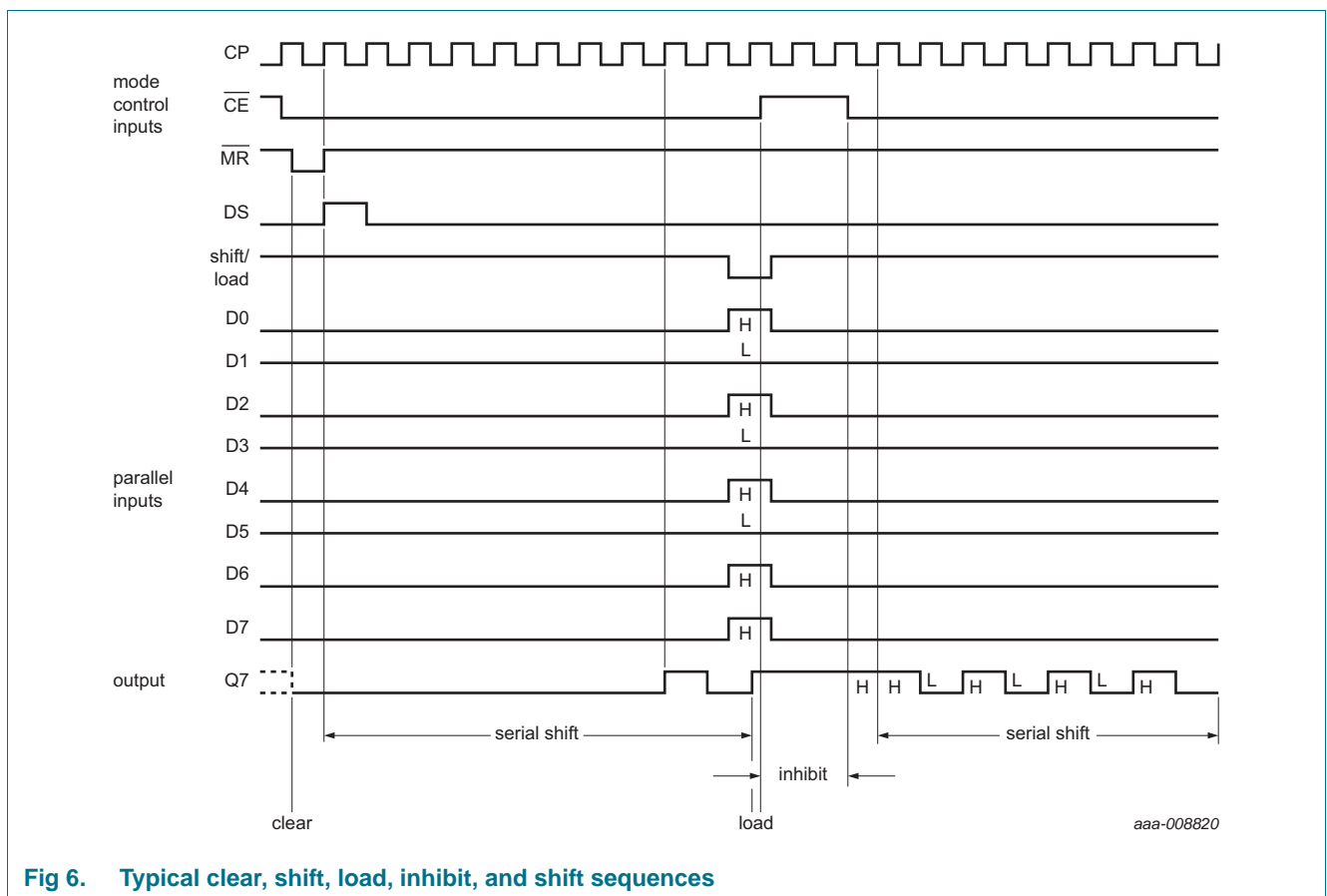


Fig 6. Typical clear, shift, load, inhibit, and shift sequences

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|-------|----------|------|
| V_{CC} | supply voltage | | -0.5 | +7 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | [1] - | ± 20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | [1] - | ± 20 | mA |
| I_O | output current | $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ | - | ± 25 | mA |
| I_{CC} | supply current | | - | 50 | mA |
| I_{GND} | ground current | | -50 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ | | | |
| | | DIP16 package | [2] - | 750 | mW |
| | | SO16 package | [3] - | 500 | mW |
| | | (T)SSOP16 package | [4] - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC166 | | | 74HCT166 | | | Unit |
|------------------|-------------------------------------|-------------------------|---------|------|-----------------|----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | - | +125 | -40 | - | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC166 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| | | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|---|-------|------|------|------------------|-------|-------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| 74HCT166 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 5.2 mA; V _{CC} = 4.5 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 4.5 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | Dn and DS inputs | - | 35 | 126 | - | 157.5 | - | 171.5 | μA |
| | | CP and \overline{CE} inputs | - | 80 | 288 | - | 360 | - | 392 | μA |
| | | \overline{MR} input | - | 40 | 144 | - | 180 | - | 196 | μA |
| | | \overline{PE} input | - | 60 | 216 | - | 270 | - | 294 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); $t_r = t_f = 6$ ns; $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 10](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------------|-------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC166 | | | | | | | | | | |
| t_{pd} | propagation delay | CP to Q7; see Figure 7 ^[1] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 50 | 150 | - | 190 | - | 225 | ns |
| | | $V_{CC} = 4.5$ V | - | 18 | 30 | - | 38 | - | 45 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 15 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0$ V | - | 14 | 26 | - | 33 | - | 38 | ns |
| | | MR to Q7; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 47 | 160 | - | 200 | - | 240 | ns |
| | | $V_{CC} = 4.5$ V | - | 17 | 32 | - | 40 | - | 48 | ns |
| t_t | transition time | output; see Figure 7 ^[2] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | $V_{CC} = 4.5$ V | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC} = 6.0$ V | - | 6 | 13 | - | 16 | - | 19 | ns |
| t_{pw} | pulse width | CP input HIGH or LOW; see Figure 7 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 80 | 17 | - | 100 | - | 120 | - | ns |
| | | $V_{CC} = 4.5$ V | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | $V_{CC} = 6.0$ V | 14 | 5 | - | 17 | - | 20 | - | ns |
| | | MR input LOW; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 100 | 25 | - | 125 | - | 150 | - | ns |
| | | $V_{CC} = 4.5$ V | 20 | 9 | - | 25 | - | 30 | - | ns |
| | | $V_{CC} = 6.0$ V | 17 | 7 | - | 21 | - | 26 | - | ns |
| t_{rec} | recovery time | MR to CP; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 0 | -19 | - | 0 | - | 0 | - | ns |
| | | $V_{CC} = 4.5$ V | 0 | -7 | - | 0 | - | 0 | - | ns |
| | | $V_{CC} = 6.0$ V | 0 | -6 | - | 0 | - | 0 | - | ns |
| t_{su} | set-up time | Dn, \overline{CE} to CP; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 80 | 14 | - | 100 | - | 120 | - | ns |
| | | $V_{CC} = 4.5$ V | 16 | 5 | - | 20 | - | 24 | - | ns |
| | | $V_{CC} = 6.0$ V | 14 | 4 | - | 17 | - | 20 | - | ns |
| | | \overline{PE} to CP; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 100 | 33 | - | 125 | - | 150 | - | ns |
| | | $V_{CC} = 4.5$ V | 20 | 12 | - | 25 | - | 30 | - | ns |
| | | $V_{CC} = 6.0$ V | 17 | 10 | - | 21 | - | 26 | - | ns |

Table 7. Dynamic characteristics ...continued

GND (ground = 0 V); $t_r = t_f = 6$ ns; $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 10](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit | |
|-----------|-------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|--|
| | | | Min | Typ | Max | Min | Max | Min | Max | | |
| t_h | hold time | Dn, \overline{CE} to CP; see Figure 9 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 2 | -8 | - | 2 | - | 2 | - | ns | |
| | | $V_{CC} = 4.5$ V | 2 | -3 | - | 2 | - | 2 | - | ns | |
| | | $V_{CC} = 6.0$ V | 2 | -2 | - | 2 | - | 2 | - | ns | |
| | | \overline{PE} to CP; see Figure 9 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 0 | -28 | - | 0 | - | 0 | - | ns | |
| | | $V_{CC} = 4.5$ V | 0 | -10 | - | 0 | - | 0 | - | ns | |
| f_{max} | maximum frequency | CP input; see Figure 7 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 6 | 19 | - | 4.8 | - | 4 | - | MHz | |
| | | $V_{CC} = 4.5$ V | 30 | 57 | - | 24 | - | 20 | - | MHz | |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 63 | - | - | - | - | - | MHz | |
| C_{PD} | power dissipation capacitance | $V_{CC} = 6.0$ V | 35 | 68 | - | 28 | - | 24 | - | MHz | |
| | | per package; $V_I = GND$ to V_{CC} | [3] | - | 41 | - | - | - | - | pF | |

74HCT166

| | | | | | | | | | | | |
|-----------|-------------------|---|-----|-----|----|----|----|----|----|----|--|
| t_{pd} | propagation delay | CP to Q7; see Figure 7 | [1] | | | | | | | | |
| | | $V_{CC} = 4.5$ V | - | 23 | 40 | - | 50 | - | 60 | ns | |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 20 | - | - | - | - | - | ns | |
| | | \overline{MR} to Q7; see Figure 8 | | | | | | | | | |
| | | $V_{CC} = 4.5$ V | - | 22 | 40 | - | 50 | - | 60 | ns | |
| t_t | transition time | output; see Figure 7 | [2] | | | | | | | | |
| | | $V_{CC} = 4.5$ V | - | 7 | 15 | - | 19 | - | 22 | ns | |
| t_W | pulse width | CP input HIGH or LOW; see Figure 7 | | | | | | | | | |
| | | $V_{CC} = 4.5$ V | 20 | 9 | - | 25 | - | 30 | - | ns | |
| | | \overline{MR} input LOW; see Figure 8 | | | | | | | | | |
| t_{rec} | recovery time | $V_{CC} = 4.5$ V | 25 | 11 | - | 31 | - | 38 | - | ns | |
| | | \overline{MR} to CP; see Figure 8 | | | | | | | | | |
| t_{su} | set-up time | $V_{CC} = 4.5$ V | 0 | -7 | - | 0 | - | 0 | - | ns | |
| | | Dn, \overline{CE} to CP; see Figure 9 | | | | | | | | | |
| t_h | hold time | $V_{CC} = 4.5$ V | 16 | 8 | - | 20 | - | 24 | - | ns | |
| | | \overline{PE} to CP; see Figure 9 | | | | | | | | | |
| | | $V_{CC} = 4.5$ V | 30 | 15 | - | 38 | - | 45 | - | ns | |
| t_h | hold time | Dn, \overline{CE} to CP; see Figure 9 | | | | | | | | | |
| | | $V_{CC} = 4.5$ V | 0 | -3 | - | 0 | - | 0 | - | ns | |
| t_h | hold time | \overline{PE} to CP; see Figure 9 | | | | | | | | | |
| | | $V_{CC} = 4.5$ V | 0 | -13 | - | 0 | - | 0 | - | ns | |

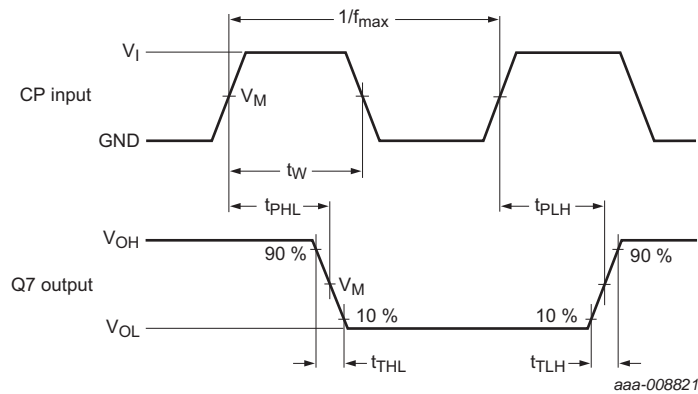
Table 7. Dynamic characteristics ...continued

GND (ground = 0 V); $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit, see [Figure 10](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| f_{max} | maximum frequency | CP input; see Figure 7 | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 25 | 45 | - | 20 | - | 17 | - | MHz |
| | | $V_{\text{CC}} = 5.0 \text{ V}$; $C_L = 15 \text{ pF}$ | - | 50 | - | - | - | - | - | MHz |
| C_{PD} | power dissipation capacitance | per package; $V_1 = \text{GND to } V_{\text{CC}}$ | [3] | - | 41 | - | - | - | - | pF |

- [1] t_{pd} is the same as t_{PHL} and t_{PLH} .
- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i + \Sigma (C_L \times V_{\text{CC}}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 $\Sigma (C_L \times V_{\text{CC}}^2 \times f_o)$ = sum of outputs;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V.

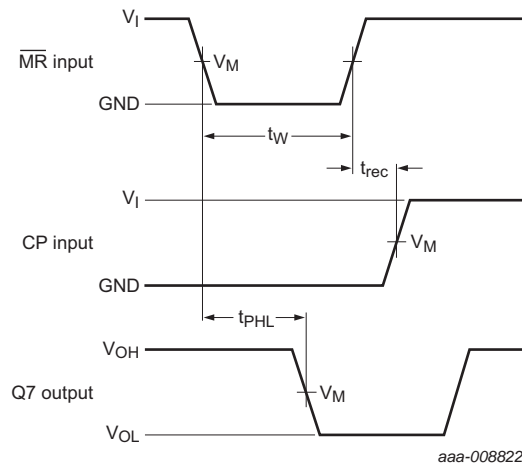
11. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

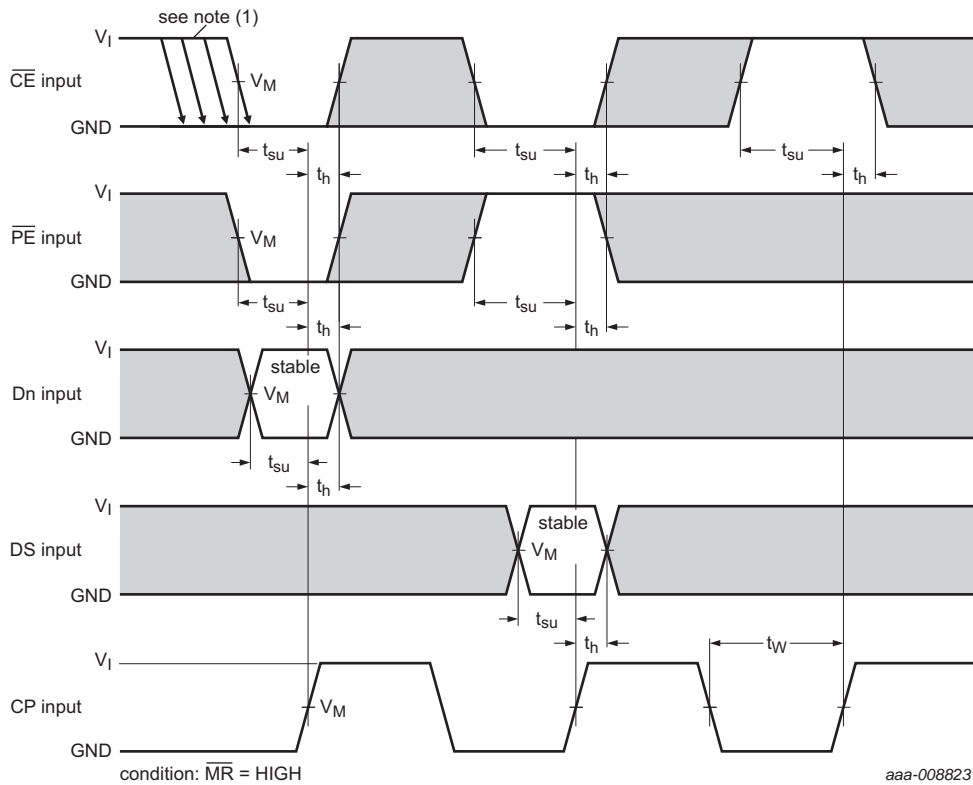
Fig 7. Clock (CP) to output (Q7) propagation delays, pulse width, output transition times and maximum frequency



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Master reset (MR) pulse width, MR to output (Q7) propagation delay and MR to clock (CP) recovery time.



The shaded areas indicate when the input is permitted to change for predictable output performance

Measurement points are given in [Table 8](#).

(1) \overline{CE} may change only from HIGH-to-LOW while CP is LOW

Fig 9. Set-up and hold times

Table 8. Measurement points

| Type | Input | | Output |
|----------|----------|-------------|-------------|
| | V_I | V_M | V_M |
| 74HC166 | V_{CC} | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT166 | 3 V | 1.3 V | 1.3 V |

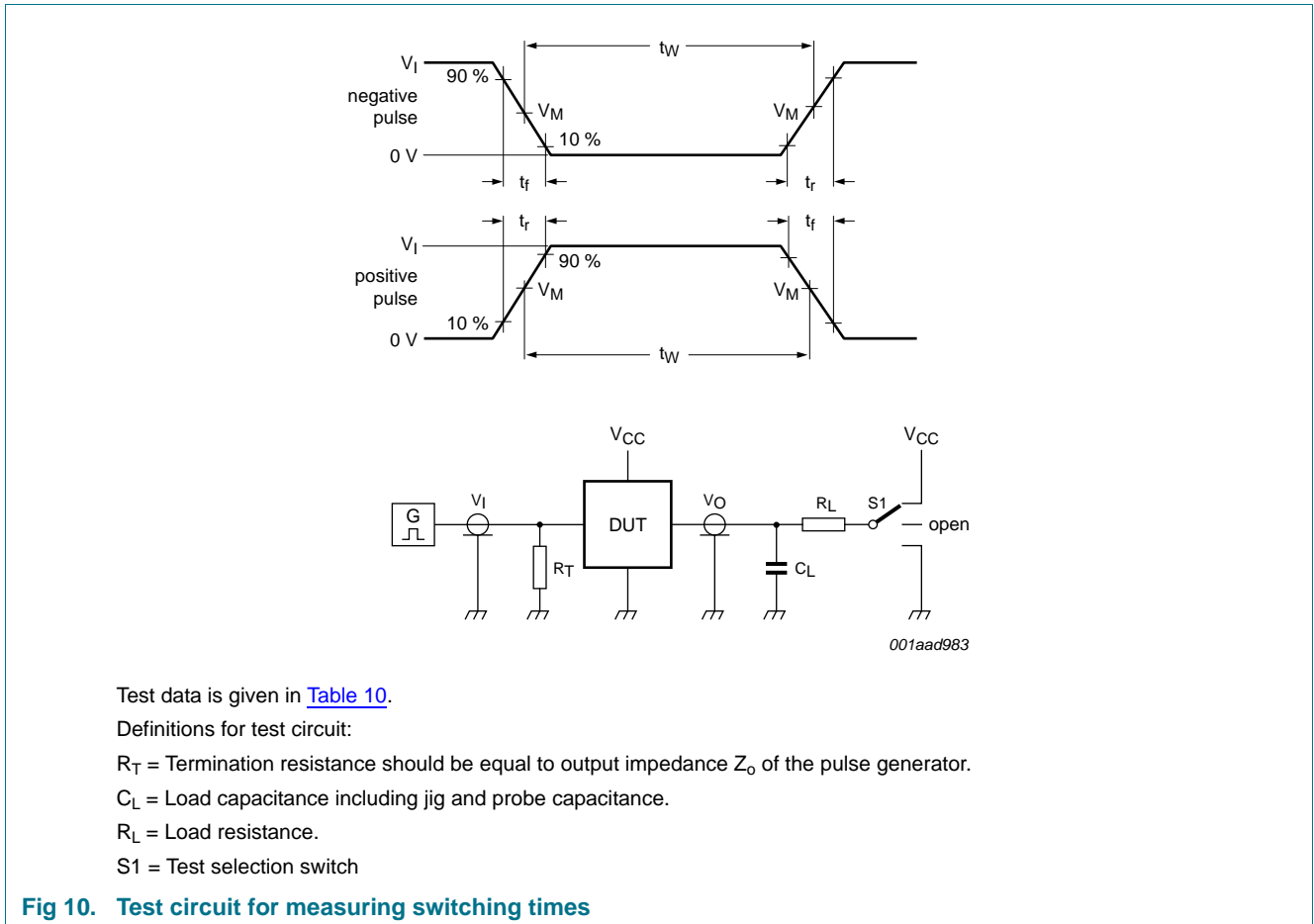


Fig 10. Test circuit for measuring switching times

Table 9. Test data

| Type | Input | | Load | | S1 position |
|----------|----------|------------|--------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} |
| 74HC166 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open |
| 74HCT166 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open |

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

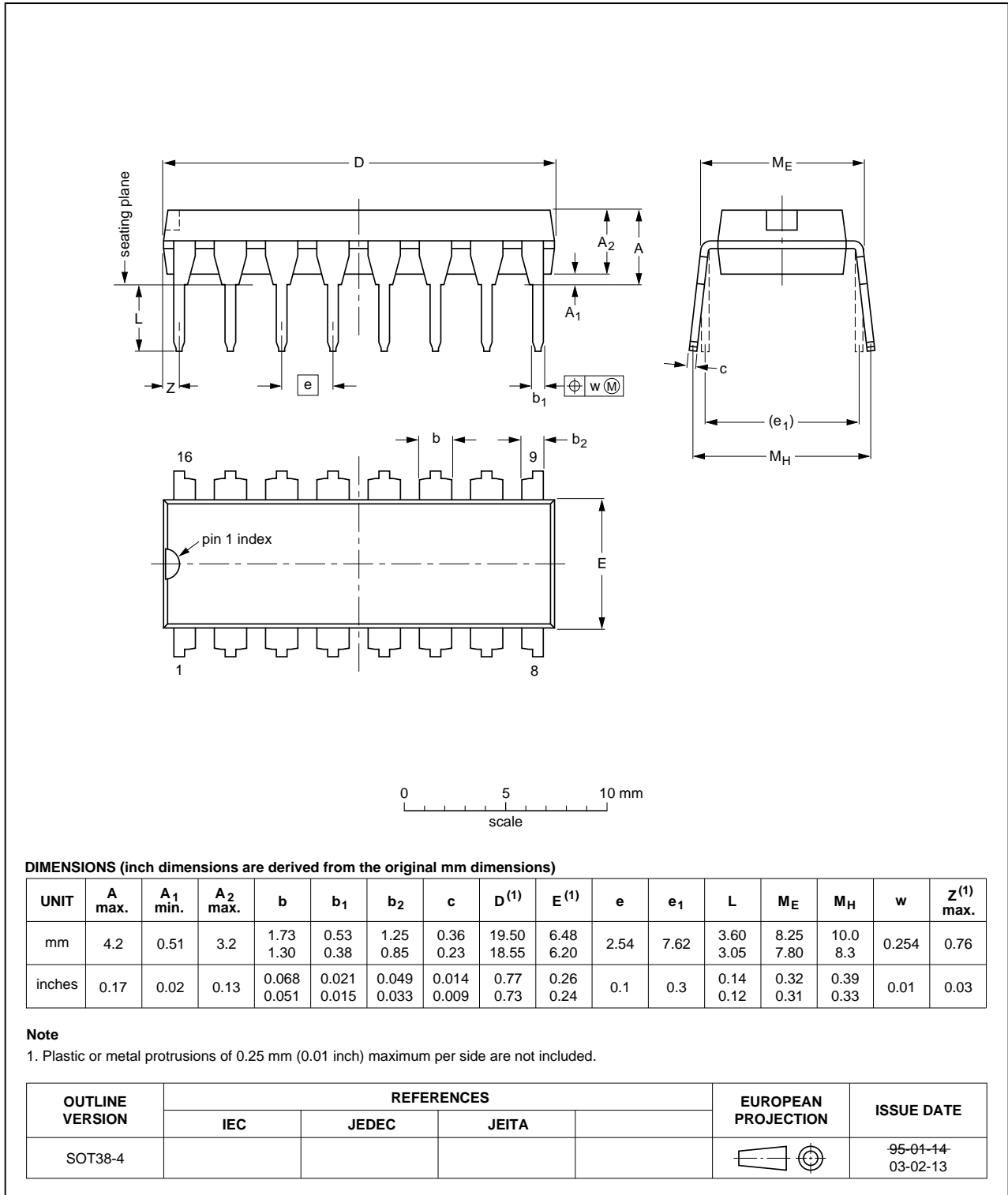


Fig 11. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

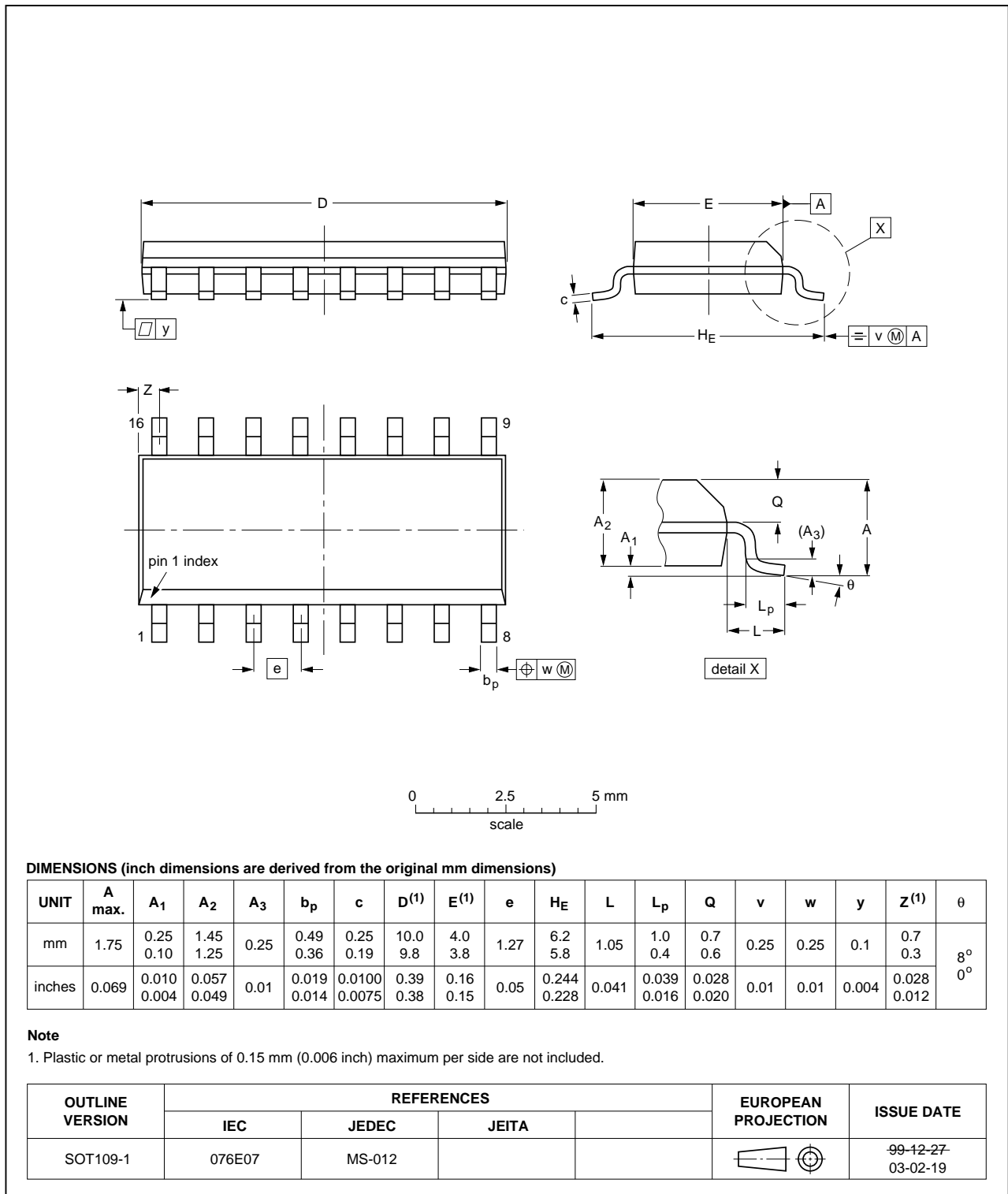


Fig 12. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

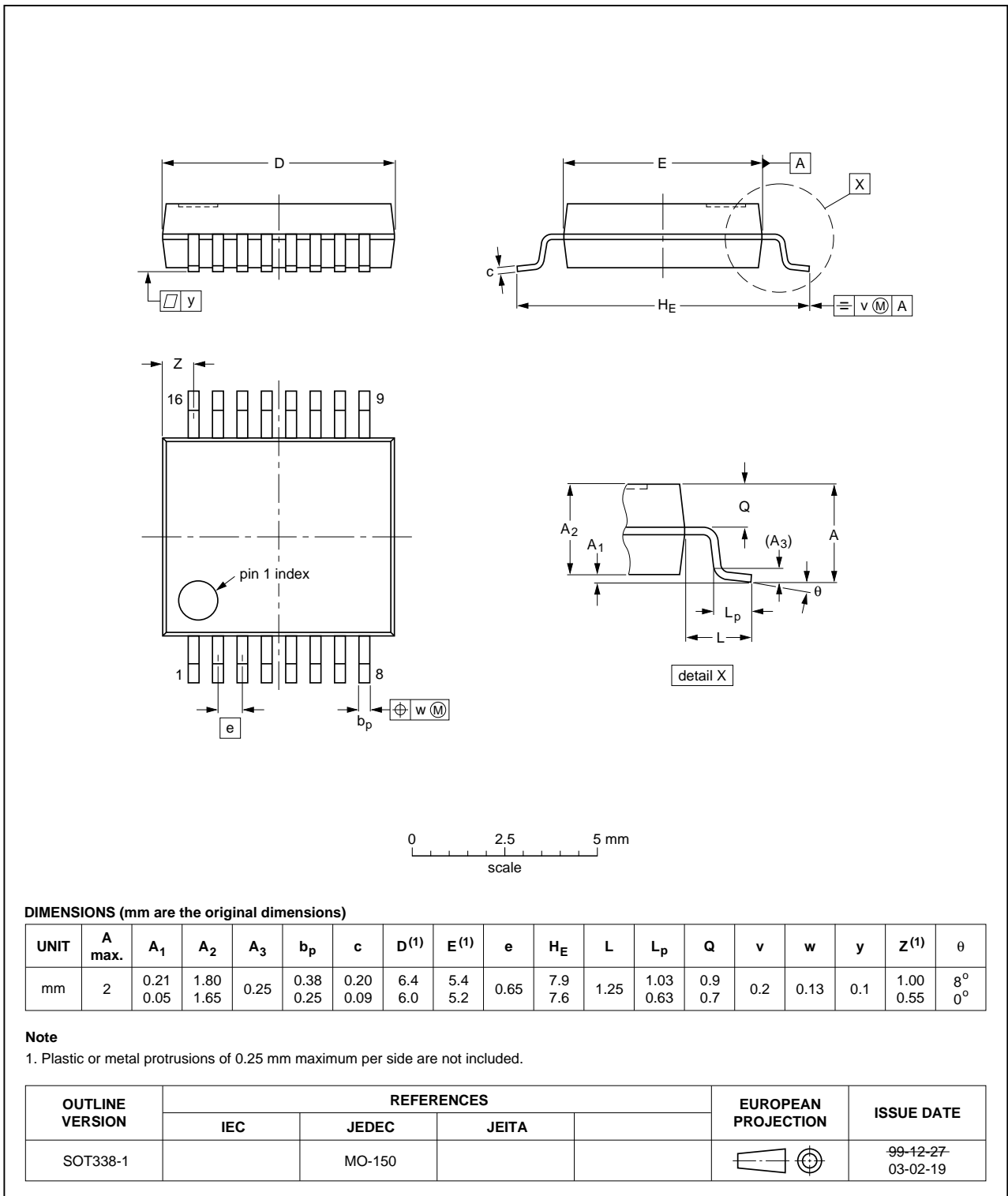


Fig 13. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

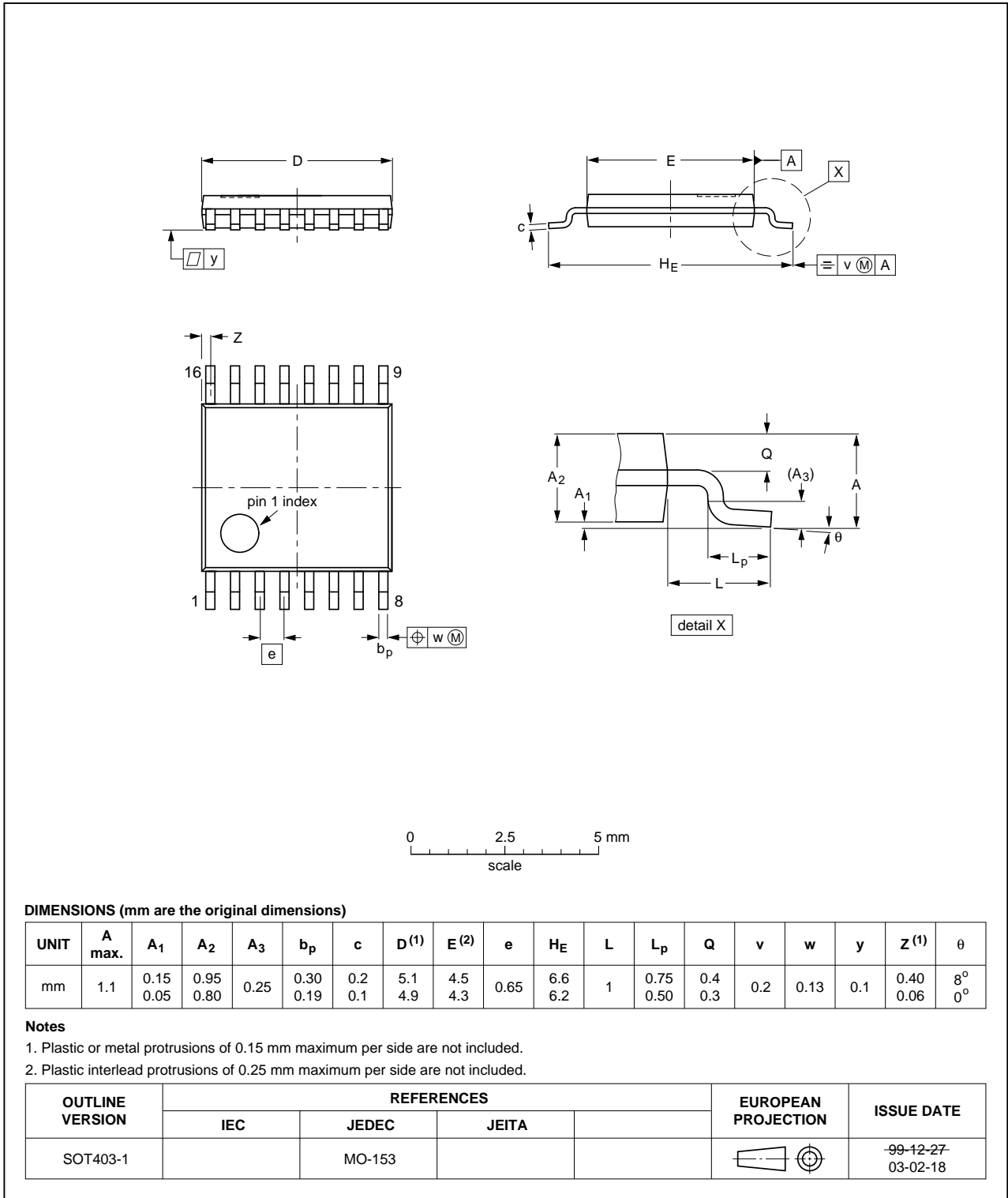


Fig 14. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--|-----------------------|---------------|-------------------|
| 74HC_HCT166_3 | 20130911 | Product data sheet | - | 74HC_HCT166_CNV_2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Family data added, see Section 9 "Static characteristics" | | | |
| 74HC_HCT166_CNV_2 | December 1990 | Product specification | - | - |

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15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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17. Contents

| | | |
|-----------|---|-----------|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Applications | 1 |
| 4 | Ordering information | 1 |
| 5 | Functional diagram | 2 |
| 6 | Pinning information | 4 |
| 6.1 | Pinning | 4 |
| 6.2 | Pin description | 4 |
| 7 | Functional description | 5 |
| 8 | Limiting values | 6 |
| 9 | Recommended operating conditions | 7 |
| 10 | Static characteristics | 7 |
| 11 | Dynamic characteristics | 9 |
| 12 | Waveforms | 11 |
| 13 | Package outline | 14 |
| 14 | Abbreviations | 18 |
| 15 | Revision history | 18 |
| 16 | Legal information | 19 |
| 16.1 | Data sheet status | 19 |
| 16.2 | Definitions | 19 |
| 16.3 | Disclaimers | 19 |
| 16.4 | Trademarks | 20 |
| 17 | Contact information | 20 |
| 18 | Contents | 21 |

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