Description

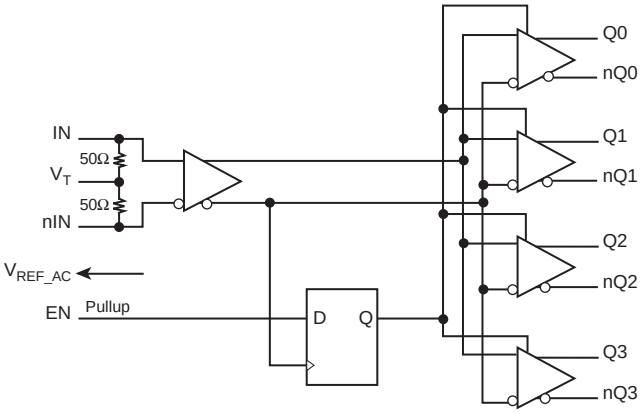
The 8S89833 is a high speed 1-to-4 Differential-to-LVDS Fanout Buffer with Internal Termination. The 8S89833 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVPECL, LVDS, and CML to be easily interfaced to the input with minimal use of external components. The device also has an output enable pin which may be useful for system test and debug purposes.

The 8S89833 is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

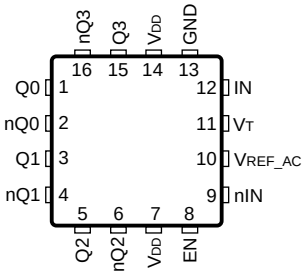
Features

- Four differential LVDS outputs
- IN, nIN input pair can accept the following differential input levels: LVPECL, LVDS, CML
- Output frequency: 2GHz
- Cycle-to-cycle jitter, RMS: 3.5ps (maximum)
- Additive phase jitter, RMS: 0.03ps (typical)
- Output skew: 30ps (maximum)
- Part-to-part skew: 200ps (maximum)
- Propagation Delay: 600ps (maximum)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



8S89833

16-Lead VFQFN
3mm x 3mm x 0.925mm package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. Normally terminated with 100Ω across the pair. LVDS interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. Normally terminated with 100Ω across the pair. LVDS interface levels.
5, 6	Q2, nQ2	Output		Differential output pair. Normally terminated with 100Ω across the pair. LVDS interface levels.
7, 14	V_{DD}	Power		Power supply pins.
8	EN	Input	Pullup	Synchronizing output enable pin. When LOW, disables outputs. When HIGH, enables outputs. Internally connected to a 37kΩ pullup resistor. LVTTL / LVCMOS interface levels.
9	nIN	Input		Inverting differential LVPECL clock input. RT = 50Ω termination to V_T.
10	V_{REF_AC}	Output		Reference voltage for AC-coupled applications. Equal to V_{DD} - 1.4V (approx.). Maximum sink/source current is ±2mA.
11	V_T	Input		Input termination center-tap. Each side of the differential input pair terminates to a V_T pin. The V_T pins provide a center-tap to a termination network for maximum interface flexibility.
12	IN	Input		Non-inverting differential clock input. RT = 50Ω termination to V_T.
13	GND	Power		Power supply ground.
15, 16	Q3, nQ3	Output		Differential output pair. Normally terminated with 100Ω across the pair. LVDS interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37		kΩ

Function Tables

Table 3. Control Input Function Table

Inputs			Outputs	
IN	**nIN**	**EN**	**Q[0:3]**	**nQ[0:3]**
0	1	1	0	1
1	0	1	1	0
X	X	0	Disabled LOW[NOTE 1]	Disabled HIGH[NOTE 1]

NOTE 1: On the next negative transition of the input signal (IN).

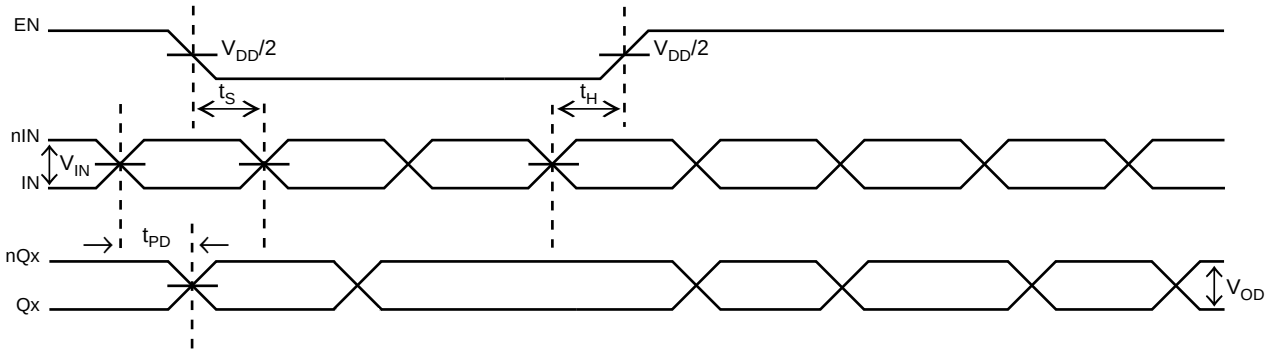


Figure 1. EN Timing Diagram

Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuos Current Surge Current	 10mA 15mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	± 2mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}, (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				100	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.6V			10	µA
I_{IL}	Input Low Current	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{DIFF_IN}	Differential Input Resistance	(IN, nIN)		80	100	120	Ω
R_{IN}	Input Resistance		IN-to-VT	40	50	60	Ω
V_{IH}	Input High Voltage	(IN, nIN)		1.2		V_{DD}	V
V_{IL}	Input Low Voltage	(IN, nIN)		0		V_{IH} – 0.15	V
V_{IN}	Input Voltage Swing			0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
V_{REF_AC}	Bias Voltage			V_{DD} – 1.44	V_{DD} – 1.38	V_{DD} – 1.32	V
I_{IN}	Input Current; NOTE 1		IN-to-VT			35	mA

NOTE 1: Guaranteed by design.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	V
V_{OS}	Offset Voltage		1.2	1.4	1.6	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

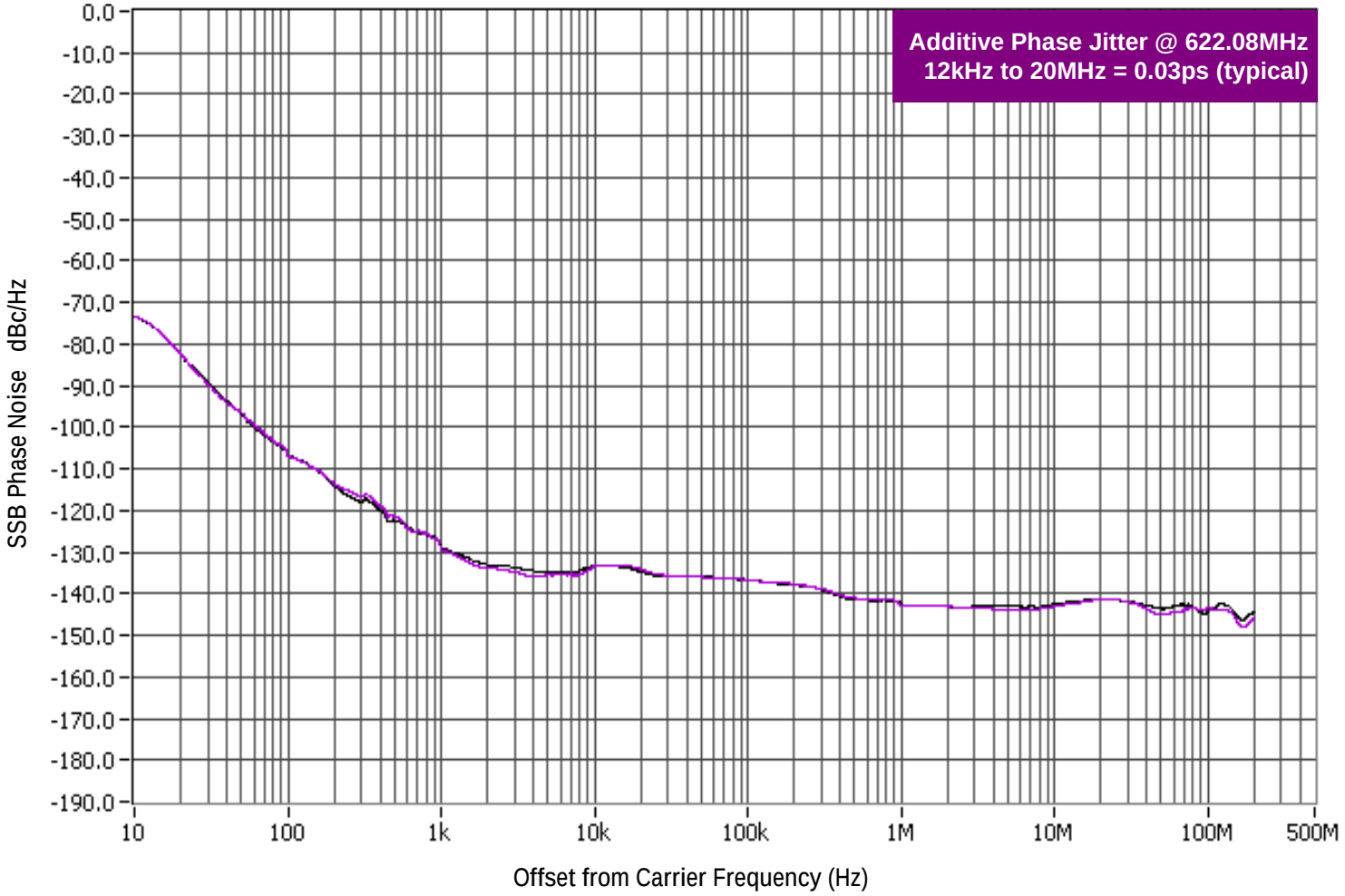
Table 5. AC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					2	GHz
t_{PD}	Propagation Delay, (Differential); NOTE 1	IN-to-Qx		400		600	ps
*t*sk(o)	Output Skew; NOTE 2, 3					30	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					200	ps
*t*jit(cc)	Cycle-to-Cycle Jitter, RMS; NOTE 5, 6					3.5	ps
*t*jit	Buffer Additive Jitter; RMS; refer to Additive Phase Jitter Section		*f* = 622.08MHz, Integration Range: 12kHz - 20MHz		0.03		ps
			f ≥ 156.25MHz, Integration Range: 12kHz - 20MHz			0.25	ps
t_S	Clock Enable Setup Time	EN to IN/nIN		300			ps
t_H	Clock Enable Hold Time	EN to IN/nIN		500			ps
t_R / t_F	Output Rise/Fall Time		20% – 80%	75		200	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters characterized at ≤ 1.4GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: Tested at *f* ≤ 750MHz.
NOTE 6: The cycle-to-cycle jitter is dependent on the input source and measurement equipment.

Additive Phase Jitter

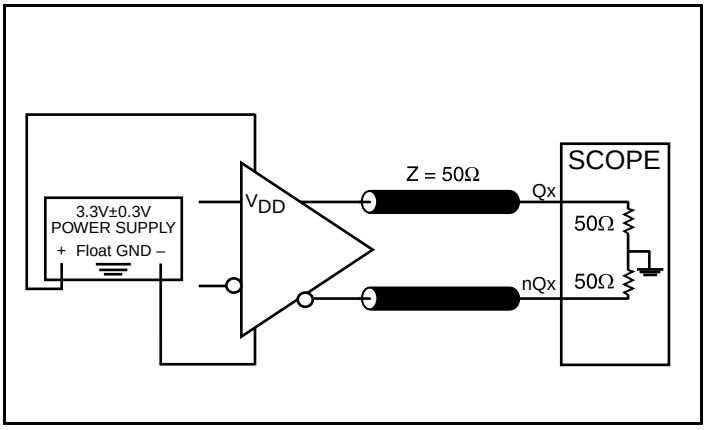
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



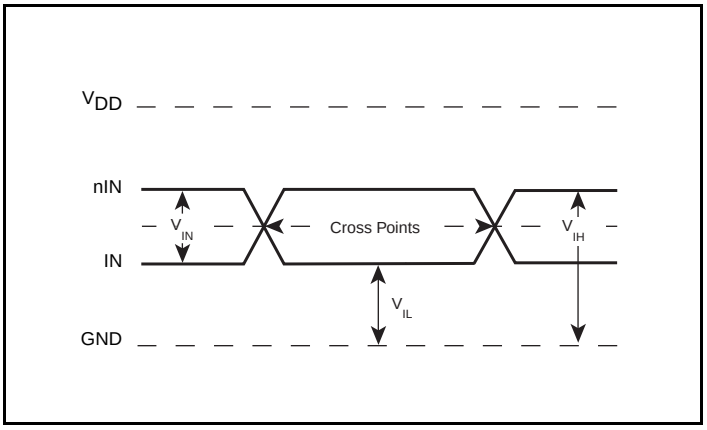
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator “IFR2042 10kHz – 6.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator”.

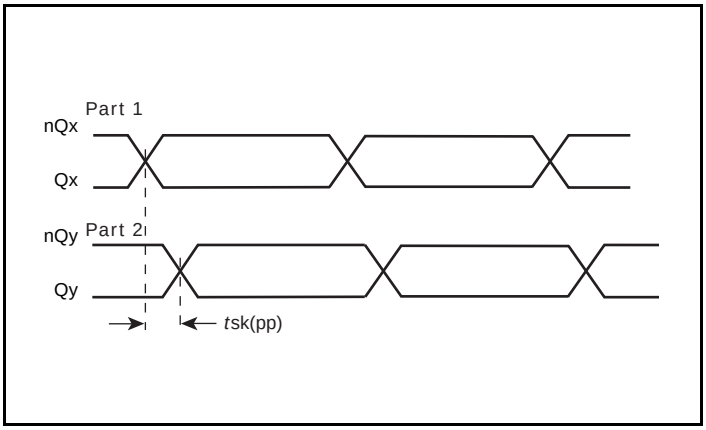
Parameter Measurement Information



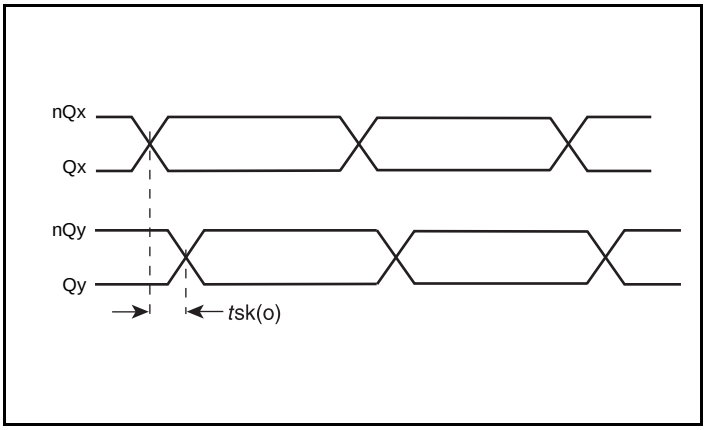
LVDS Output Load AC Test Circuit



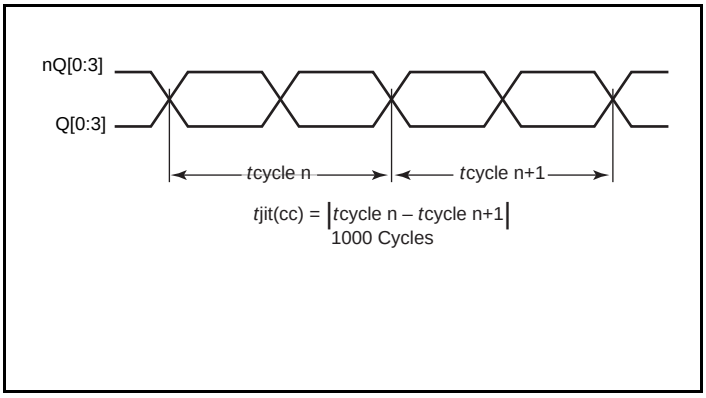
Differential Input Level



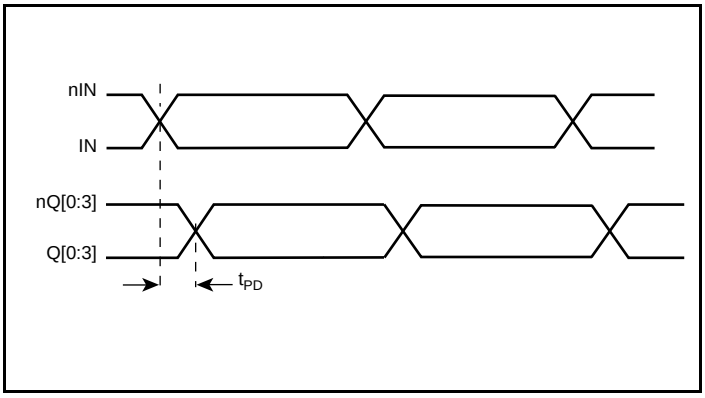
Part-to-Part Skew



Output Skew

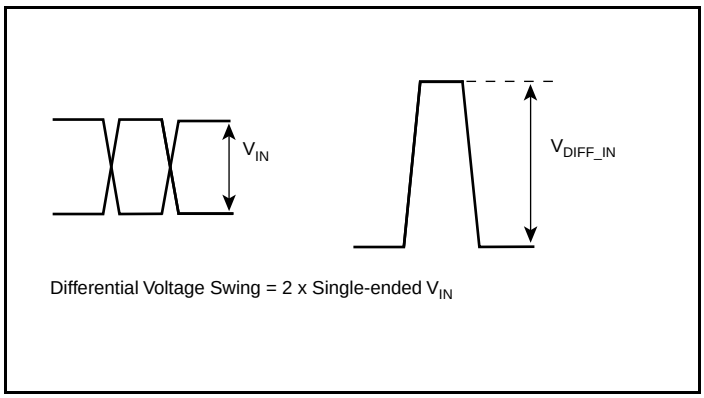


Cycle-to-Cycle Jitter, RMS

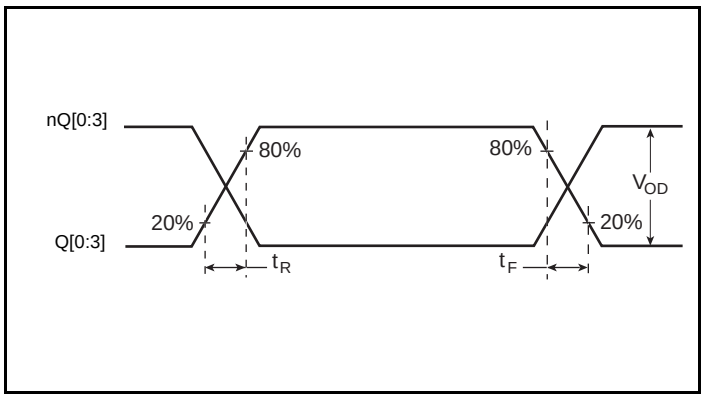


Propagation Delay

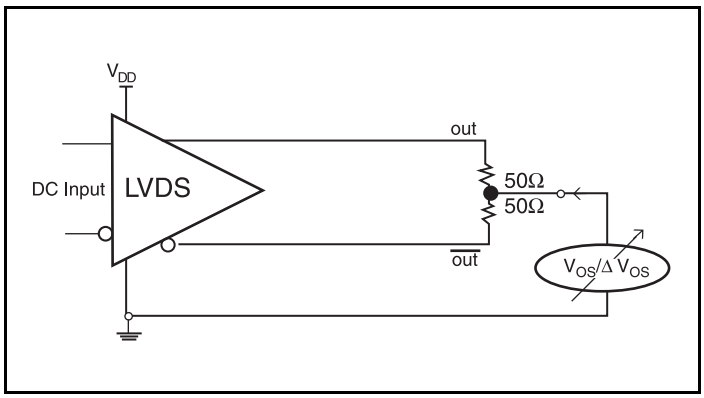
Parameter Measurement Information, continued



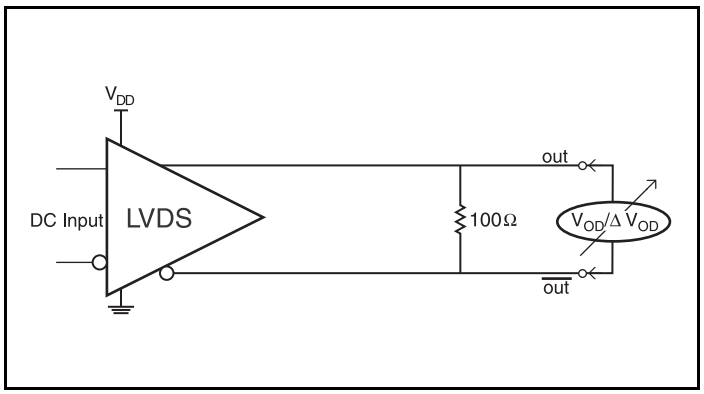
Single-Ended & Differential Input Voltage Swing



Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both differential signals must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

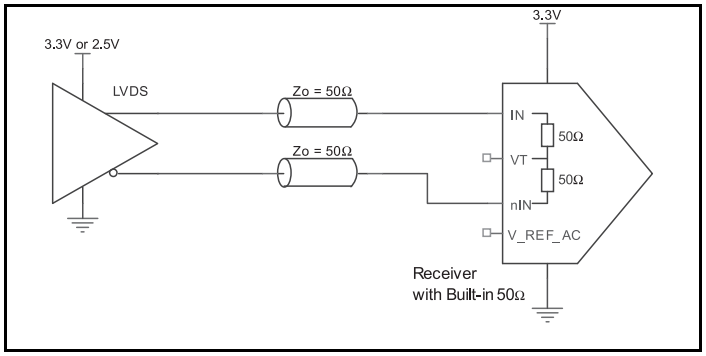


Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

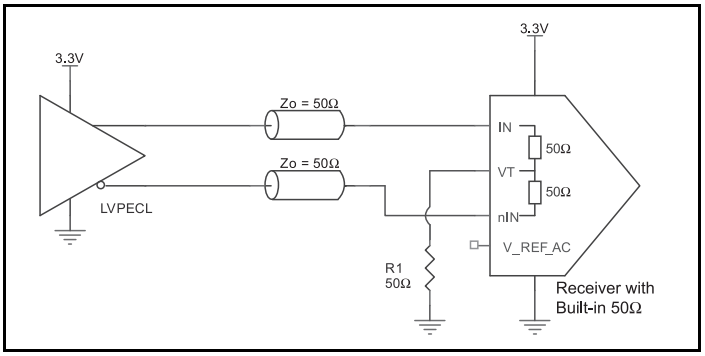


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

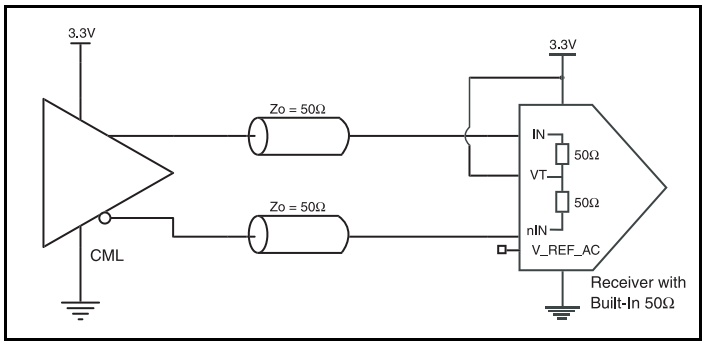


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

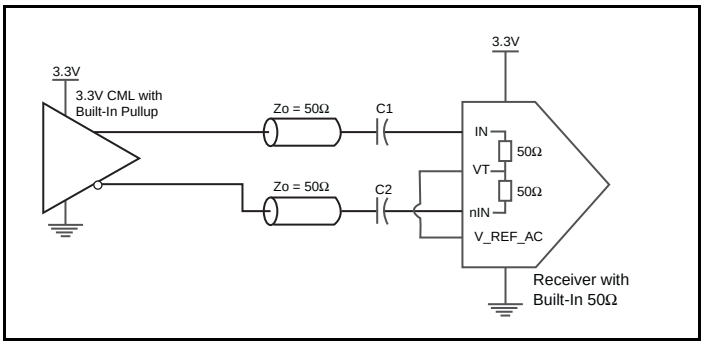


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

Recommendations for Unused Output Pins

Outputs

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

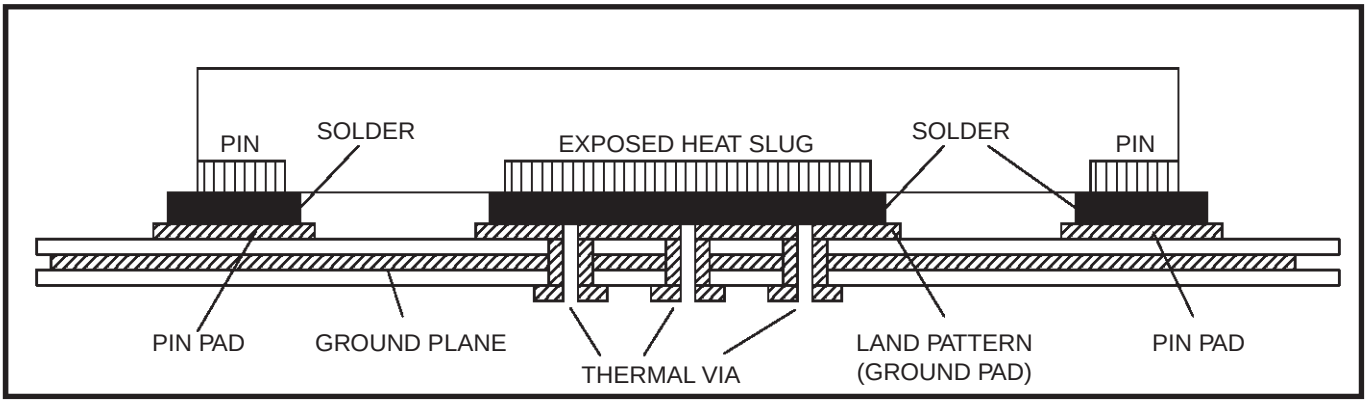


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure X can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

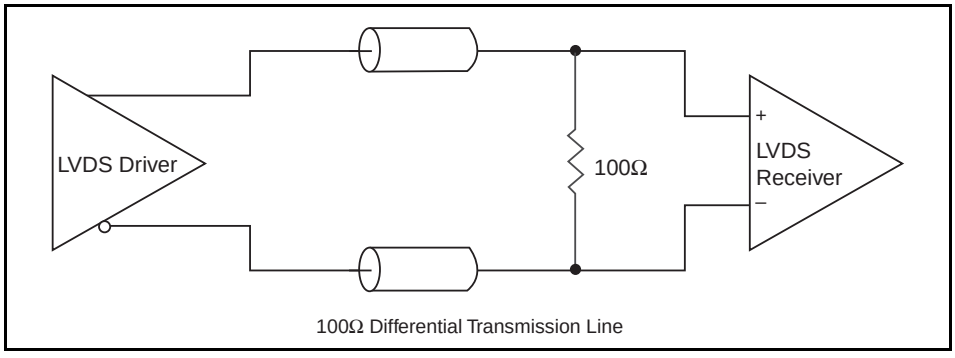


Figure 4. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 8S89833.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8S89833 is the sum of the core power plus the analog power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 0.3V = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.63V * 100mA = **363mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX}$ = $(V_{IN\_MAX})^2$ / R_{T_MIN} = $(1.2V)^2$ / 80Ω = **18mW**

Total Power$_{\_MAX}$ = 363mW + 18mW = **381mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.381W * 74.7°C/W = 113.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for 8S89833 is: 353
This device is pin and function compatible and a suggested replacement for 889833.

Package Outline Drawings

The package outline drawings are located in the last section of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S89833AKILF	833A	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
8S89833AKILFT	833A	“Lead-Free” 16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

Revision History

Revision Date	Description of Change
September 22, 2017	▪ Updated the package outline drawings; however, no mechanical changes ▪ Completed other minor improvements
August 24, 2016	▪ Table 4C Differential DC Characteristics Table, typo correction: – V_{IL} row, maximum spec changed from V_{IN} - 0.15V to V_{IH} - 0.15V. ▪ Deleted “I” suffix from the part number.
February 8, 2016	▪ Removed ICS from part number where needed. ▪ Removed LF note below Ordering Information table. ▪ Updated header and footer.

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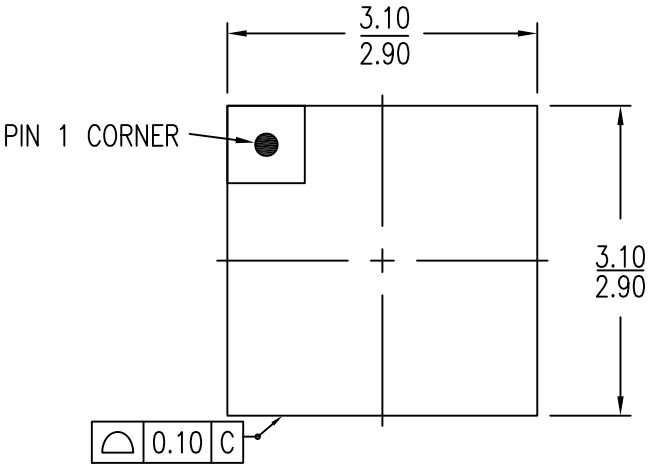
Tech Support
www.IDT.com/go/support

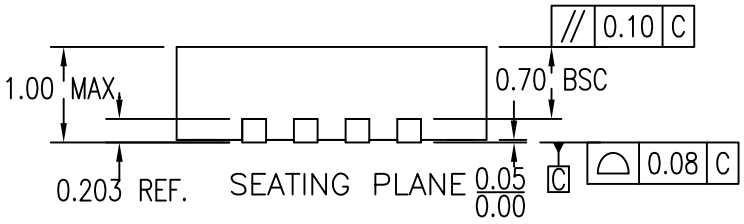
16L-QFN Package Outline Drawing

3.0 x 3.0 x 1.0 mm, 0.5 mm Pitch, 1.70 x 1.70 mm Epad

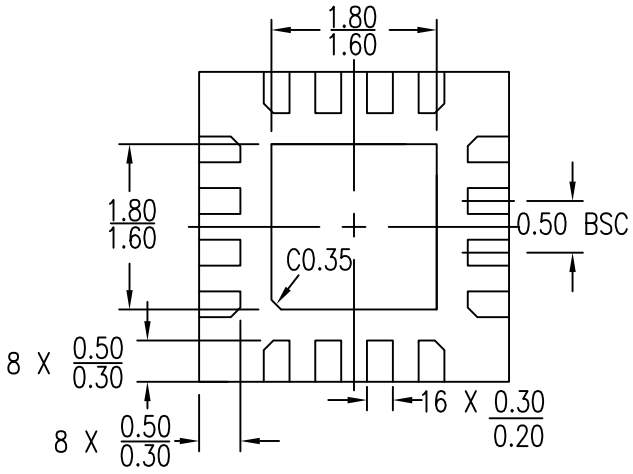
NL/NLG16P2, PSC-4169-02, Rev 03, Page 1



TOP VIEW



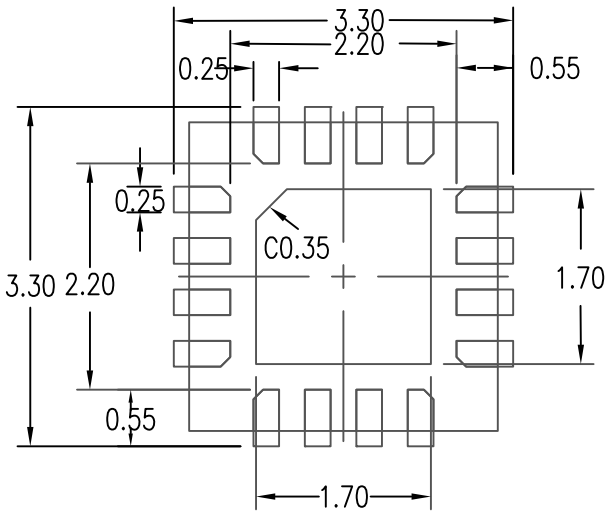
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES



RECOMMENDED LAND PATTERN

NOTES:
1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Aug 15, 2017	Rev 03	Update Epad Range
Jul 28, 2017	Rev 02	New format