Si5018-EVB

EVALUATION BOARD FOR Si5018 SiPHY™ OC-48/STM-16 CLOCK AND DATA RECOVERY IC WITH FEC

Description

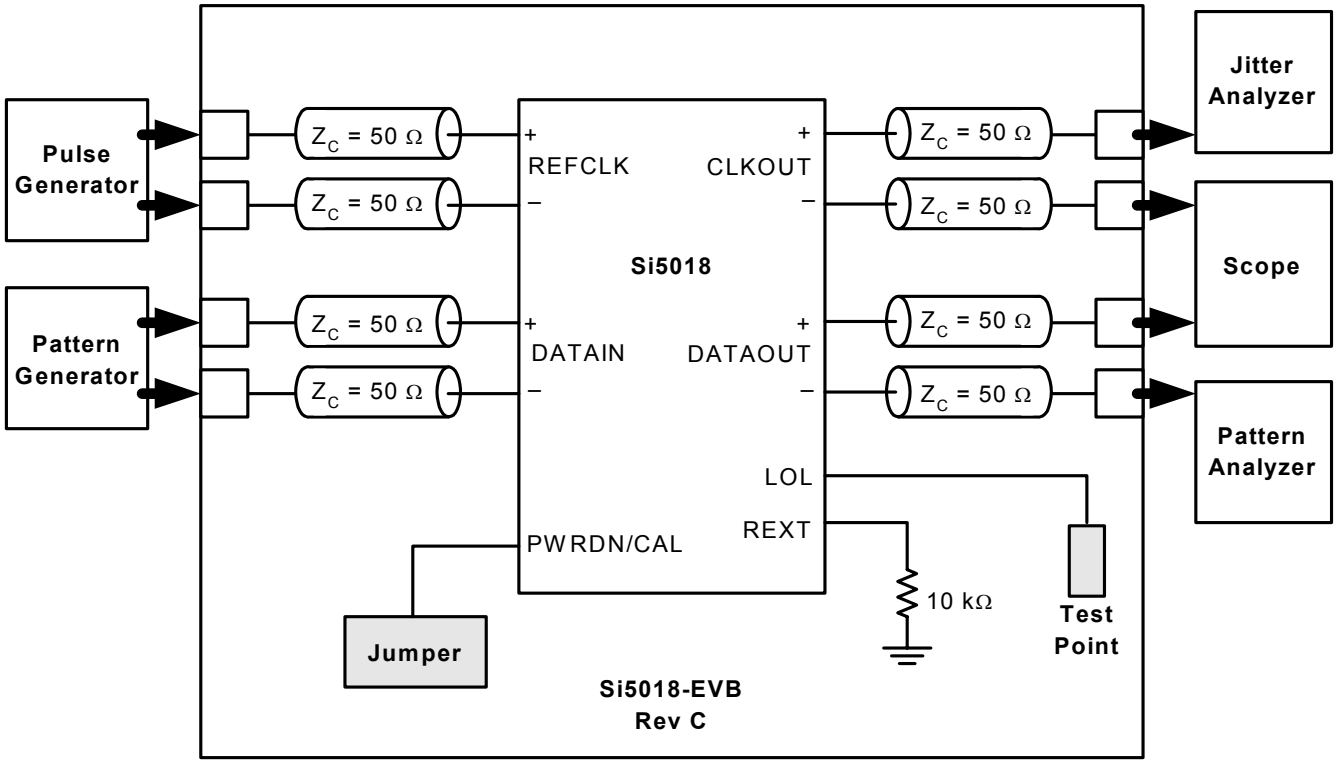
The Si5018 evaluation board provides a platform for testing and characterizing Silicon Laboratories Si5018 OC-48, STM-16, and 2.7 Gbps FEC clock and data recovery (CDR) device.

All high-speed I/Os are ac coupled to ease interfacing to industry standard test equipment.

Features

- Single 2.5 V power supply
- Differential I/Os ac coupled
- Simple jumper configuration

Function Block Diagram



Functional Description

The evaluation board simplifies characterization of the Si5018 OC-48, STM-16, and 2.7 Gbps FEC clock and data recovery (CDR) device by providing access to all of the Si5018 I/Os. Device performance can be evaluated by following the Test Configuration section below. Specific performance metrics include jitter tolerance, jitter generation, and jitter transfer.

Power Supply

The evaluation board requires one 2.5 V supply. Supply filtering is placed on the board to filter typical system noise components, however, initial performance testing should use a linear supply capable of supplying 2.5 V ±5% dc.

CAUTION: The evaluation board is designed so that the body of the SMA jacks and GND are shorted. Care must be taken when powering the PCB at potentials other than GND at 0.0 V and VDD at 2.5 V relative to chassis GND.

Self-Calibration

The Si5018 device provides an internal self-calibration function that optimizes the loop gain parameters within the internal DSPLL™. Self-calibration is initiated by a high-to-low transition of the PWRDN/CAL signal while a valid reference clock is supplied to the REFCLK input. On the Si5018-EVB board, a voltage detector IC is utilized to initiate self-calibration. The voltage detector drives the PWRDN/CAL signal low after the supply voltage has reached a specific voltage level. This circuit is described in Silicon Laboratories application note AN42. On the Si5018-EVB, the PWRDN/CAL signal is also accessible via a jumper located in the lower left-hand corner of the evaluation board. PWRDN/CAL is wired to the signal post adjacent to the 2.5 V post.

Device Powerdown

The CDR can be powered down via the PWRDN/CAL signal. When asserted the evaluation board will draw minimal current. PWRDN/CAL is controlled via one jumper located in the lower left-hand corner of the evaluation board. PWRDN/CAL is wired to the signal post adjacent to the 2.5 V post.

CLKOUT, DATAOUT, DATAIN

These high-speed I/Os are wired to the board perimeter on 30 mil (0.030 inch) 50 Ω microstrip lines to the end-launch SMA jacks as labeled on the PCB. These I/Os are ac coupled to simplify direct connection to a wide array of standard test hardware. Because each of these signals are differential both the positive (+) and negative (–) terminals must be terminated to 50 Ω. Terminating only one side will adversely degrade the performance of the CDR. The inputs are terminated on the die with 50 Ω resistors.

To improve the DATAOUT eye-diagram, short 100 Ω transmission line segments precede the 50 Ω high-speed traces. These segments increase the interface bandwidth from the chip to the 50 Ω traces and reduce data inter-symbol-interference. Please refer to Silicon Laboratories application note AN43 for more details.

Note: The 50 Ω termination is for each terminal/side of a differential signal, thus the differential termination is actually 50 Ω + 50 Ω = 100 Ω.

REFCLK

REFCLK is used to center the frequency of the DSPLL™ so that the device can lock to the data. Ideally the REFCLK frequency should be 1/128th, 1/32nd, or 1/16th the VCO frequency and must have a frequency accuracy of ±100 PPM. Internally, the CDR automatically recognizes the REFCLK frequency within one of these three frequency ranges. Typical REFCLK frequencies are given in Table 1. REFCLK is ac coupled to the SMA jacks located on the top side of the evaluation board.

Table 1. Typical REFCLK Frequencies

SONET/SDH	Gigabit Ethernet	SONET/ SDH with 15/14 FEC	Ratio of VCO to REFCLK
19.44 MHz	19.53 MHz	20.83 MHz	128
77.76 MHz	78.125 MHz	83.31 MHz	32
155.52 MHz	156.25 MHz	166.63 MHz	16

Loss-of-Lock (LOL)

LOL is an indicator of the relative frequency between the data and the REFCLK. LOL will assert when the frequency difference is greater than ±600 PPM. In order to prevent LOL from de-asserting prematurely, there is hysterisis in returning from the out-of-lock condition. LOL will be de-asserted when the frequency difference is less than ±300 PPM.

LOL is wired to a test point which is located on the upper right-hand side of the evaluation board.

Test Configuration

The three critical tests that are typically performed on a CDR device are jitter transfer, jitter tolerance, and jitter generation. By connecting the Si5018 Evaluation Board as shown in Figure 1, all three measurements can be easily made.

REFCLK should be within ±100 PPM of the frequency selected from Table 1. PWRDN/CAL must be unjumpered.

Jitter Tolerance: Referring to Figure 1, this test requires a pattern generator, a clock source (synthesizer signal source), a modulation source, a jitter analyzer, a pattern analyzer, and a pulse generator (all unconnected high-speed outputs must be terminated to 50 Ω). During this test the Jitter Analyzer causes a modulation on the data pattern which drives the DATAIN ports of the CDR. The Bit-Error-Rate (BER) is monitored on the Pattern Analyzer. The modulation (jitter) frequency and amplitude is recorded when the BER approaches a specified threshold.

Jitter Generation: Referring to Figure 1, this test requires a pattern generator, a clock source (synthesizer signal source), a jitter analyzer, and a pulse generator (all unconnected high-speed outputs must be terminated to 50 Ω). During this test there is no modulation of the Data Clock, so the data that is sent to the CDR is jitter free. The Jitter Analyzer measures the RMS and peak-to-peak jitter on the CDR CLKOUT. Thus, any jitter measured is jitter generated by the CDR.

Jitter Transfer: Referring to Figure 1, this test requires a pattern generator, a clock source (synthesizer signal source), a modulation source, a jitter analyzer, and a pulse generator (all unconnected high-speed outputs must be terminated to 50 Ω). During this test the Jitter Analyzer modulates the data pattern and data clock reference. The modulated data clock reference is compared with the CLKOUT of the CDR. Jitter on CLKOUT relative to the jitter on the data clock reference is plotted versus modulation frequency at predefined jitter amplitudes.

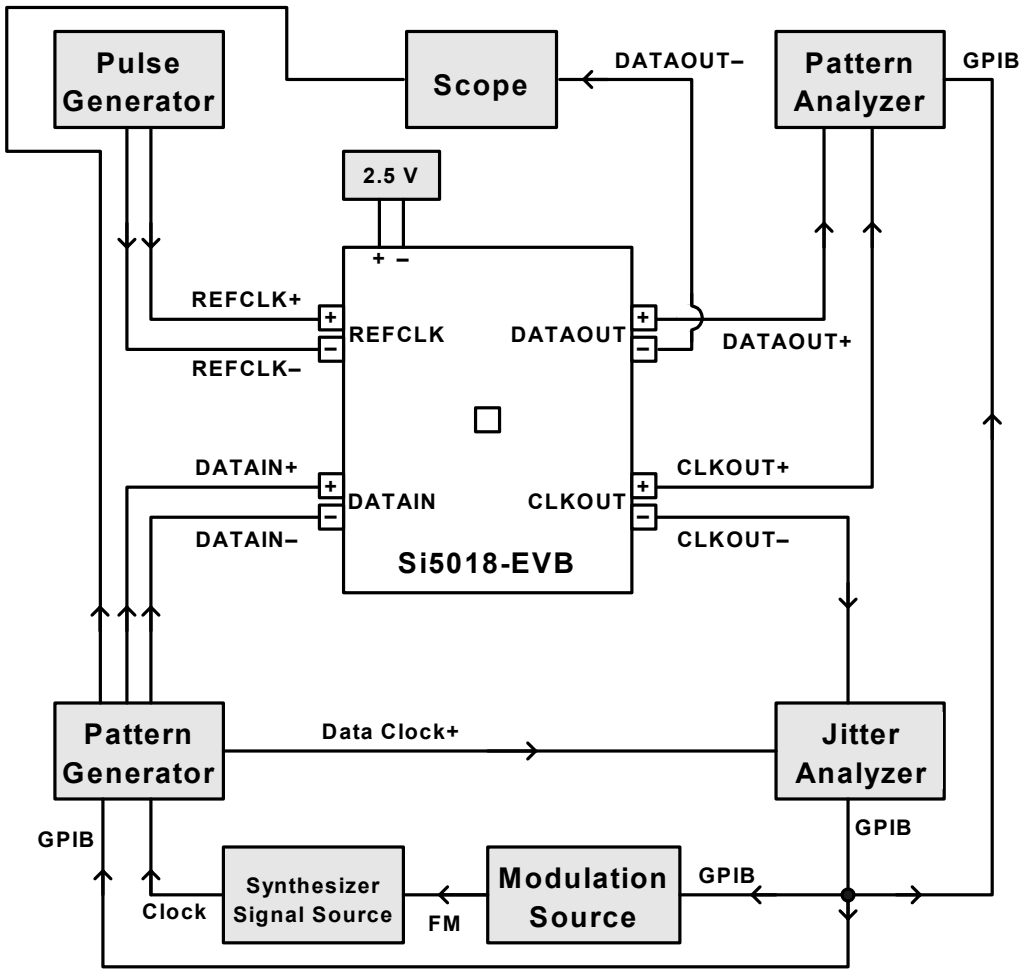


Figure 1. Test Configuration for Jitter Tolerance, Transfer, and Generation

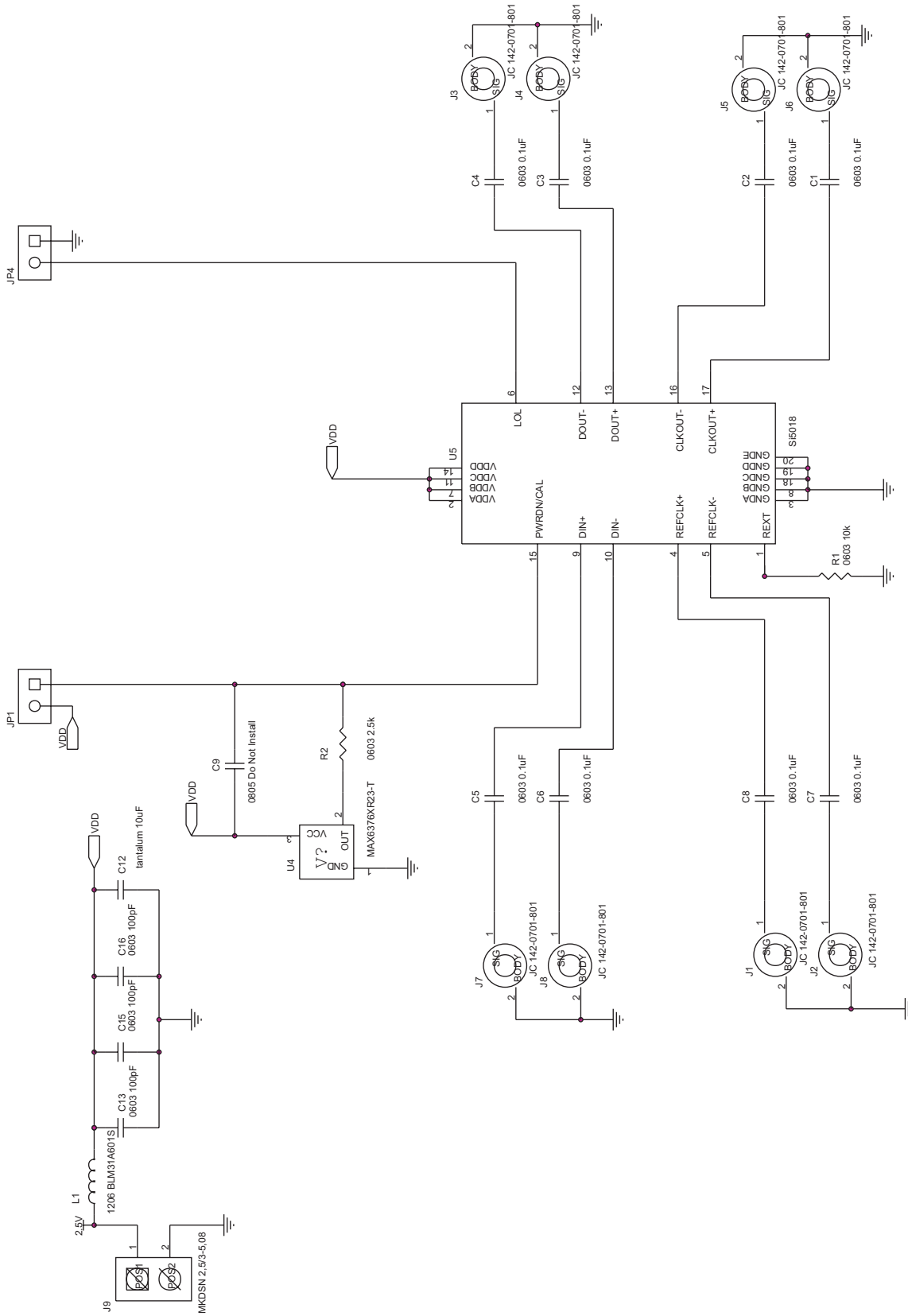


Figure 2. Si5018 Schematic

Bill of Materials

Si5018EVB Assy Rev B-02 BOM			
Reference	**Part Desc**	**Part Number**	**Manufacturer**
C1,C2,C3,C4,C5, C6,C7,C8	CAP, SM, 0.1uF, 0603	C0603X7R160-104KNE	Venkel
C12	CAP, SM, 10 uF, TANTALUM, 3216	TA010TCM106KAR	Venkel
C13,C15,C16	CAP, SM, 100 pF, 16V, 0603	C0603C0G500101KNE	Venkel
JP1	CONNECTOR, HEADER, 2X1	2340-6111TN or 2380-6121TN	3M
J1,J2,J3,J4,J5,J6, J7,J8	CONNECTOR, SMA, SIDE MOUNT	901-10003	Amphenol
J9	CONNECTOR, POWER, 2 POS	1729018	Phoenix Contact
L1	RESISTOR, SM, 0 OHM, 1206	CR1206-8W-000T	Venkel
R1	RESISTOR, SM, 10K, 1%, 0603	CR0603-16W-1002FT	Venkel
R2	RESISTOR, SM, 2.55K, 1%, 0603	CR0603-16W-2551FT	Venkel
U4	MAX6376XR23-T	MAX6376XR23-T	Maxim
U5	Si5018	SI5018-BM	Silicon Laboratories
PCB	PRINTED CIRCUIT BOARD	Si5018-EVB PCB Rev C	Silicon Laboratories
No Load			
C9	SPARE,0805		

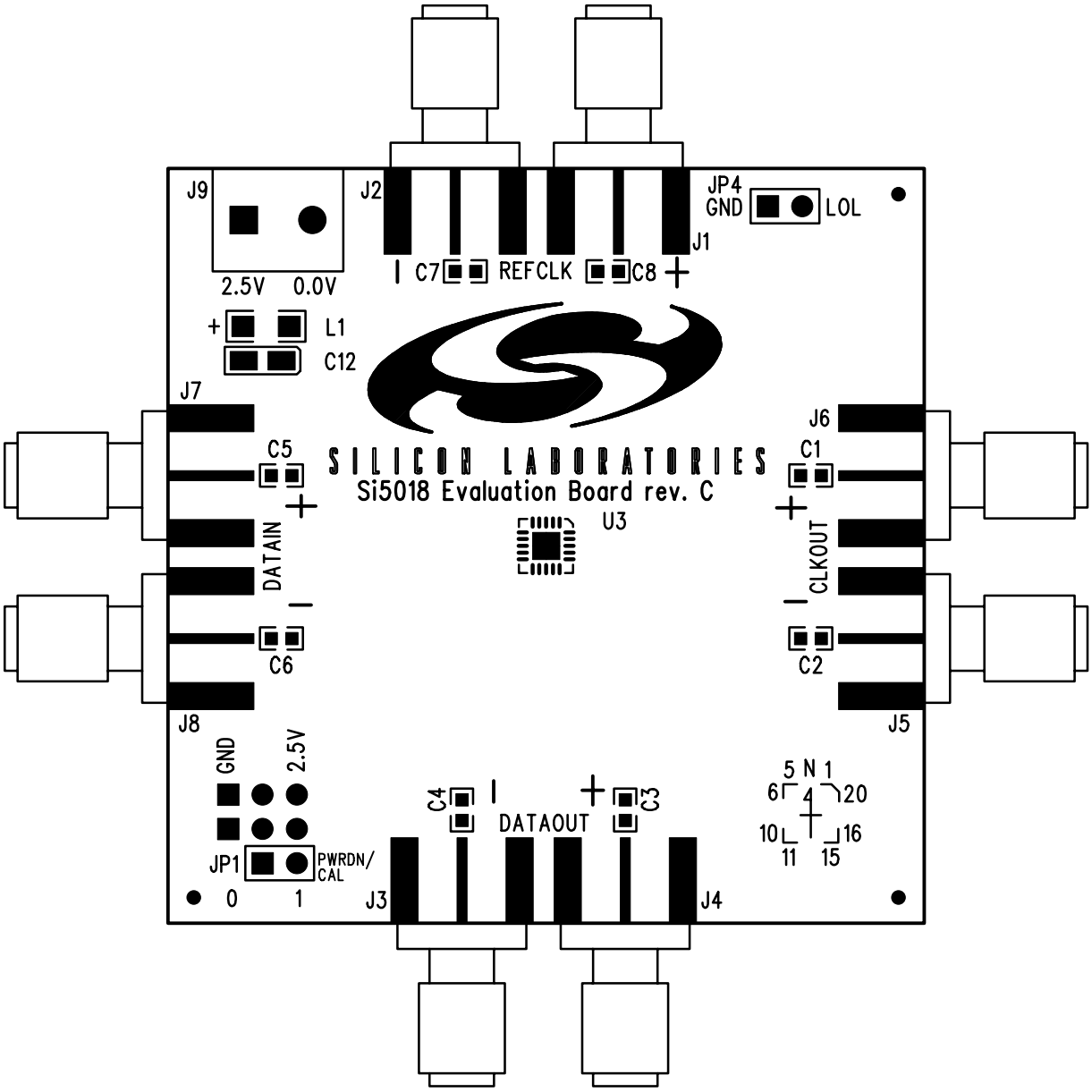


Figure 3. Si5018 Silkscreen

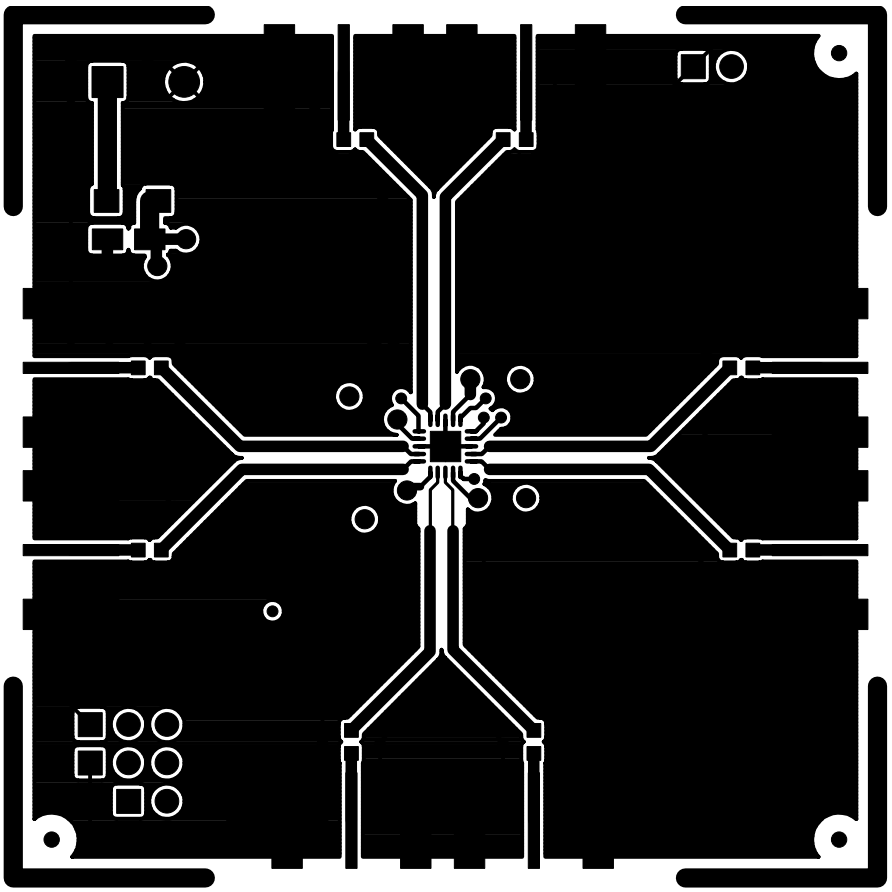


Figure 4. Si5018 Component Side

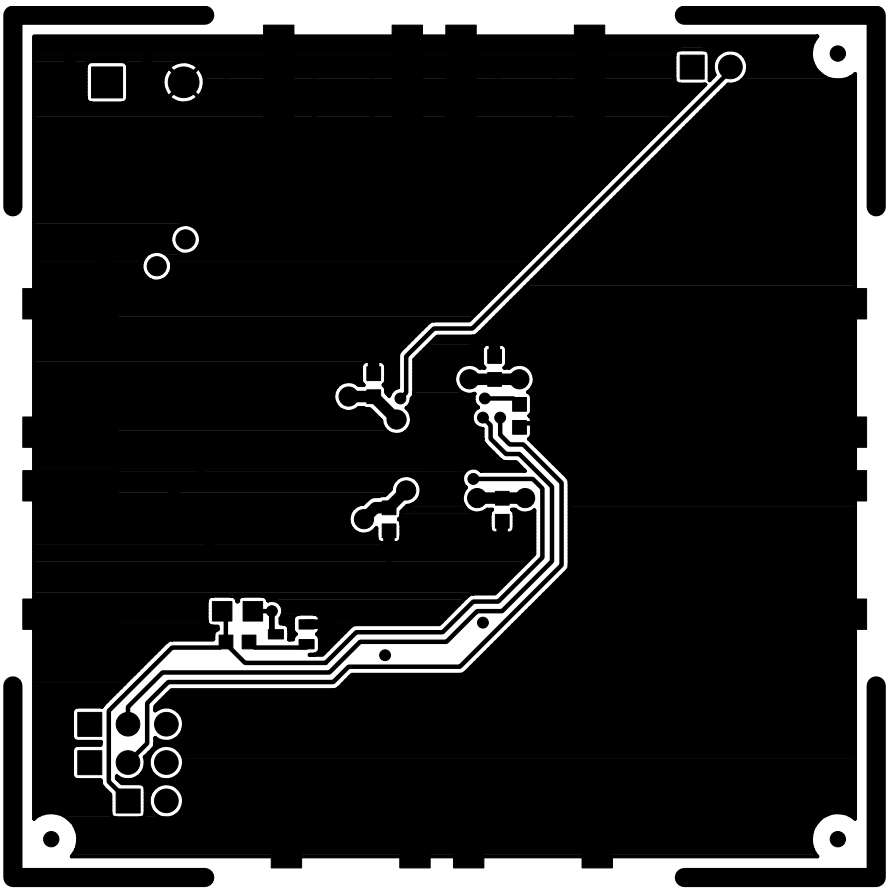


Figure 5. Solder Side

Document Change List

Revision 0.41 to Revision 1.0

- "Preliminary" language removed.

Evaluation Board Assembly Revision History

Assembly Level	PCB	Si5018 Device	Assembly Notes
A-01	A	A	Assemble per BOM rev A-01.
B-01	B	B	Assemble per BOM rev B-01.
B-02	C	B	Assemble per BOM rev B-02.

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