LED System Driver IC

ICLS8023Z

Off-Line LED Current Mode Controllers
with Integrated 800 V CoolMOS™ & Startup Cell

Data Sheet

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
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Current Mode Controller with Integrated 800 V Startup Cell/Depletion CoolMOS™

Product Highlights

- 800 V avalanche-rugged CoolMOS™ with startup cell
- Adjustable blanking window for high-load jumps to increase reliability
- Frequency jittering and soft driving for low EMI
- Auto Restart protection for overload, overtemperature, overvoltage and undervoltage
- Pb-free lead plating, RoHS-compilant

Features

- 800 V avalanche-rugged CoolMOS™ with startup cell
- 65 kHz internally-fixed switching frequency with jittering feature
- Auto Restart mode for overtemperature detection
- Auto Restart mode for overvoltage detection
- Auto Restart mode for overload and open loop
- Auto Restart mode for VCC undervoltage
- Floating Load Protection (FLP) mode in the case of open loads
- External auto-restart enable pin
- Overtemperature protection with 50 °C hysteresis
- Built-in 10 ms soft start
- Built-in 20 ms and extendable blanking time for short duration peak power
- Propagation delay compensation for both maximum load and burst mode
- Overall tolerance of current limiting < ± 5 %
- Internal leading edge blanking
- BiCMOS technology for low power consumption and wide VCC voltage range
- Soft gate drive with 50 Ω turn-on resistor

Description

controllers employ a fixed-frequency operation mode optimized for offline LED lighting. The integrated constant power function (patented by Infineon Techologies AG) and the frequency jitter enable high performance without investment of too much effort in stabilization of the system and filtering in terms of EMC.

A wide VCC range up to 26 V is provided by use of BiCMOS technology to cover changes in the auxiliary supply voltage if a CV/CC regulation is implemented on the secondary side.

Auto Restart Mode is entered in the case of overtemperature, VCC overvoltage, output open loop or overload and VCC undervoltage. If an open load event occurs, the device enters the so-called Floating Load Protection (FLP) mode to protect the LED against destruction. The dimensions of the transformer and the secondary diode can be reduced owing to the internal precise peak current limitation to yield greater cost efficiency.

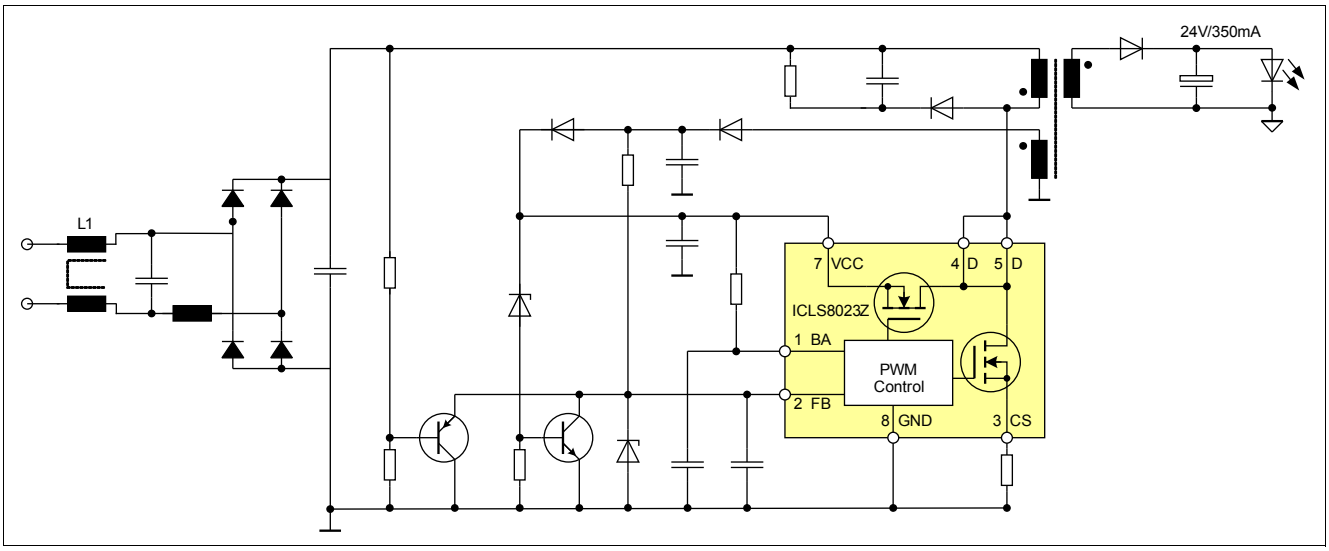


Figure 1 Typical application of ICLS8023Z controllers

Type	Package	Marking	V_{DS}	F_{OSC}	R_{DSon} [1]	230 VAC ± 15 % [2]	110 VAC ± 15 % [2]
ICLS8023Z	PG-DIP-7	ICLS8023Z	800 V	65 kHz	2.26 Ω	24 W	12 W

1) typ. @ T = 25 °C

2) Calculated maximum input power rating at T_a = 80 °C, T_j = 125 °C and without copper area as heat sink

1 Pin Configuration and Functionality

1.1 Pin Configuration for PG-DIP-7

Table 1 Pin Configuration for PG-DIP-7

Pin	Symbol	Function
1	BA	Extended blanking time & auto-restart enable
2	FB	Feedback
3	CS	Current Sense / 800 V[1)] depletion CoolMOS™ source
4	n.c.	Not connected
5	Drain	800 V[1)] CoolMOS™ drain
6	–	No pin
7	VCC	Controller supply voltage
8	GND	Controller ground

1) @ T_j = 110 °C

1.2 PG-DIP-7 Package

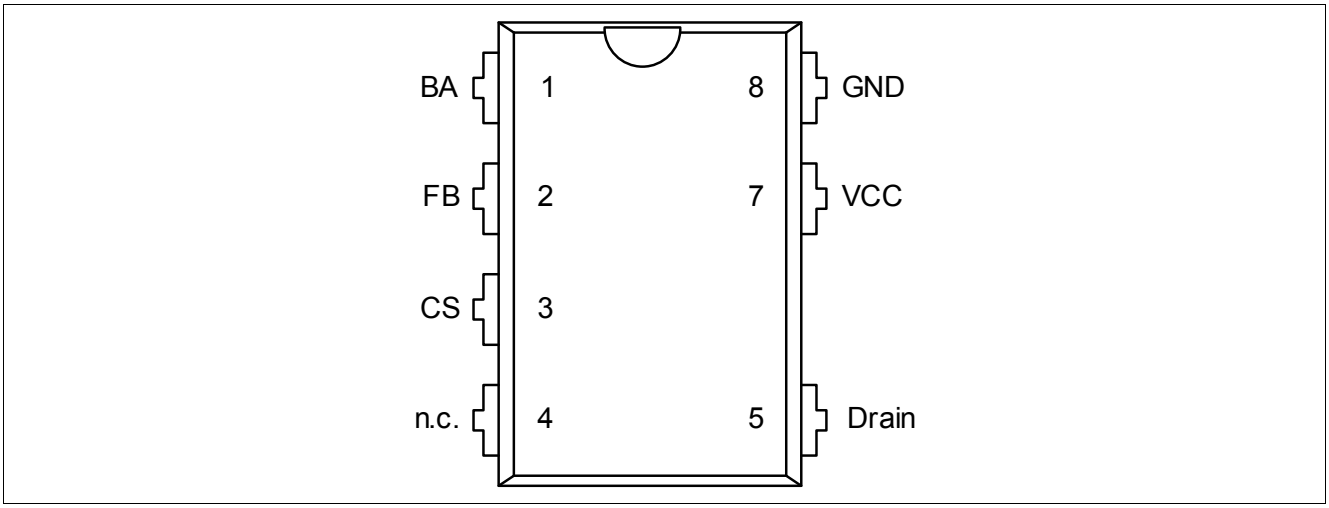


Figure 2 Pin configuration of PG-DIP-7 (top view)

1.3 Pin Functionality

BA (extended blanking time & auto-restart enable)

The BA pin combines the functions of extendable blanking time for overload protection and the external auto-restart enable. The extendable blanking time function is to extend the built-in 20 ms blanking time for overload protection by adding an external capacitor to ground. The external auto-restart enable function is an external access to stop the gate switching and force the IC to enter auto-restart mode. It is triggered by pulling the pin voltage to less than 0.4 V.

FB (feedback)

The information on the regulation is provided by the FB pin to the internal protection unit and to the internal PWM comparator to control the duty cycle. In the event of an open load event, the device enters the Floating Load Protection (FLP) mode.

CS (current sense)

The current sense pin senses the voltage developed on the series resistor inserted into the source of the integrated depletion CoolMOS™. If CS reaches the internal threshold of the current limit comparator, the driver output is immediately switched off. The current information is provided to the PWM comparator to realize the current mode.

Drain (drain of integrated depletion CoolMOS™)

The drain pin provides the connection to the drain of the internal depletion CoolMOS™.

VCC (power supply)

The VCC pin is the positive supply of the IC. The operating range of the supply is between 10.5 V and 25 V.

GND (ground)

The GND pin is the common ground of the controller.

2 Block Diagram

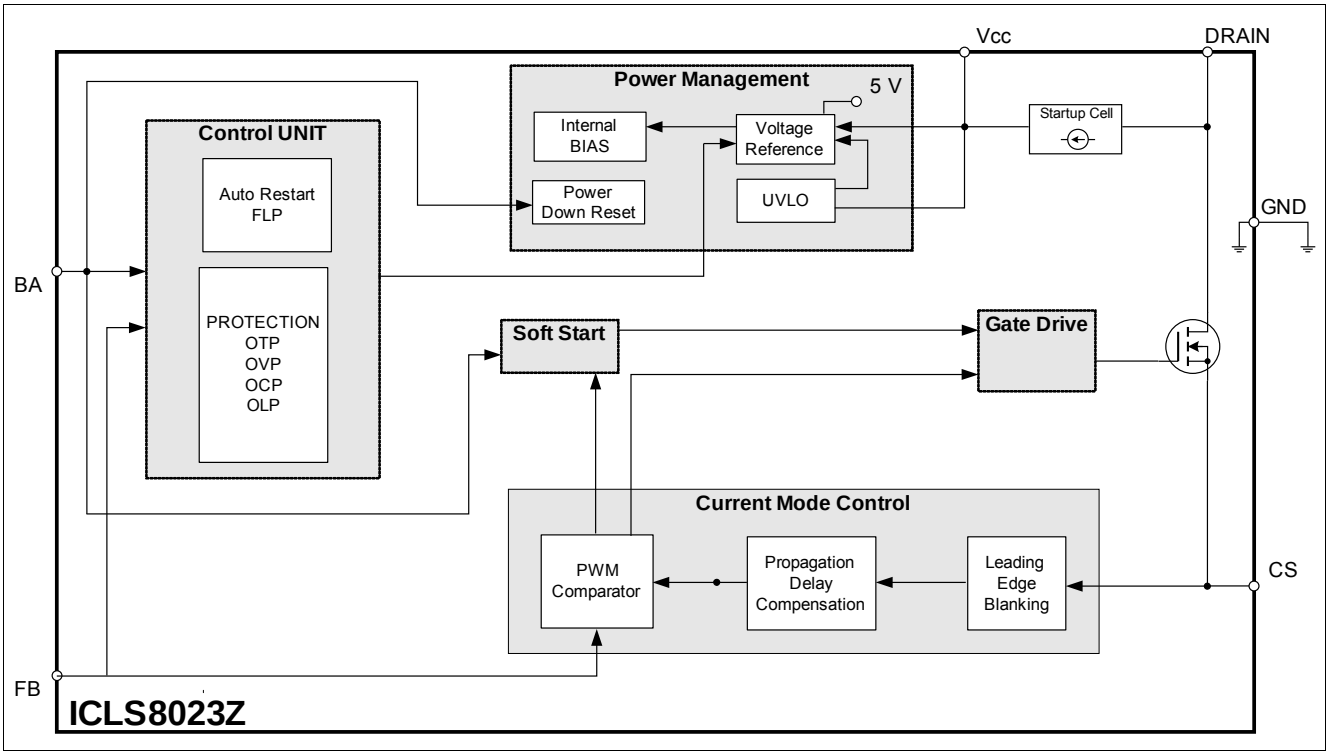


Figure 3 Block diagram of ICLS8023Z controllers

3 Functional Description

All values used in the functional description are typical values. When calculating the worst cases, the minimium/maximum values listed in **Electrical Characteristics** on page **32** have to be considered.

3.1 Introduction

For ICLS8023Z controllers, a high voltage startup cell is integrated into the system IC, which is switched off once the undervoltage lockout-on threshold of 17 V is exceeded. This startup cell is part of the integrated depletion CoolMOS™. The external startup resistor is no longer necessary as the startup cell is connected to the drain, resulting in reduced power losses. This increases the efficiency under light load conditions drastically.

The soft start capacitor is also used for providing an adjustable blanking window for high load jumps. The overload detection function is disabled during this window. With this concept, no further external components are necessary to adjust the blanking window.

An Auto Restart mode is implemented in the IC to reduce the average power conversion in the event of malfunction or unsafe operating conditions in the LED drives. This feature increases the system's robustness and safety, which would otherwise lead to a destruction of the LED drive. Once the malfunction is corrected, normal operation is automatically initiated after the next startup phase.

Together with the soft start capacitor, the feedback can also sense a missing load, which leads to rising output and auxiliary voltages. This triggers the Floating Load Protection (FLP) mode. When feedback falls below 1.35 V, the Soft Start voltage begins to rise up to a threshold of 4 V (depends on the C4 value) and the IC is switched into FLP mode.

The precise internal peak current limitation reduces the costs for the transformer and the secondary diode. The influence of the change in the input voltage on the power limitation can be avoided together with the integrated Propagation Delay Compensation circuit. Consequently, the maximum power is practically independent of the input voltage required for wide range LED drives. There is no need for additional oversizing of the LED drives – e.g., for the transformer or the secondary diode.

3.2 Power Management

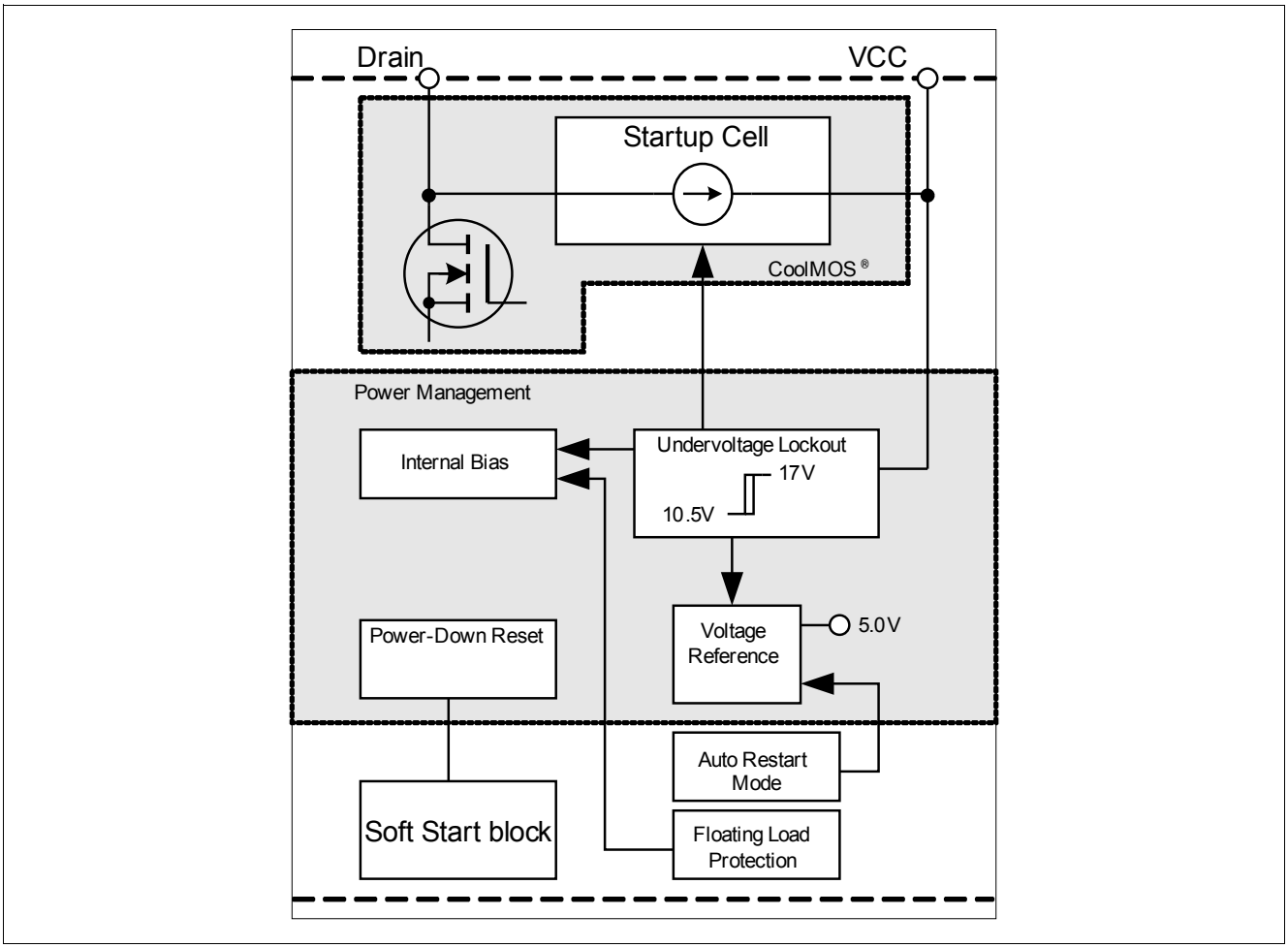


Figure 4 Power management of ICLS8023Z controllers

The undervoltage lockout function monitors the external supply voltage V_{VCC}. When the LED drive is connected to the main line, the internal startup cell is biased and starts to charge the external capacitor C_{VCC}, which is connected to the VCC pin. The VCC charge current that is provided by the startup cell from the drain pin is 0.9 mA. If V_{VCC} exceeds the on-threshold V_{CCon} (= 17 V), the bias circuit is switched on. Then the startup cell is switched off by the undervoltage lockout; therefore no power losses are present due to the connection of the startup cell to the drain voltage. An hysteresis loop is implemented to avoid uncontrolled ringing at switch-on. Switch-off of the controller can only take place after the active mode has been entered and V_{VCC} has fallen below 10.5 V.

The maximum current consumption before the controller is activated is about 200 µA.

If V_{VCC} falls below the off-threshold V_{CCoff} (= 10.5 V), the bias circuit is switched off and the soft start counter is reset. This ensures in every startup cycle that the soft start begins at zero.

The bias circuit is switched off if Auto Restart mode is entered. The current consumption is then reduced to 320 µA.

Once the malfunction condition is resolved, this block will then turn back on. The recovery from Auto Restart mode does not require disconnection of the LED drive from the AC line.

When Floating Load Protection (LFP) is entered, the internal bias is switched off most of the time but the voltage reference is kept alive in order to reduce the current consumption below 620 µA.

3.3 Improved Current Mode

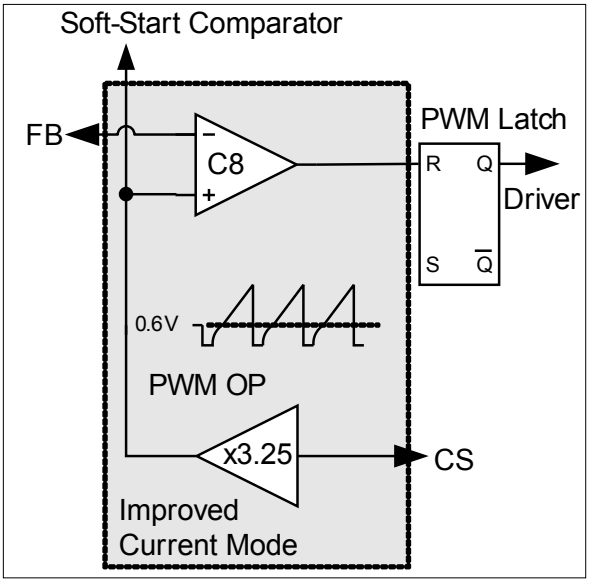


Figure 5 Current Mode

Current Mode means the duty cycle is controlled by the slope of the primary current. This is done by comparing the FB signal with the amplified current sense signal.

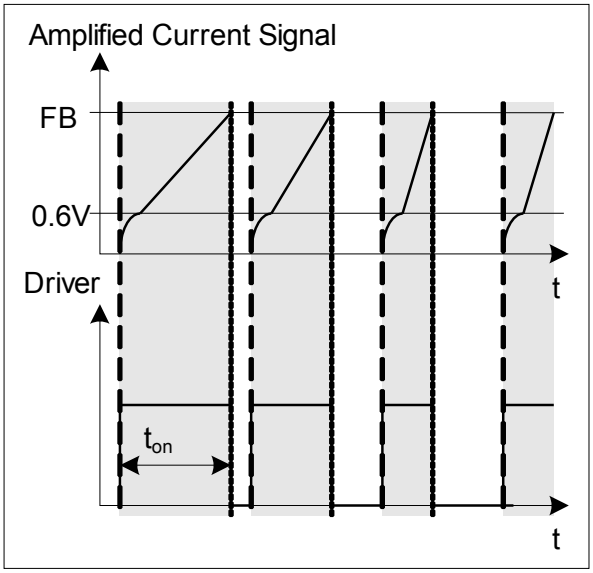


Figure 6 Pulse Width Modulation

If the amplified current sense signal exceeds the FB signal, the on-time t_{on} of the driver is finished by resetting the PWM latch (**Figure 6**).

The primary current is sensed by the external series resistor R_{Sense} inserted in the source of the integrated CoolMOS™. By means of current mode regulation, the secondary output voltage is insensitive to the line variations. The current waveform slope will change with the line variation, which controls the duty cycle.

The external R_{Sense} allows individual adjustment of the maximum source current of the integrated CoolMOS™.

To improve the current mode during light load conditions the amplified current ramp of the PWM-OP is superimposed on a voltage ramp, which is built by the switch T2, the voltage source V1 and a resistor R1 (see **Figure 7**). Every time the oscillator shuts down for maximum duty cycle limitation the switch T2 is closed by V_{OSC}. When the oscillator triggers the gate driver, T2 is opened so that the voltage ramp can start.

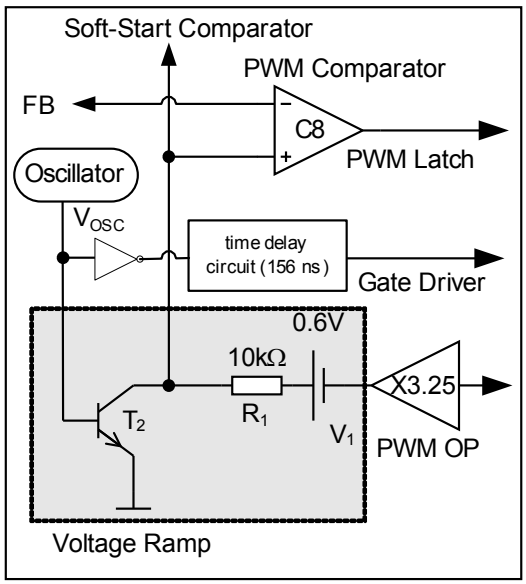


Figure 7 Improved Current Mode

In the case of light loads the amplified current ramp is too small to ensure stable regulation. In such cases the voltage ramp is a well-defined signal for the comparison with the FB signal. The duty cycle is then controlled by the slope of the voltage ramp.

By means of the time delay circuit which is triggered by the inverted V_{OSC} signal, the gate driver is switched off until it reaches approximately a 156 ns delay time (**Figure 8**). It allows the duty cycle to be reduced continuously to 0 % by decreasing V_{FB} below that threshold.

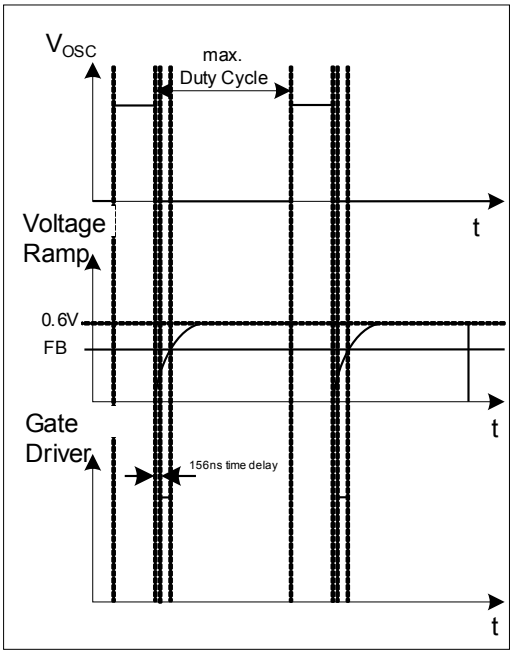


Figure 8 Light Load Conditions

3.3.1 PWM-OP

The input of the PWM-OP is applied over the internal leading edge blanking to the external sense resistor R_{Sense} connected to the CS pin. R_{Sense} converts the source current into a sense voltage. The sense voltage is amplified with a gain of 3.25 by the PWM-OP. The output of the PWM-OP is connected to the voltage source V1. The voltage ramp with the superimposed amplified current signal is fed into the positive inputs of the PWM comparator C8 and the soft start comparator (**Figure 9**).

3.3.2 PWM Comparator

The PWM comparator compares the sensed current signal of the integrated CoolMOS™ with the feedback signal V_{FB} (**Figure 9**). V_{FB} is created by an external optocoupler or external transistor in combination with the internal pull-up resistor R_{FB} and provides the load information of the feedback circuitry. When the amplified current signal of the integrated CoolMOS™ exceeds the signal V_{FB} the PWM comparator switches off the gate driver.

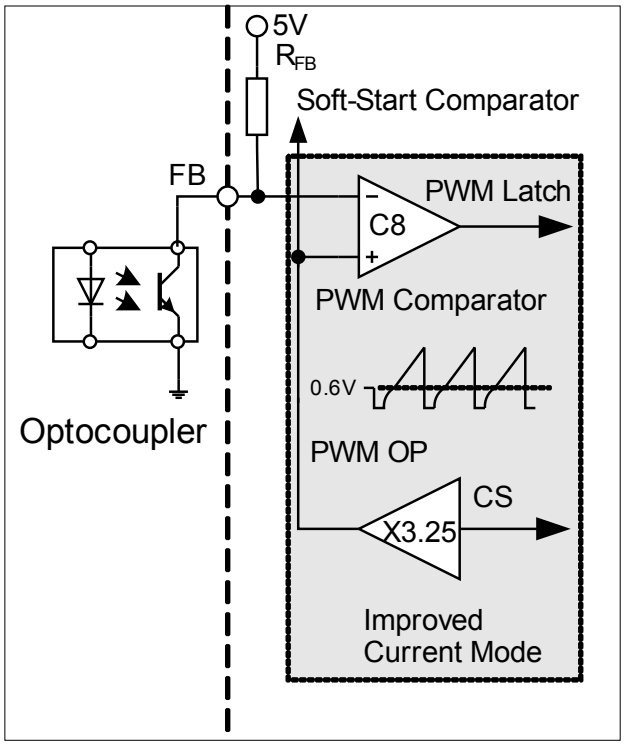


Figure 9 PWM Controlling

3.3.3 Startup Phase

In the startup phase, the IC provides a soft start period to control the primary current by means of a duty cycle limitation. The soft start function is a built-in function and it is controlled by an internal counter.

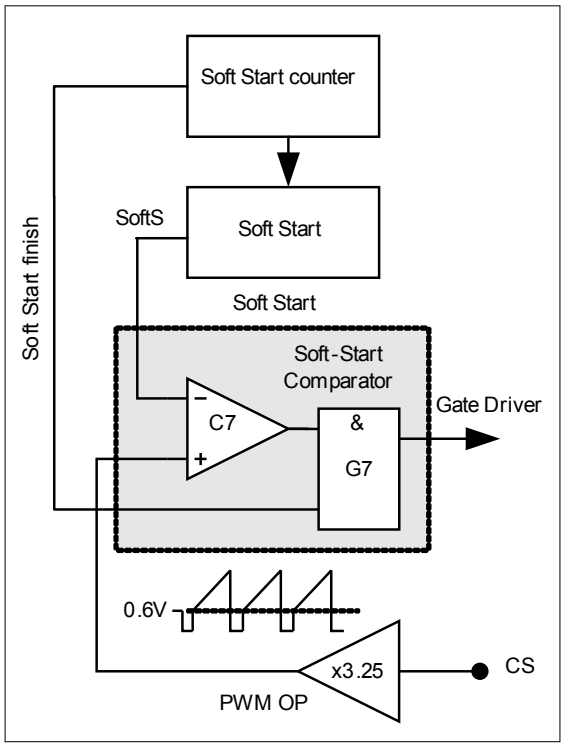


Figure 10 Soft Start

When the V_{CC} exceeds the on-threshold voltage, the IC starts the soft start mode (**Figure 11**).

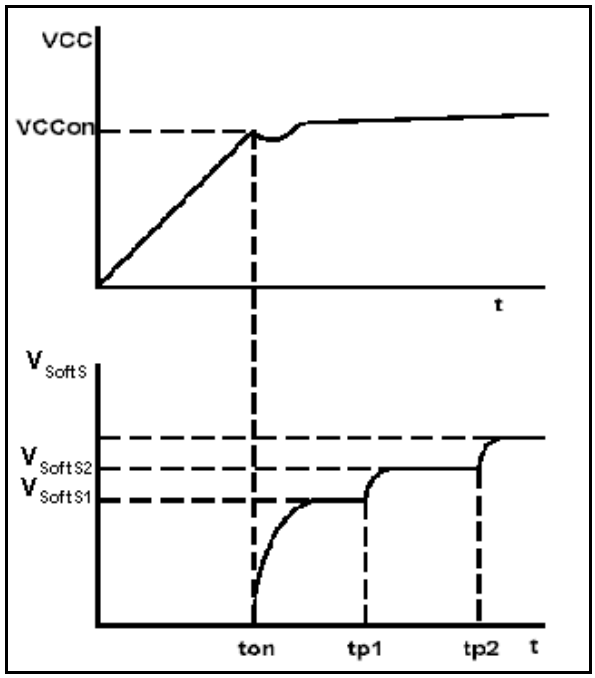


Figure 11 Soft Start Phase

The function is realized by an internal soft start resistor, a current sink and a counter. The amplitude of the current sink is controlled by the counter (**Figure 12**).

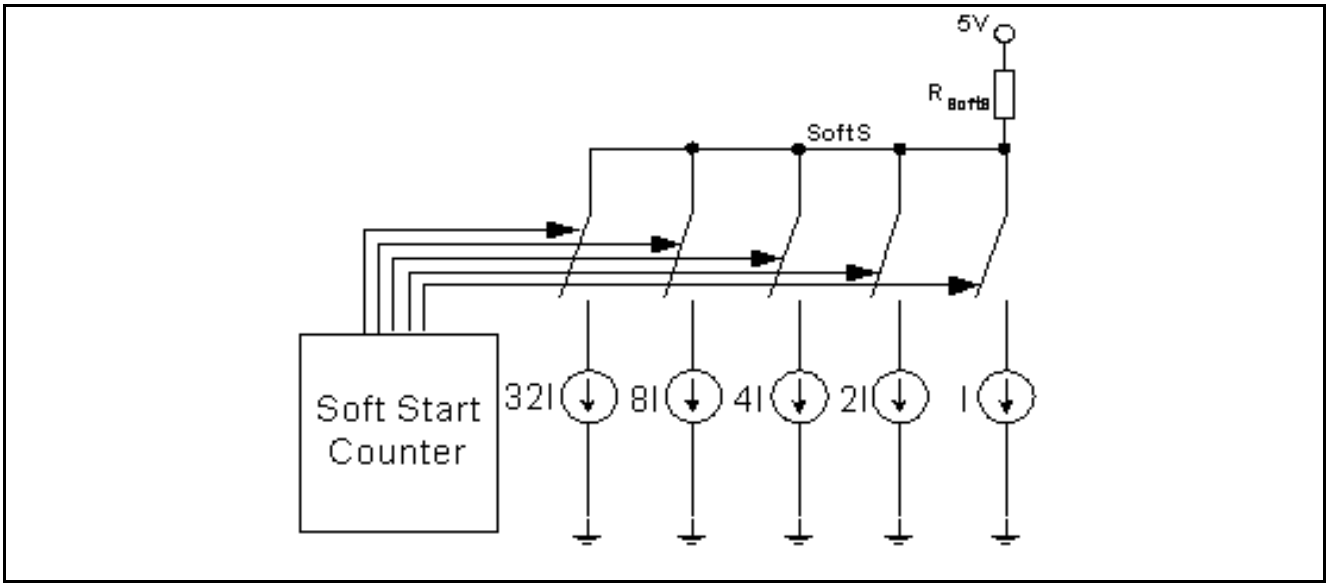


Figure 12 Soft Start Circuit

After the IC is switched on, the V_{SoftS} voltage is controlled such that the voltage is increased step-by-step (in 32 steps) with the increase of the counts. The soft start counter sends a signal to the current sink control every 300 μs so that the current sink decreases gradually and the duty ratio of the gate drive increases gradually. The soft start is finished in 10 ms ($t_{Soft\text{-}Start}$) after the IC is switched on. At the end of the soft start period, the current sink is switched off.

Within the soft start period, the duty cycle increases from zero to maximum gradually (see **Figure 13**).

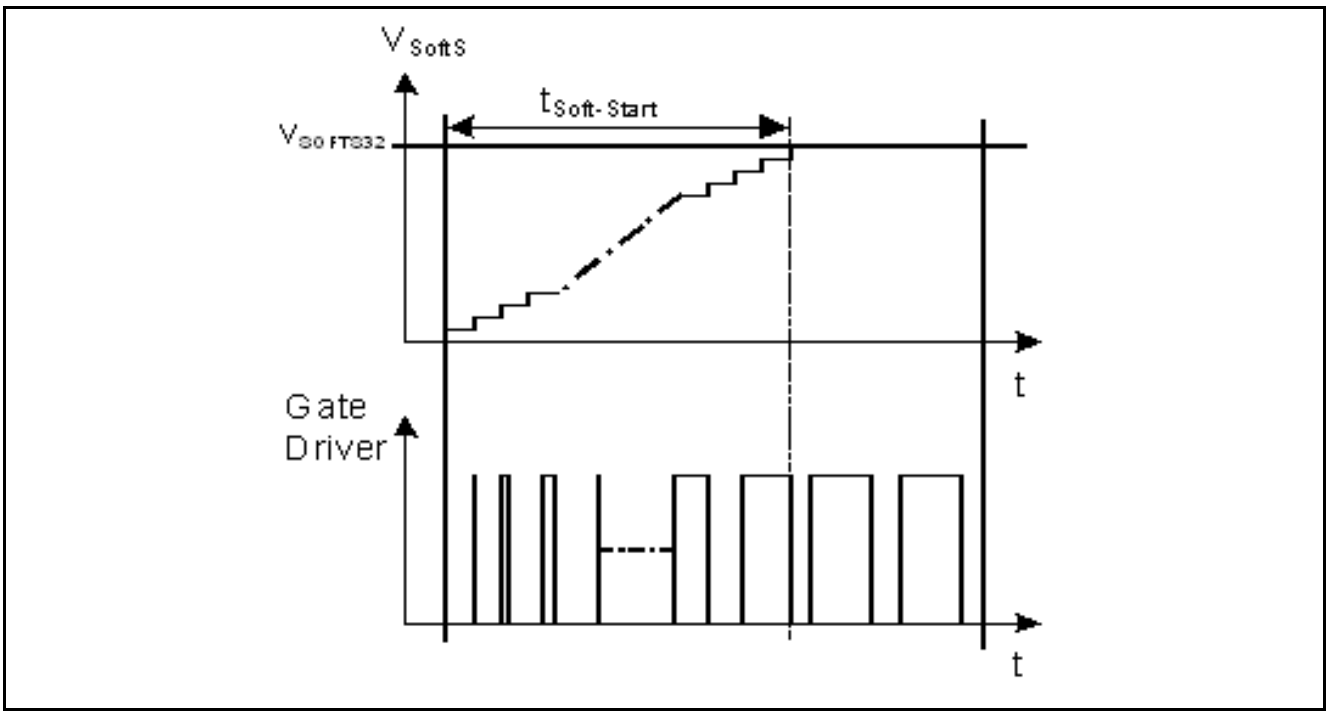


Figure 13 Gate Drive Signal in the Soft Start Phase

In addition to start-up, soft start is also activated at each restart attempt during auto restart.

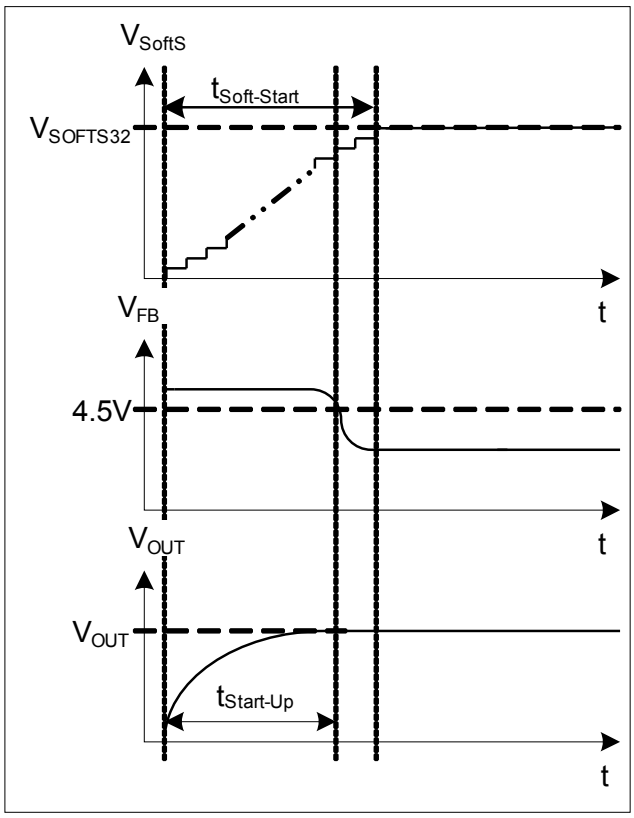


Figure 14 Start-Up Phase

The start-up time $t_{Start-Up}$ before the converter output voltage V_{OUT} is settled must be shorter than the soft start phase $t_{Soft-Start}$ (**Figure 14**). Soft start allows effective minimization of current and voltage stresses on the integrated CoolMOS™, the clamp circuit and the output rectifier and it helps to prevent saturation of the transformer during start-up.

3.4 PWM Section

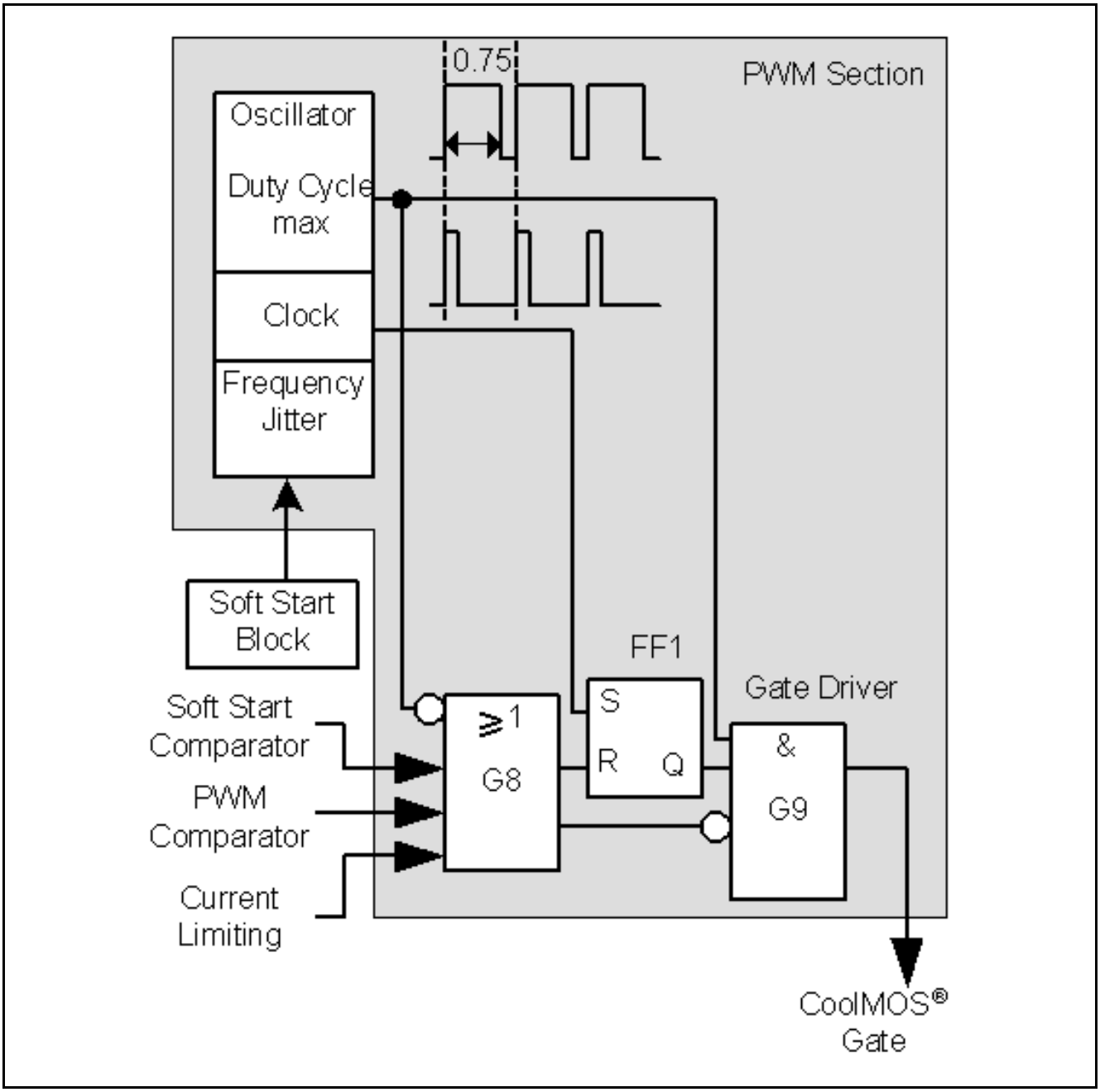


Figure 15 PWM Section Block

3.4.1 Oscillator

The oscillator generates a fixed frequency of 65 kHz with frequency jittering of ± 4 % (which is ± 2.6 kHz) at a jittering period of 4 ms.

A capacitor, a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum duty cycle limitation of D_{max} = 0.75.

Once the soft start period is over and when the IC goes into normal operating mode, the switching frequency of the clock is varied by the control signal from the soft start block. Then the switching frequency is varied in the range of 65 kHz ± 2.6 kHz at period of 4 ms.

3.4.2 PWM Latch FF1

The output of the oscillator block provides continuous pulses to the PWM latch, which turns on/off the integrated CoolMOS™. After the PWM latch is set, it is reset by the PWM comparator, the soft start comparator or the current limit comparator. When it is in reset mode, the output of the driver is shut down immediately.

3.4.3 Gate Driver

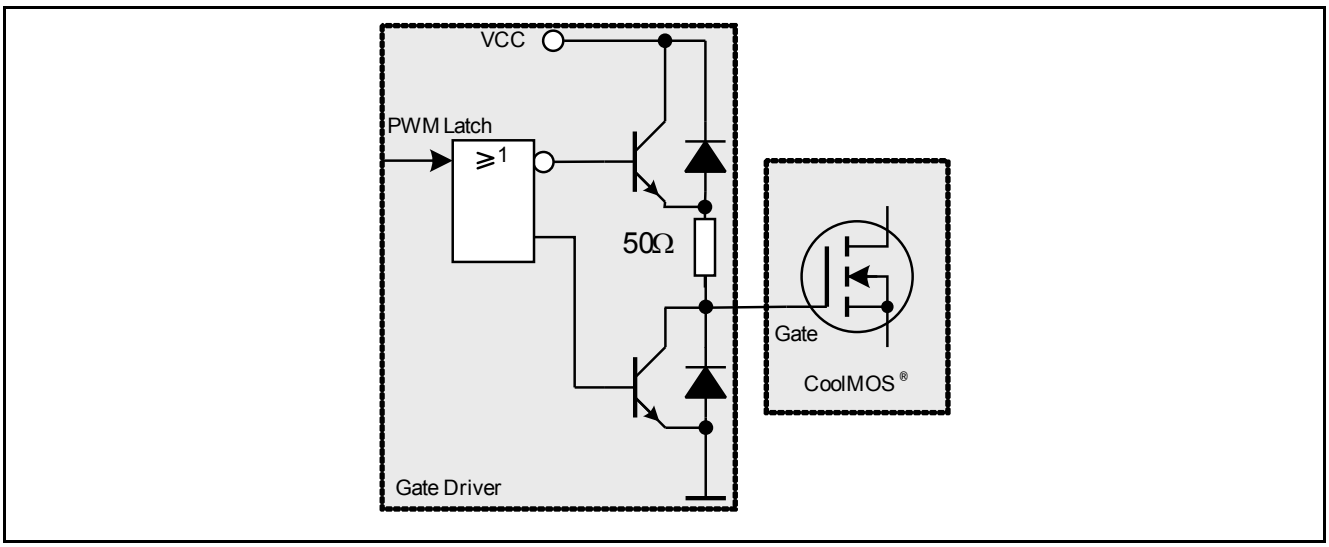


Figure 16 Gate Driver

The driver stage is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch-on slope when exceeding the integrated CoolMOS™ threshold. This is achieved by a slope control of the rising edge at the driver's output (**Figure 17**) and adding a 50 Ω gate turn-on resistor (**Figure 16**). Thus the leading switch-on spike is minimized.

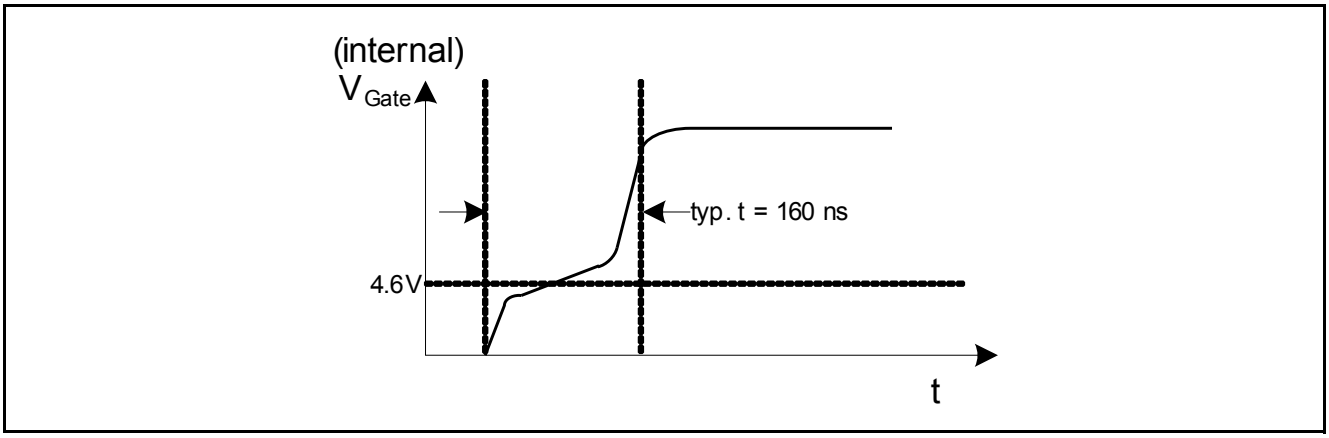


Figure 17 Gate Rising Slope

Furthermore the driver circuit is designed to eliminate cross conduction of the output stage.

During power-up, when V_{CC} is below the undervoltage lockout threshold V_{VCCoff}, the output of the gate driver is set to low in order to disable power transfer to the secondary side.

3.5 Current Limiting

A cycle-by-cycle peak current limiting operation is realized by the current limit comparator C10. The source current of the integrated CoolMOS™ is sensed via an external sense resistor R_{Sense}. By means of R_{Sense} the source current is transformed to a sense voltage V_{Sense}, which is fed to the pin CS. If the voltage V_{Sense} exceeds the internal threshold voltage V_{csth}, the comparator C10 immediately turns off the gate drive by resetting the PWM latch FF1.

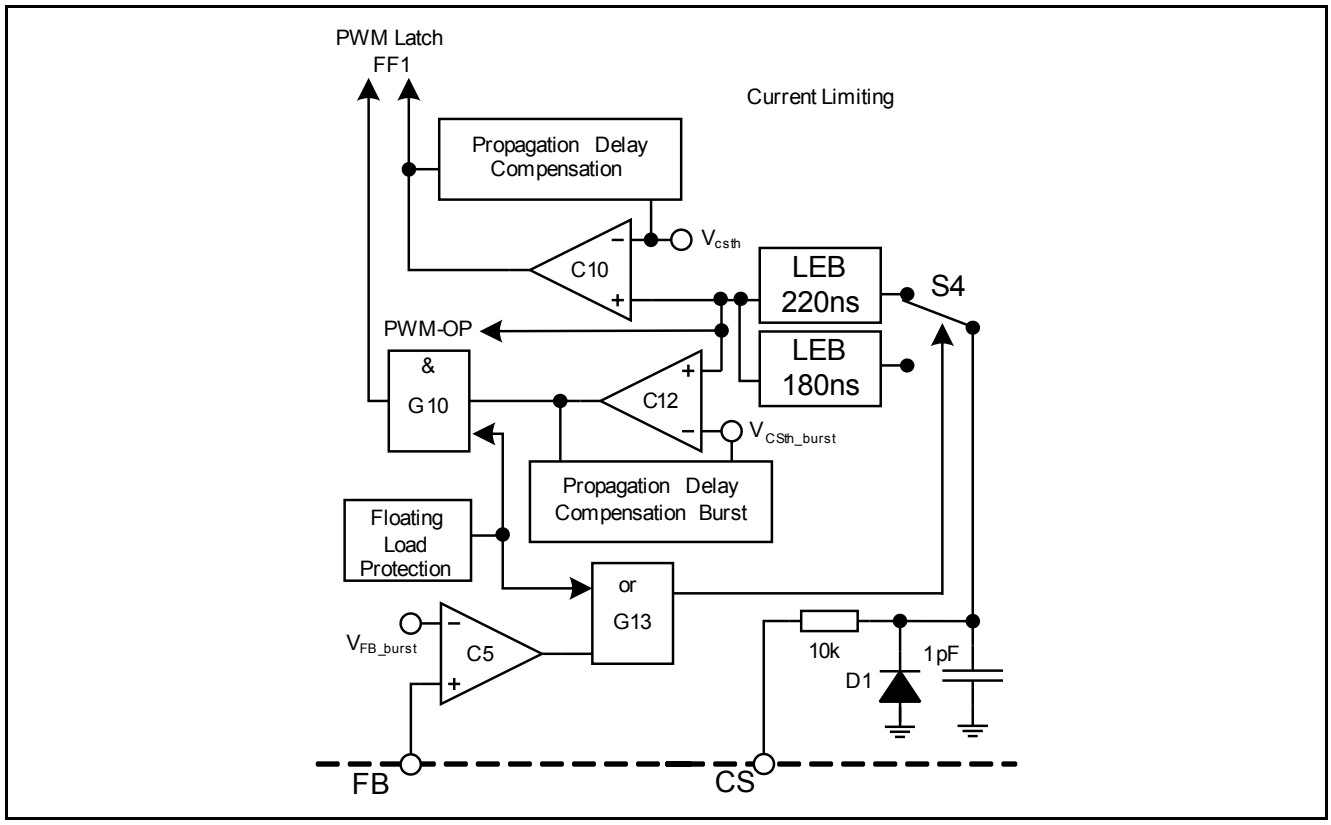


Figure 18 Current Limiting Block

Propagation delay compensation is added to support the immediate shutdown of the integrated CoolMOS™ with very short propagation delay. Thus the influence of the AC input voltage on the maximum output power can be reduced to a minimu. This compensation applies to both the peak load and burst mode.

In order to prevent the current limit from distortions caused by leading edge spikes, Leading Edge Blanking (LEB) is integrated into the current sense path for the comparators C10, C12 and the PWM-OP.

The output of comparator C12 is activated by the gate G10 if the FLP is entered. When it is activated, the current limiting is reduced to V_{csth_FLP}. This voltage level determines the maximum power level in Floating Load Protection mode.

3.5.1 Leading Edge Blanking

Whenever the integrated CoolMOS™ is switched on, a leading edge spike is generated due to the primary-side capacitances and reverse recovery time of the secondary-side rectifier. This spike can cause the gate drive to switch off unintentionally. In order to avoid premature termination of the switching pulse, this spike is blanked out with a time constant of t_{LEB} = 220 ns for normal load and t_{LEB} = 180 ns for FLP mode.

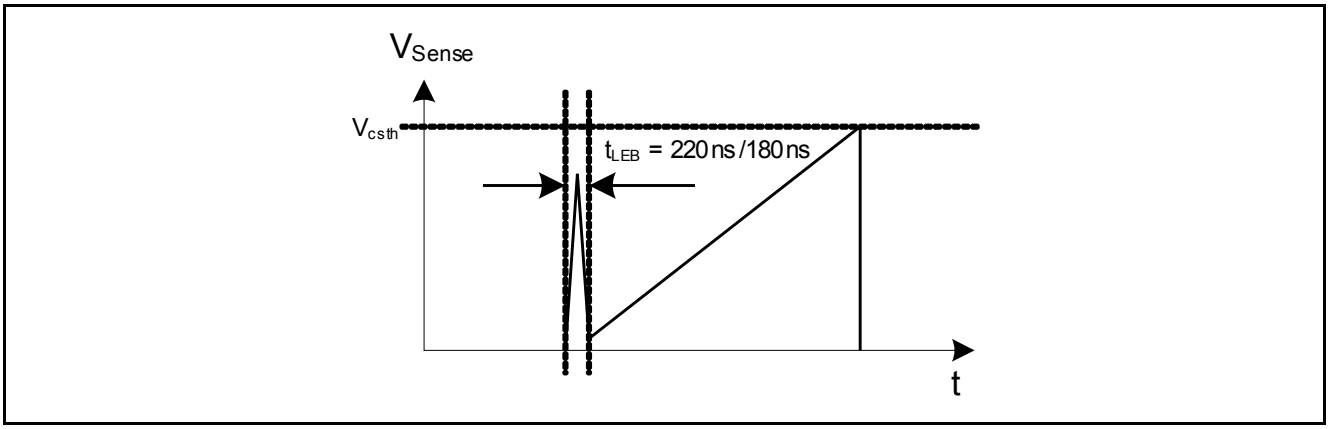


Figure 19 Leading Edge Blanking

3.5.2 Propagation Delay Compensation (patented)

In the case of overcurrent detection, there is always propagation delay to switch off the integrated CoolMOS™. An overshoot of the peak current I_{peak} is induced to the delay, which depends on the ratio of dI/dt of the peak current (**Figure 20**).

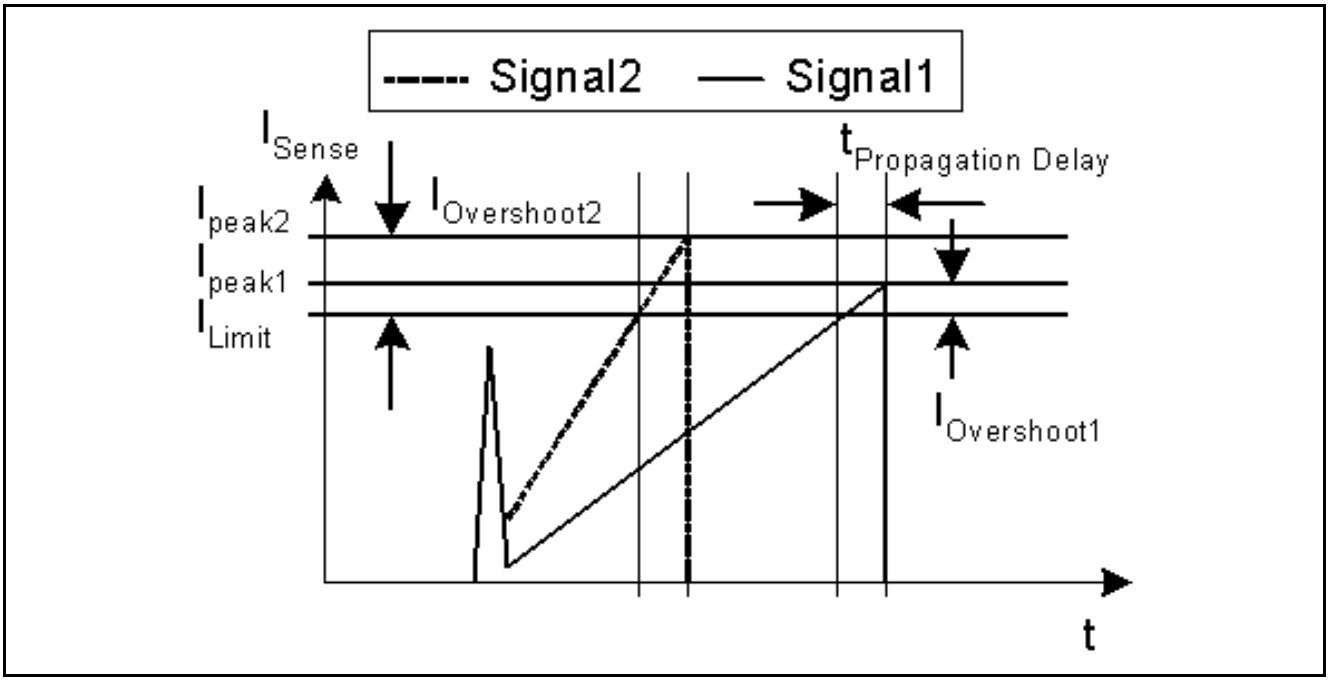


Figure 20 Current Limiting

The overshoot of Signal2 is larger than of Signal1 due to the steeper rising waveform. This change in the slope depends on the AC input voltage. Propagation Delay Compensation is integrated to reduce the overshoot due to dI/dt of the rising primary current. Thus the propagation delay time between exceeding the current sense threshold V_{csth} and the switching-off of the integrated CoolMOS™ is compensated over temperature within a wide input range. Current limiting is then very accurate.

For example, I_{peak} = 0.5 A with R_{Sense} = 2. The current sense threshold is set to a static voltage level V_{csth} = 1 V without Propagation Delay Compensation. A current ramp of dI/dt = 0.4 A/µs, or dV_{Sense}/dt = 0.8 V/µs, and a propagation delay time of $t_{Propagation\ Delay}$ = 180 ns leads to an I_{peak} overshoot of 14.4 %. With the propagation delay compensation, the overshoot is only around 2 % (**Figure 21**).

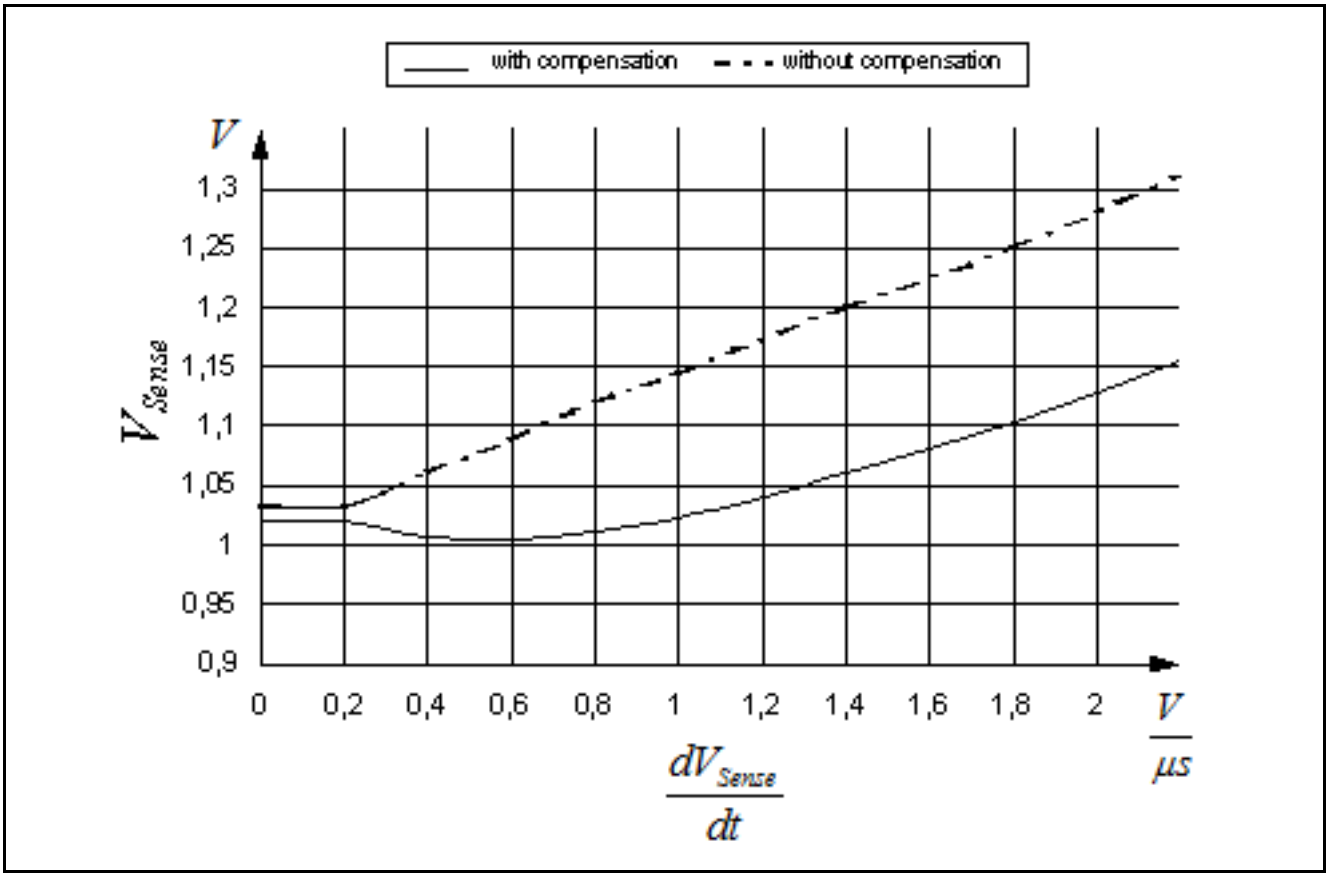


Figure 21 Overcurrent Shutdown

The Propagation Delay Compensation is realized by means of a dynamic threshold voltage V_{csth} (**Figure 22**). In case of a steeper slope the switch-off of the driver is earlier to compensate the delay.

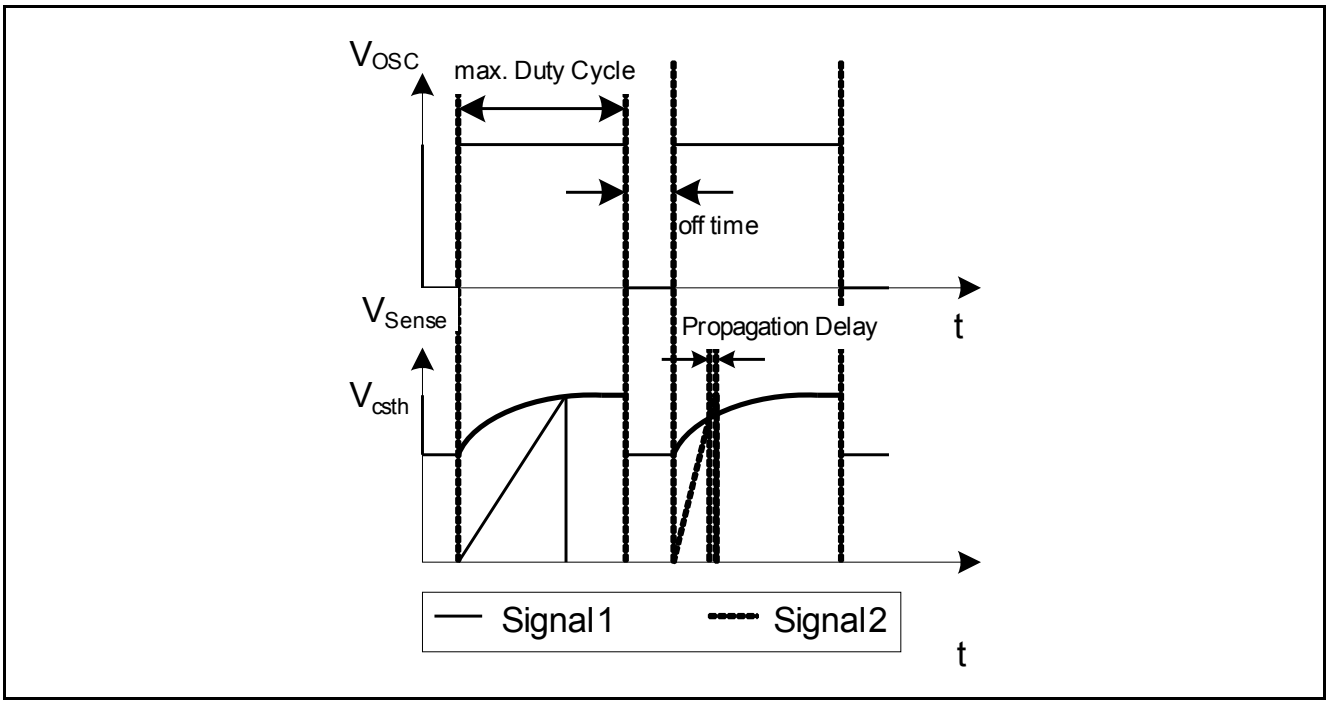


Figure 22 Dynamic Voltage Threshold V_{csth}

Similarly, the same concept of propagation delay compensation is also implemented in FLP mode with a reduced level, V_{csth_FLP} (**Figure 18**). With this implementation, the entry and exit FLP mode power can be very close between low line and high line input voltage.

3.6 Control Unit

The Control Unit contains the functions for Floating Load Protection (FLP) mode and Auto Restart mode. The FLP mode and the Auto Restart mode both have 20 ms internal blanking times. For the overload Auto Restart mode, the 20 ms blanking time can be further extended by adding an external capacitor at the BA pin. With the blanking time, the IC avoids entering into those two modes accidentally. This buffer time is very useful for the application, which works in short durations of peak power occasionally.

3.6.1 Basic and Extendable Blanking Mode

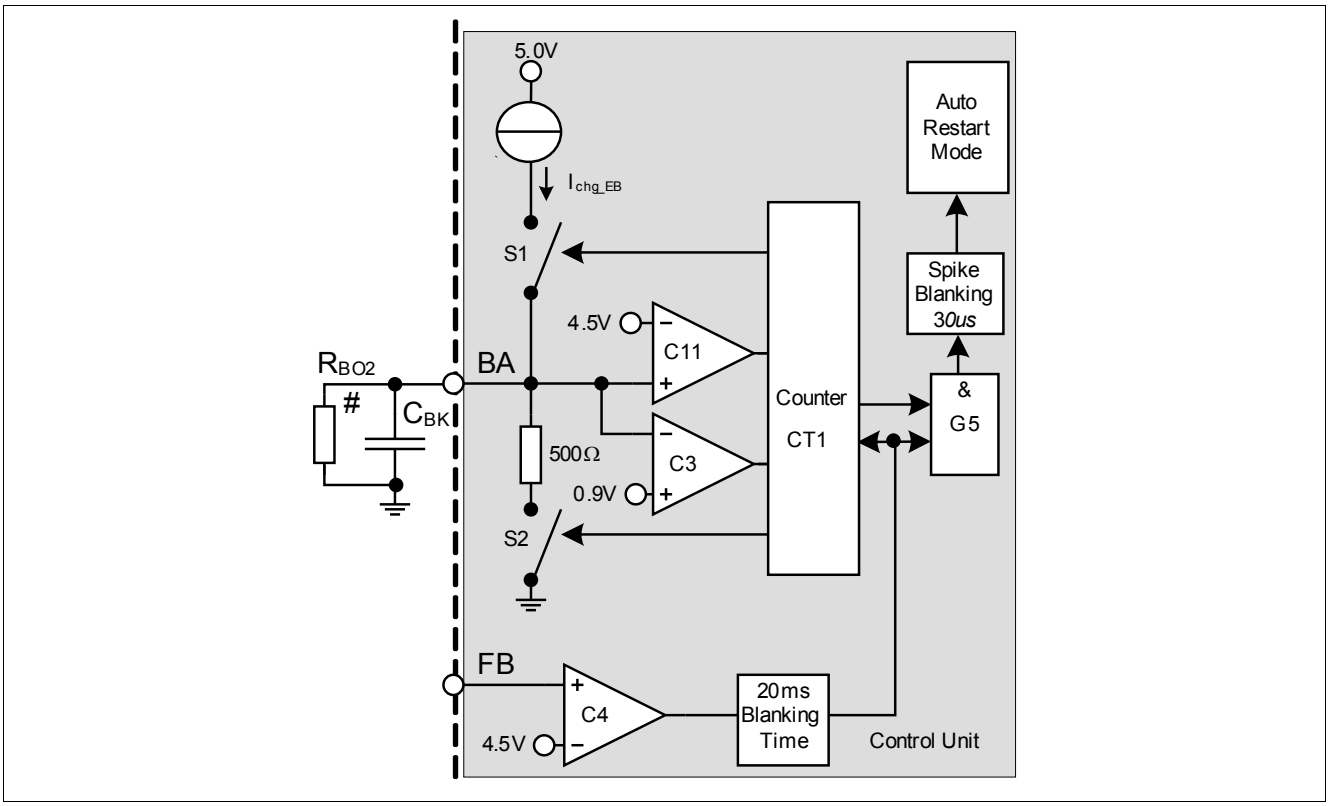


Figure 23 Basic and Extendable Blanking Mode

There are 2 kinds of blanking mode: basic mode and the extendable mode. The basic mode is a built-in 20 ms blanking time while the extendable mode can extend this blanking time by connecting an external capacitor to the BA pin. For the extendable mode, the gate G5 remains blocked even though the 20 ms blanking time is reached. After reaching the 20 ms blanking time the counter is activated and the switch S1 is turned on to charge the voltage of the BA pin by the constant current source, I_{chg_EB}. When the voltage of the BA pin hits 4.5 V, which is sensed by the comparator C11, the counter will increase the counter by 1. Then it switches off the switch S1 and turns on the switch S2. The voltage at the BA pin will be discharged through a 500 Ω resistor. When the voltage drops to 0.9 V, which is sensed by the comparator C3, the switch S2 will be turned off and the switch S1 will be turned on. Then the constant current I_{chg_EB} will charge the C_{BK} capacitor again. When the voltage at BA hits 4.5 V, which is sensed by comparator C11, the counter will increase the count to 2. The process repeats until it reaches a total count of 256 (**Figure 23**). Then the counter will release a high output signal. When the AND gate G5 detects both

high signals at the inputs, it will activate the 30 ms spike blanking circuit and finally the Auto Restart mode will be activated.

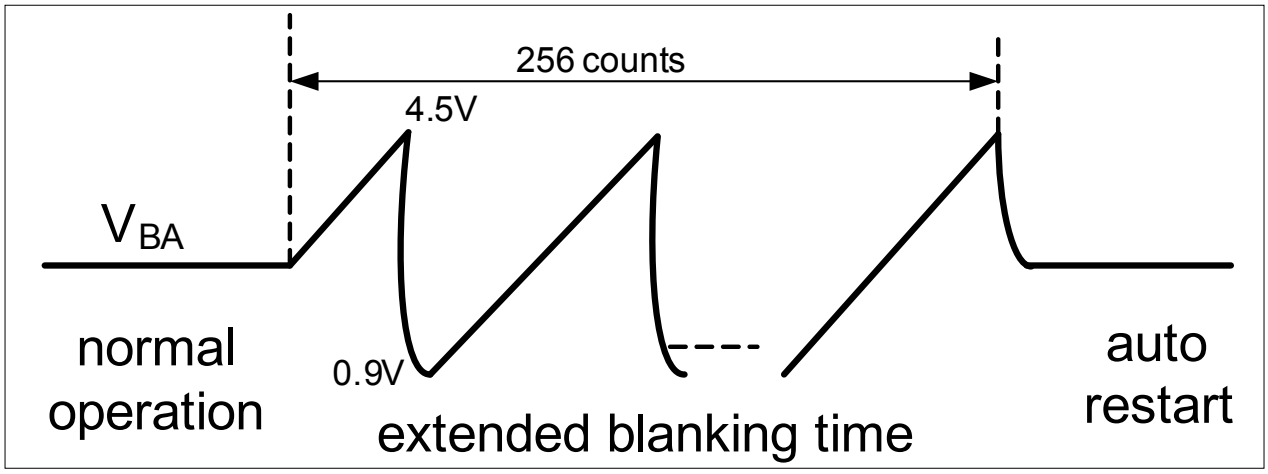


Figure 24 Waveform at Extended Blanking Time

For example, if C_{BK} = 0.1 µF, I_{chg_EB} = 720 µA

Extended blanking time =

256*(C_{BK}*(4.5V-0.9V)/I_{chg_EB} + C_{BK}*500*ln(4.5/0.9)) = 148.6 ms

Total blanking time = 20 ms+ 148.6 ms = 168.6 ms

If there is a resistor R_{BO2} connected to the BA pin, the effective charging current will be reduced. The blanking time will be increased.

For example, if C_{BK} = 0.1 µF, I_{chg_EB} = 720 µA, R_{BO2} = 12.8 KΩ,

I_{chg_EB}'= I_{chg_EB}-(4.5 V+0.9 V)/(2*R_{BO2}) = 509 µA

Extended blanking time =

256*(C_{BK}*(4.5V-0.9V)/I_{chg_EB}' + C_{BK}*500*ln(4.5/0.9)) = 201.6ms

Total blanking time = 20 ms + 201.6 = 221.6 ms

where I_{chg_EB}'=net charging current to C_{BK}

3.6.2 Floating Load Protection (FLP)

The circuit starts up as usual, but a missing load leads to a rise in the output and auxiliary voltages.

Reaching the VCC threshold of 24.5 V (voltage divider RD2/R4 and Q2) leads to a reduction in the feedback voltage and hence to reduced output current pulses in order to keep the output voltage below the maximum rating of the components. If the feedback level falls below 1.35 V, the Soft Start voltage begins to rise up to a threshold of 4 V (depends on the C4 value) and the IC is switched into the FLP mode.

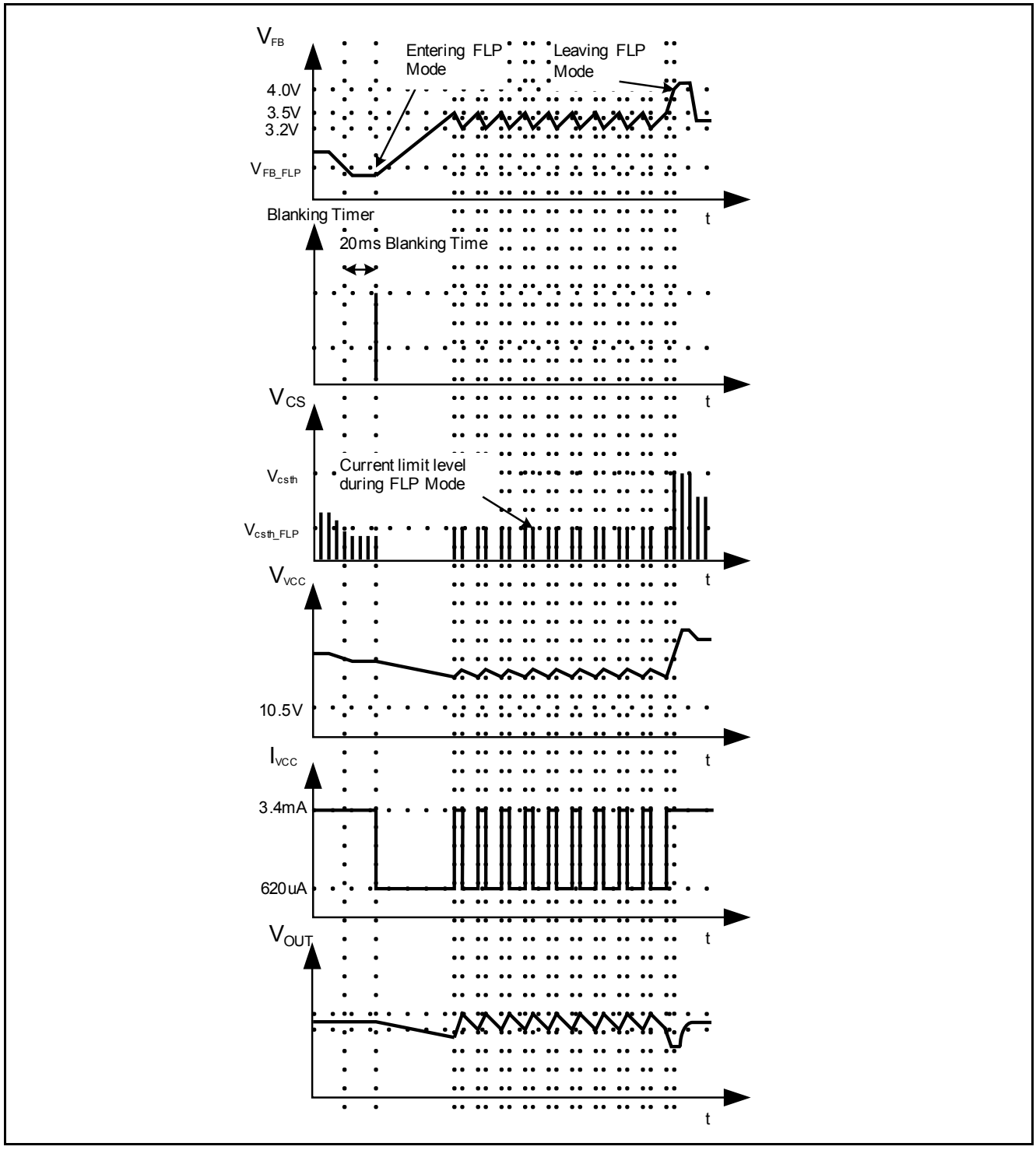


Figure 25 Signals in FLP Mode

3.6.3 Protection Modes

The IC provides Auto Restart mode as the major protection feature. Auto Restart mode can prevent destruction of the LED. There are 2 kinds of auto restart mode: odd skip auto restart mode and non switch auto restart mode. Odd skip auto restart mode is provided so there is no detection of faults and no switching pulse for the odd number restart cycle. On even numbers of restart cycles the fault detect and soft start switching pulses are maintained. If the fault persists, it continues the Auto Restart mode. However, if the fault is removed, it can release to normal operation only on the even number auto restart cycle (**Figure 26**).

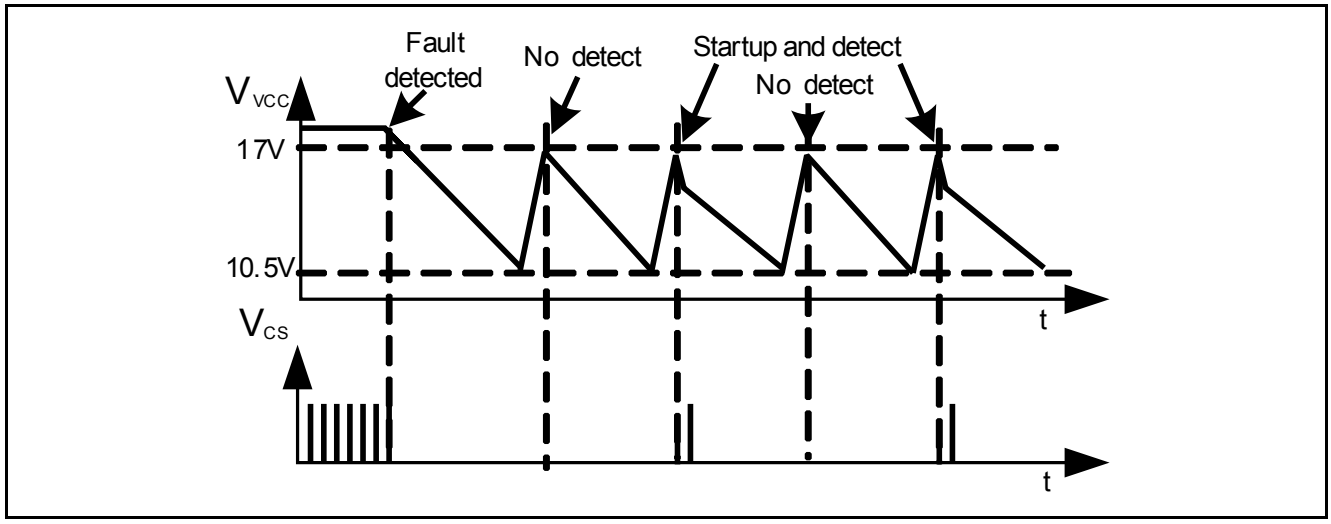


Figure 26 Odd Skip Auto Restart Waveform

Nonswitch auto restart mode is similar to odd skip auto restart mode except the start-up switching pulses are also suppressed on the even number of the restart cycle. The detection of faults still remains on even numbers of the restart cycle. When the fault is removed, the IC will resume normal operation on the even number of the restart cycle (**Figure 27**).

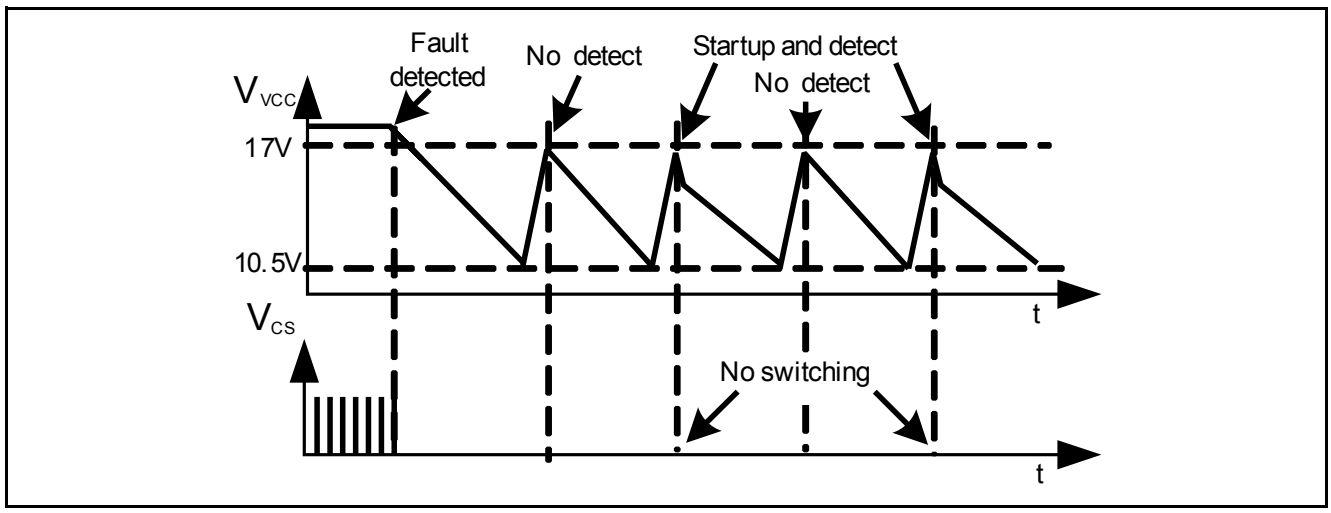


Figure 27 Nonswitch Auto Restart Waveform

The main purpose of the odd skip auto restart is to extend the restart time so that the power loss during auto restart protection can be reduced. This feature is particularly good for smaller Vcc capacitors where the restart time is shorter.

The following table lists the possible system failures and the corresponding protection modes:

VCC overvoltage (1)	Odd skip auto restart mode
VCC overvoltage (2)	Odd skip auto restart mode
Overload	Odd skip auto restart mode
Open loop	Odd skip auto restart mode
VCC undervoltage	Nonswitch auto restart mode
Short optocoupler	Nonswitch auto restart mode
Overtemperature	Nonswitch auto restart mode
External protection enable	Nonswitch auto restart mode

3.6.3.1 Vcc OVP, OTP, External Protection Enable and Vcc Undervoltage

There are 2 types of Vcc overvoltage protection: Vcc OVP (1) and Vcc OVP (2). The Vcc OVP (1) takes action only during the soft start period. The Vcc OVP (2) takes action in any condition.

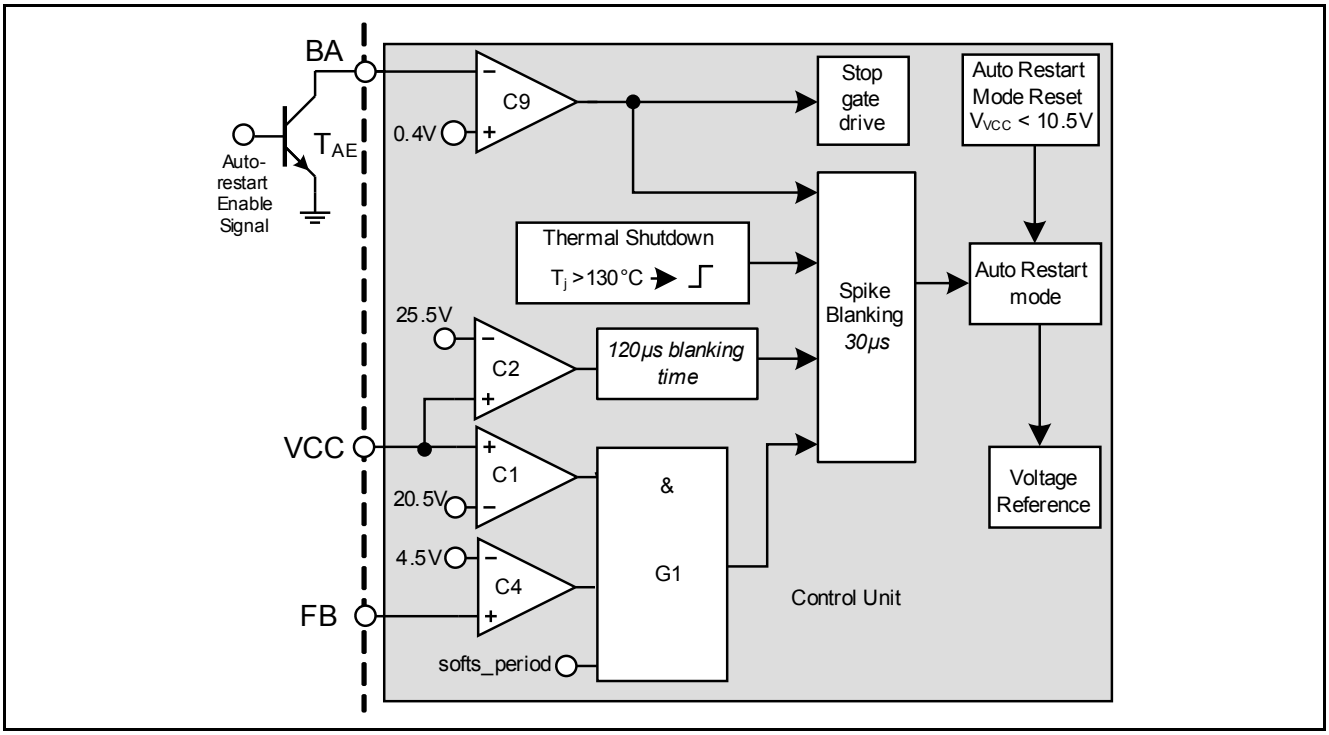


Figure 28 Vcc OVP, OTP, External Protection Enable

Vcc OVP (1) condition is when V_{VCC} voltage is > 20.5 V, V_{FB} voltage is > 4.5 V and during the soft start period, the IC enters into odd skip auto restart mode. This condition likely happens during start-up on an open loop fault (**Figure 28**).

Vcc OVP (2) condition is when V_{VCC} voltage is > 25.5 V, the IC enters into odd skip auto restart mode (**Figure 28**).

The overtemperature protection OTP is sensed inside the controller IC. The Thermal Shutdown block keeps on monitoring the junction temperature of the controller. After detecting a junction temperature higher than 130 °C, the IC will enter into the nonswitch auto restart mode. The IC is also implemented with a 50 °C hysteresis. This means the IC can only be recovered when the controller junction temperature is dropped 50 °C lower than the overtemperature trigger point (**Figure 28**).

The external auto restart enable feature can provide flexibility to a customer's self-defined protection feature. This function can be triggered by pulling down the V_{BA} voltage to < 0.4 V. Or it can simply trigger the base pin of an

external transistor, T_{AE} at the BA pin. When this function is enabled, it will enter into the nonswitch auto restart mode. The gate drive is stopped and there is no switching pulse before it is recovered (**Figure 28**).

The Vcc undervoltage and short opto-coupler will go into the nonswitch auto restart mode inherently.

In the case of V_{CC} undervoltage, the V_{CC} voltage drops indefinitely. When it drops below the V_{CC} undervoltage lockout “OFF” voltage (10.5 V), the IC will turn off the IC and the startup cell will turn on again. Then the V_{CC} voltage will be charged up to UVLO “ON” voltage (17 V) and the IC turns on again provided the startup cell charge-up current is not drained by the fault. If the fault is not removed, the V_{CC} will continue to drop until it hits UVLO “OFF” voltage and the restart cycle repeats.

Short optocoupler can lead to V_{CC} undervoltage because once the optocoupler (transistor side) is shorted, the feedback voltage will drop to zero and there will be no switching pulse. Then the V_{CC} voltage will drop the same as the V_{CC} undervoltage.

3.6.3.2 Overload Protection, Open Loop Protection

In overload or open loop cases, the V_{FB} voltage exceeds 4.5 V, which will be observed by comparator C4. Then the built-in blanking time counter starts to count. When it reaches 20 ms, the extended blanking time counter CT1 is activated. The switch S2 is turned on and the voltage at the BA pin will be discharged through a 500 Ω resistor. When it drops to 0.9 V, the switch S2 is turned off and the switch S1 is turned on. Then a constant current source I_{chg_EB} will start to charge up the BA pin. When the voltage hits 4.5 V, which is monitored by the comparator C11, the switch S1 is turned off and the count will increase by 1. Then the switch S2 will turn on again and the voltage will drop to 0.9 V and rise to 4.5 V again. The count will then increase by 1 again. When the total count reaches 256, the counter CT1 will stop and it will release a high output signal. When both the input signals at AND gate G5 is high, the odd skip auto restart mode is activated after the 30 µs spike blanking time (**Figure 29**).

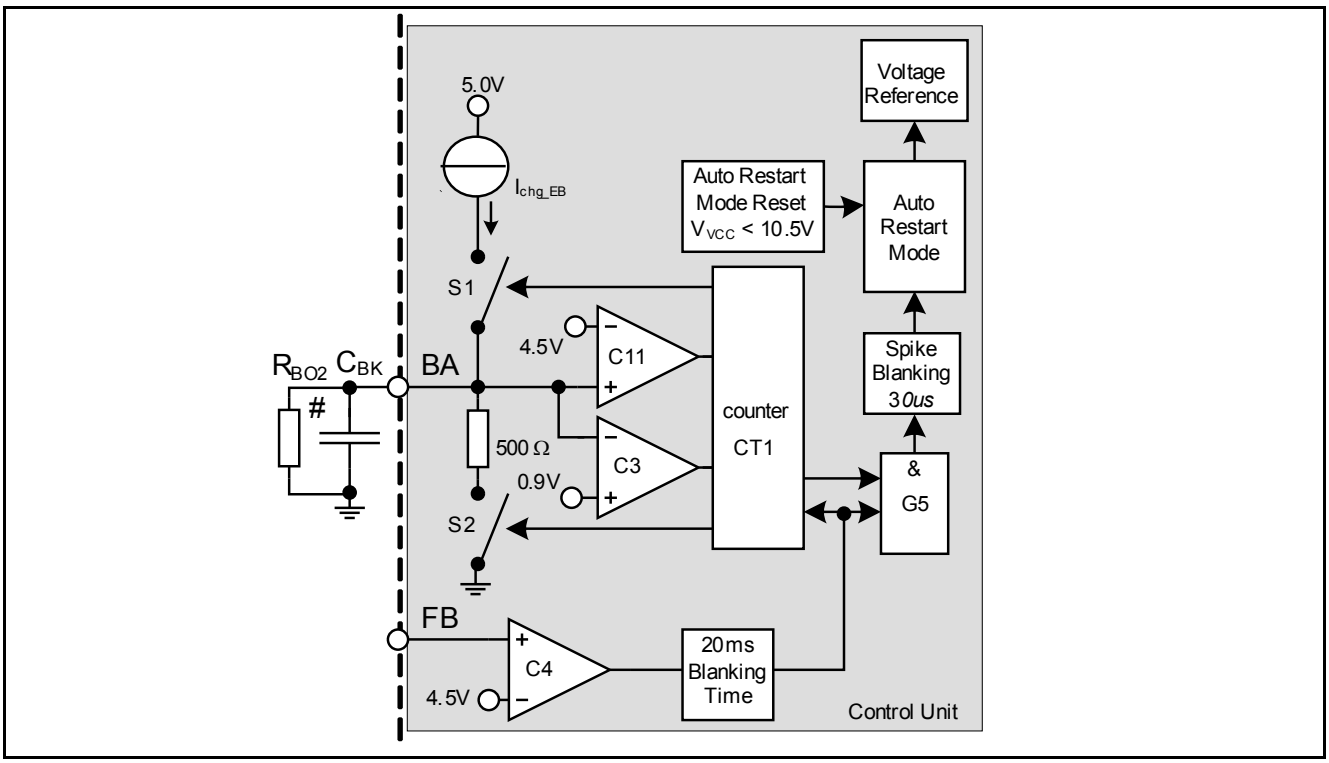


Figure 29 Overload Protection, Open Loop Protection

The total blanking time depends on the addition of the built-in and the extended blanking time. If there is no C_{BK} capacitor at the BA pin, the count will finish within 0.1 ms and the equivalent blanking time is just the built-in time

of 20 ms. However, if the C_{BK} capacitor is big enough, it can be as long as 1 s. If C_{BK} is 0.1 µF and I_{chg_EB} is 720 µA, the extendable blanking time is around 148.6 ms and the total blanking time is 168.6 ms.

Since the BA pin is a multifunction pin, it can share with different functions. The resistor R_{BO2} may however affect the extendable blanking time (**Figure 29**). Thus it should consider R_{BO2} in the calculation of the extendable blanking time. For example, the extended blanking time may be changed from 148.6 ms to 201.6 ms for cases with and without 12.8 KΩ R_{BO2} resistor. The list below shows one particular C_{BK}, R_{BO2} vs blanking time.

C_{BK}	RBO2	Extended blanking time	Overall blanking time
0.1 µF	–	148.6 ms	168.6 ms
0.1 µF	37.5 KΩ	162.8 ms	182.8 ms
0.1 µF	12.8 KΩ	201.6 ms	221.6 ms

Another factor to affect the extended blanking time is the input voltage through the R_{B01} and R_{B02}. It would, on the contrary, reduce the extended blanking time.

4 Electrical Characteristics

All voltages are measured in respect to ground (GND, pin 8). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Absolute maximum ratings are defined as ratings, which when exceeded may lead to destruction of the integrated circuit. For the same reason, ensure that any capacitor to be connected to pin 7 (VCC) is discharged before assembling the application circuit. T_a = 25 °C unless otherwise specified.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Drain/source voltage	V_{DS}	–	800	V	
Pulse drain current, t_p limited by max. T_j = 150 °C	I_{D_Puls}	–	4.9	A	
Avalanche energy, repetitive t_{AR} limited by max. T_j = 150 °C[1)]	E_{AR}	–	0.047	mJ	
Avalanche current, repetitive t_{AR} limited by max. T_j=150 °C[1)]	I_{AR}	–	1.5	A	
VCC supply voltage	V_{VCC}	-0.3	27	V	
FB voltage	V_{FB}	-0.3	5.5	V	
BA voltage	V_{BA}	-0.3	5.5	V	
CS voltage	V_{CS}	-0.3	5.5	V	
Junction temperature	T_j	-40	150	°C	Controller & CoolMOS™
Storage temperature	T_S	-55	150	°C	
Thermal resistance – junction, ambient	R_{thJA}	–	96	K/W	
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	–	260	°C	1.6 mm (0.063 in.) from case for 10 s
ESD capability (incl. drain pin)	V_{ESD}	–	2	kV	Human body model[2)]

1) Repetetive avalanche causes additional power losses that can be calculated as $P_{AV} = E_{AR} * f$

2) According to EIA/JESD22-A114-B (discharging a 100 pF capacitor through a 1.5 kΩ series resistor)

4.2 Operating Range

Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC supply voltage	V_{VCC}	V_{VCCoff}	25	V	Max. value limited due to Vcc OVP
Junction temperature of controller	T_{jCon}	–25	130	°C	Max. value limited due to thermal shutdown of controller
Junction temperature of CoolMOS™	$T_{JCoolMOS}$	–25	150	°C	

4.3 Characteristics

4.3.1 Supply Section

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from –25 °C to 125 °C. Typical values represent the median values, which are related to 25 °C. Unless otherwise stated, a supply voltage of VCC = 17 V is assumed.

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Startup current	$I_{VCCstart}$	–	200	300	µA	V_{VCC} = 16 V
VCC charge current	$I_{VCCcharge1}$			5.0	mA	V_{VCC} = 0 V
	$I_{VCCcharge2}$	0.55	0.9	1.60	mA	V_{VCC} = 1 V
	$I_{VCCcharge3}$	0.38	0.7	–	mA	V_{VCC} = 16 V
Leakage current of the startup cell & CoolMOS™	$I_{StartLeak}$	–	0.2	50	µA	V_{Drain}= 650 V at T_j = 100 °C[1)]
Supply current with inactive gate	$I_{VCCsup1}$	–	1.9	3.2	mA	
Supply current with active gate	$I_{VCCsup2}$	–	3.1	4.8	mA	I_{FB} = 0 A
Supply current in Auto Restart mode with inactive gate	$I_{VCCrestart}$	–	320	–	µA	I_{FB} = 0 A
Supply current in Floating Load Protection (FLP) mode with inactive gate	$I_{VCCFLP1}$	–	620	950	µA	V_{FB} = 2.5 V
	$I_{VCCFLP2}$	–	620	950	µA	V_{CC} = 11.5 V, V_{FB} = 2.5 V
VCC turn-on threshold	V_{VCCon}	16.0	17.0	18.0	V	
VCC Turn-off threshold	V_{VCCoff}	9.8	10.56	11.2	V	
VCC Turn-on/off hysteresis	V_{VCChys}	–	6.5	–	V	

1) The parameter is not subjected to production testing; it is verified by design/characterization

4.3.2 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Trimmed reference voltage	V_{REF}	4.90	5.00	5.10	V	Measured at pin FB, I_{FB} = 0 A

4.3.3 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Fixed oscillator frequency	f_{OSC1}	56.5	65	73.4	kHz	
	f_{OSC2}	58.2	65	70.2	kHz	T_j = 25 °C
Frequency jittering range	f_{jitter}	–	± 2.6	–	kHz	T_j = 25 °C
Frequency jittering period	t_{jitter}	–	4.0	–	ms	T_j = 25 °C
Max. duty cycle	D_{max}	0.70	0.75	0.80		
Min. duty cycle	D_{min}	0	–	–		V_{FB} < 0.3 V
PWM OP gain	A_V	3.05	3.25	3.45		
Voltage ramp offset	$V_{Offset-Ramp}$	–	0.6	–	V	
V_{FB} operating range, min. level	V_{FBmin}	–	0.7	–	V	
V_{FB} operating range, max. level	V_{FBmax}	–	–	4.3	V	CS=1V limited by comparator C4[1)]
Feedback pull-up resistor	R_{FB}	9.0	15.4	22.0	kΩ	

1) This parameter is not subject to production testing and is verified by design/characterization

4.3.4 Soft Start Time

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Soft start time	t_{SS}	–	10.0	–	ms	

4.3.5 Control Unit

Parameter		Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Blanking time voltage lower limit for comparator C3		V_{BKC3}	0.80	0.90	1.00	V	
Blanking time voltage upper limit for comparator C11		V_{BKC11}	4.28	4.50	4.72	V	
Overload limit for comparator C4		V_{FBC4}	4.28	4.50	4.72	V	
Entry FLP select high level for comparator C19		$V_{FBLPC19}$	4.28	4.50	4.72	V	
Entry FLP select low level for comparator C20		$V_{FBLPC20}$	0.40	0.50	0.60	V	
FLP mode entry level for comparator C5	10 % P_{in_max}	V_{FB_FLP1}	1.51	1.60	1.69	V	< 7 counts
	6.67 % P_{in_max}	V_{FB_FLP2}	1.34	1.42	1.50	V	8 ~ 39 counts
	4.38 % P_{in_max}	V_{FB_FLP3}	1.20	1.27	1.34	V	40 ~ 191 counts
FLP mode high level for comparator C6a		$V_{FBFLPC6a}$	3.35	3.50	3.65	V	In Floating Load Protection (FLP) mode
FLP mode low level for comparator C6b		$V_{FBFLPC6b}$	3.06	3.20	3.34	V	
FLP mode level for comparator C13		$V_{FBFLPC13}$	3.85	4.00	4.15	V	
Overvoltage detection limit for comparator C1		$V_{VCCOVP1}$	19.5	20.5	21.5	V	V_{FB} = 5 V, during soft start
Overvoltage detection limit for comparator C2		$V_{VCCOVP2}$	25.0	25.5	26.3	V	
Auto-restart enable reference voltage for comparator C9		V_{AE}	0.25	0.40	0.45	V	
Charging current for extended blanking time		I_{chg_EB}	480	720	864	µA	
Thermal shutdown[1)]		T_{jSD}	130	140	150	°C	Controller
Hysteresis for thermal shutdown[1)]		T_{jSD_hys}	-	50	-	°C	
Built-in blanking time for overload protection or enter FLP mode		t_{BK}	-	20	-	ms	
Time for entry FLP select		t_{EFLPS}	-	1	-	ms	
Spike blanking time for auto restart protection		t_{Spike}	-	30	-	µs	

1) The parameter is not subjected to production testing but is verified by design/characterization. The thermal shutdown temperature refers to the junction temperature of the controller.

Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except V_{VCCOVP} and V_{VCCPD}.

4.3.6 Current Limiting

Parameter		Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Peak current limitation (incl. propagation delay)		V_{csth}	0.99	1.06	1.13	V	dV_{sense} / dt = 0.6 V/µs (Figure 21)
Peak current limitation during Floating Load Protection mode	20 % P_{in_max}	$V_{csthFLP1}$	0.39	0.45	0.51	V	< 7 counts
	13.3 % P_{in_max}	$V_{csthFLP2}$	0.32	0.37	0.44	V	8 ~ 39 counts
	9.6 % P_{in_max}	$V_{csthFLP3}$	0.25	0.31	0.37	V	40 ~ 191 counts
Leading edge blanking	Normal mode	$t_{LEBnormal}$	–	220	–	ns	
	FLP mode	t_{LEB_FLP}	–	180	–	ns	
CS input bias current		I_{CSbias}	-1.5	-0.2	–	µA	V_{CS} = 0 V

4.3.7 CoolMOS™ Section

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Drain/source breakdown voltage	$V_{(BR)DSS}$	800 870	– –	– –	V V	T_j = 25 °C T_j = 110 °C[1]
Drain/source on resistance	R_{DSon}	– – –	2.26 5.02 6.14	2.62 5.81 7.10	Ω Ω Ω	T_j = 25 °C T_j = 125 °C[1] T_j = 150 °C[1] at I_D = 0.81 A
Effective output capacitance, energy-related	$C_{o(er)1}$	–	16.3	–	pF	V_{DS} = 0 V to 480 V
Rise time	t_{rise}	–	30[2]	–	ns	–
Fall time	t_{fall}	–	30[2]	–	ns	–

1) The parameter is not subject to production testing and is verified by design/characterization
2) Measured in a typical flyback converter application

5 CoolMOS™ Performance Characteristic

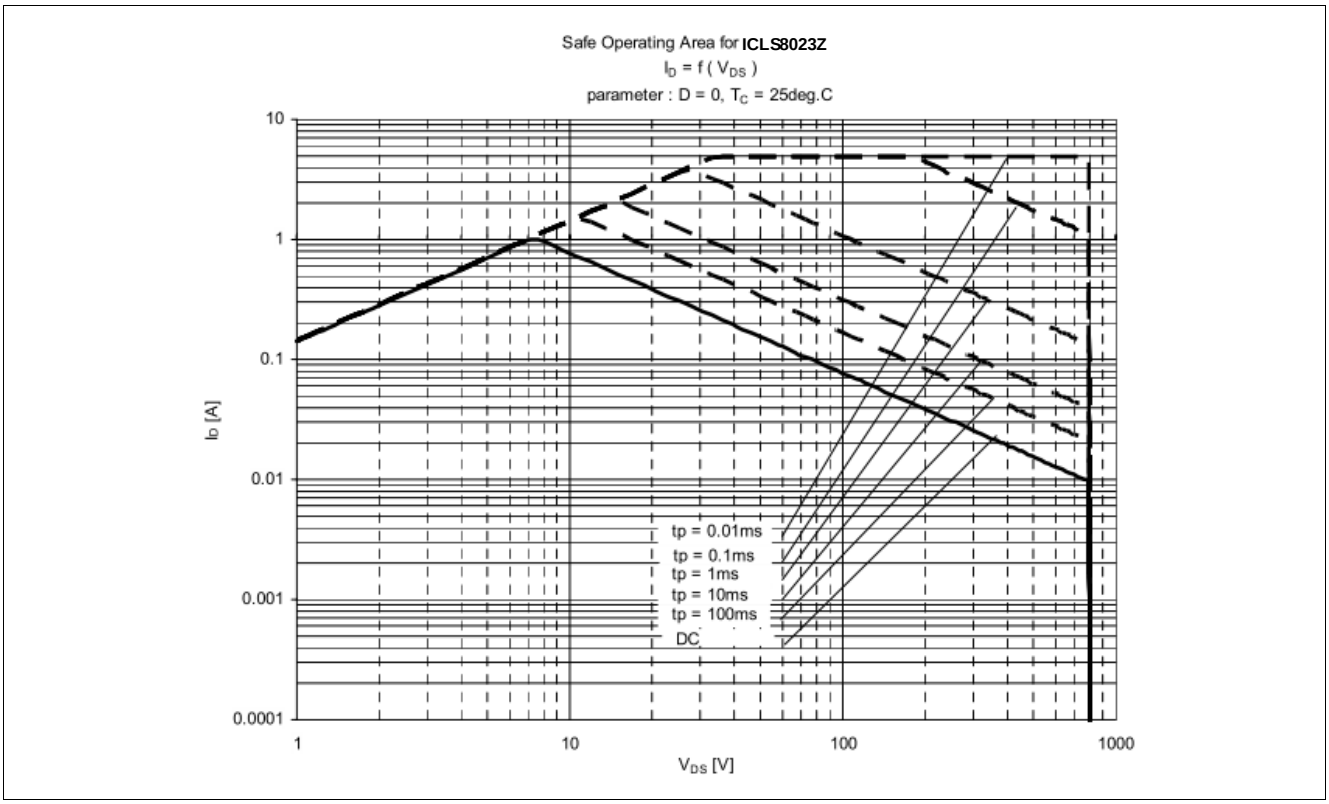


Figure 30 Safe Operating Area (SOA) curve for ICLS8023Z controllers

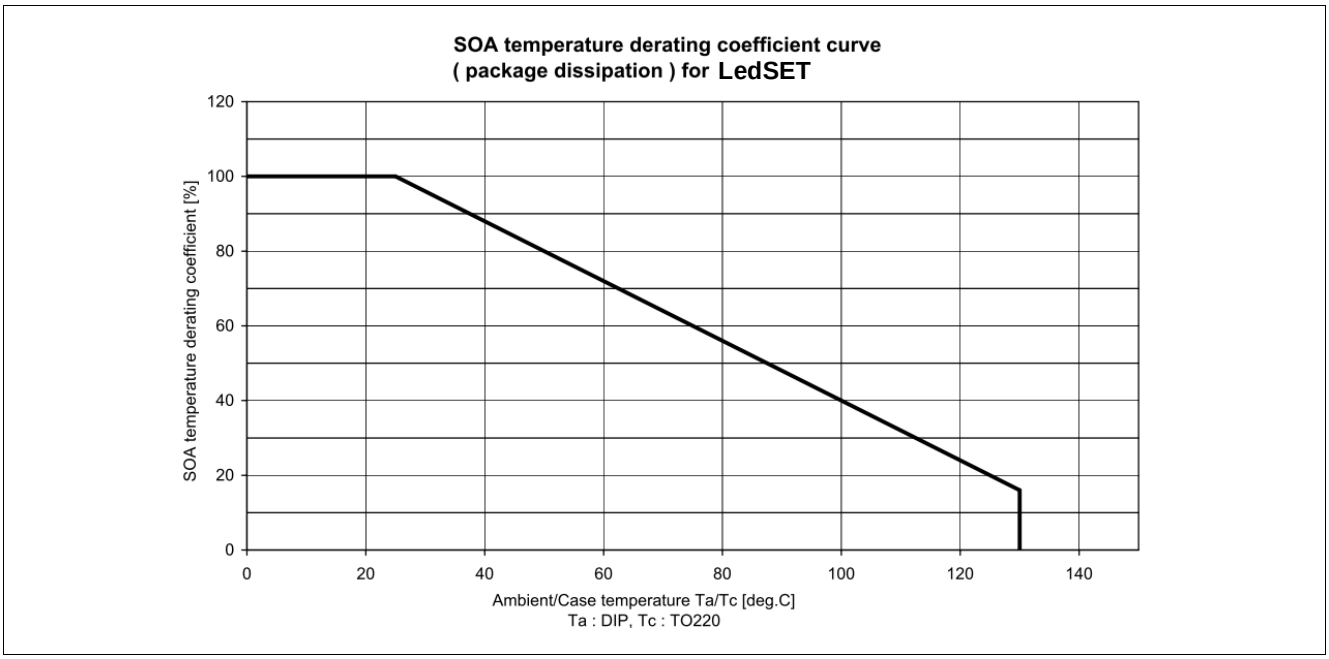


Figure 31 SOA temperature derating coefficient curve

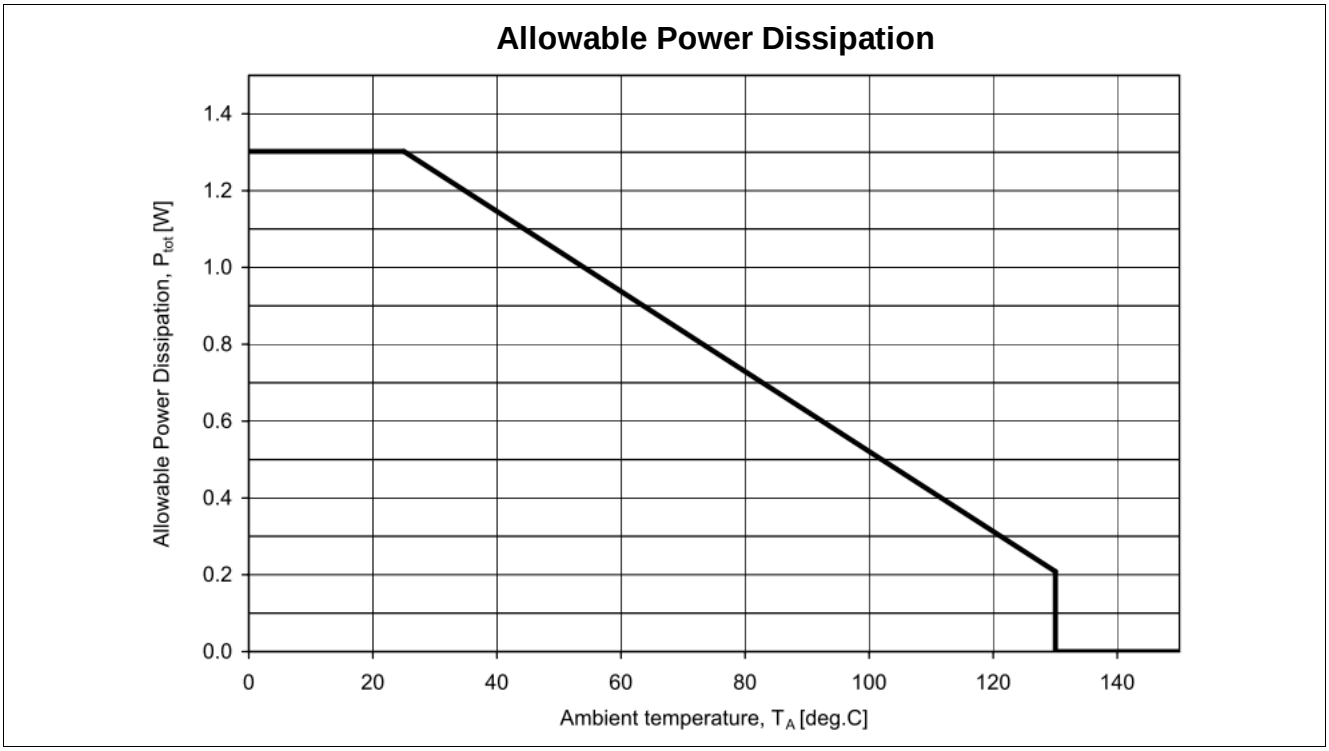


Figure 32 Power dissipation; $P_{tot} = f(T_a)$

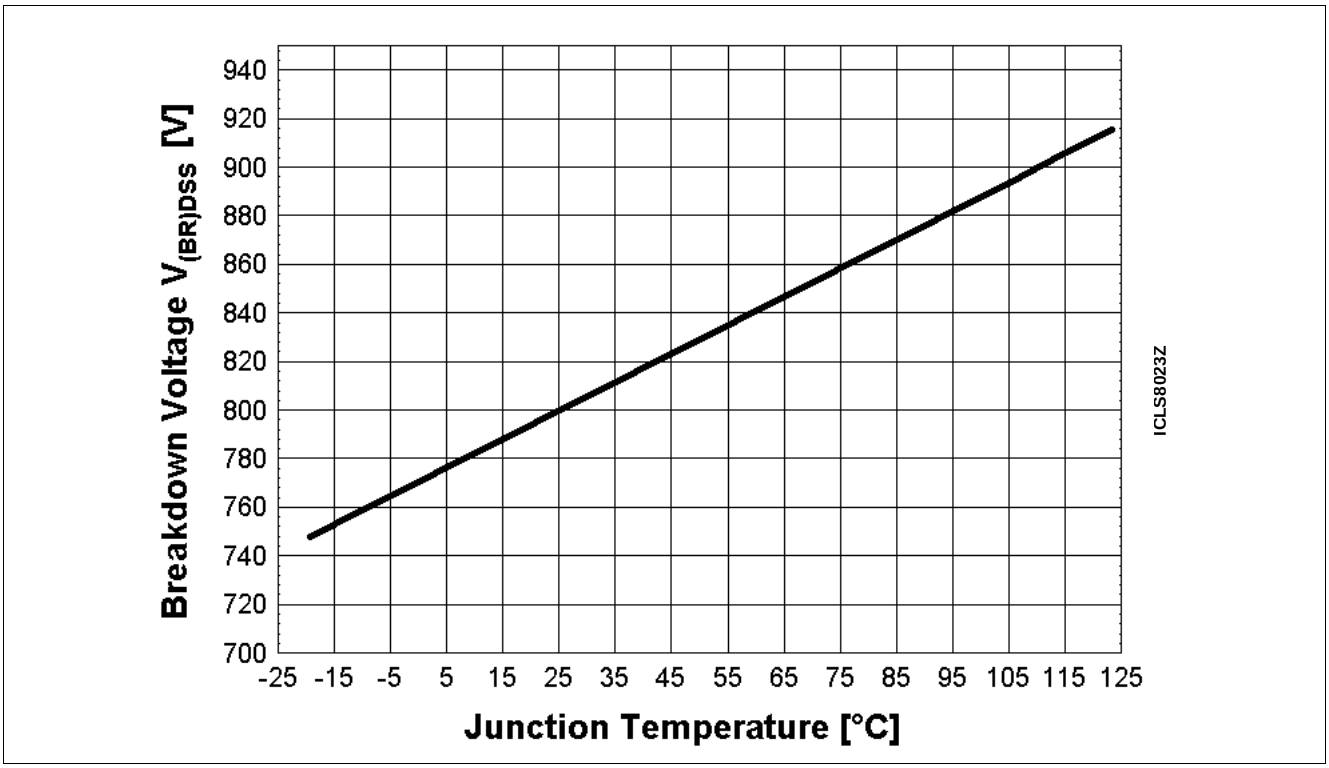


Figure 33 Drain-source breakdown voltage; $V_{BR(DSS)} = f(T_j)$, $I_D = 0.25$ mA

6 Input Power Curve

Two input power curves giving the typical input power versus ambient temperature are showed below; Vin = 85 Vac ~ 265 Vac (**Figure 34**) and Vin = 230 Vac ± 15 % (**Figure 35**). The curves are derived on the basis of a typical discontinuous mode flyback model which considers either a 60 % maximum duty ratio or 150 V maximum secondary-to-primary-reflected voltage (higher priority). The calculation is based on no copper area as the heat sink for the device. The input power already includes the power loss at input common mode choke, bridge rectifier and the CoolMOS™.The device saturation current (I_{D_Puls} @ T_j = 125 °C) is also considered.

To estimate the output power of the device, simply multiply the input power at a particular operating ambient temperature with the estimated efficiency for the application. For example, a wide range input voltage (**Figure 34**), operating temperature 50 °C, estimated efficiency 85 %, then the estimated output power is 23 W (28 W * 85 %).

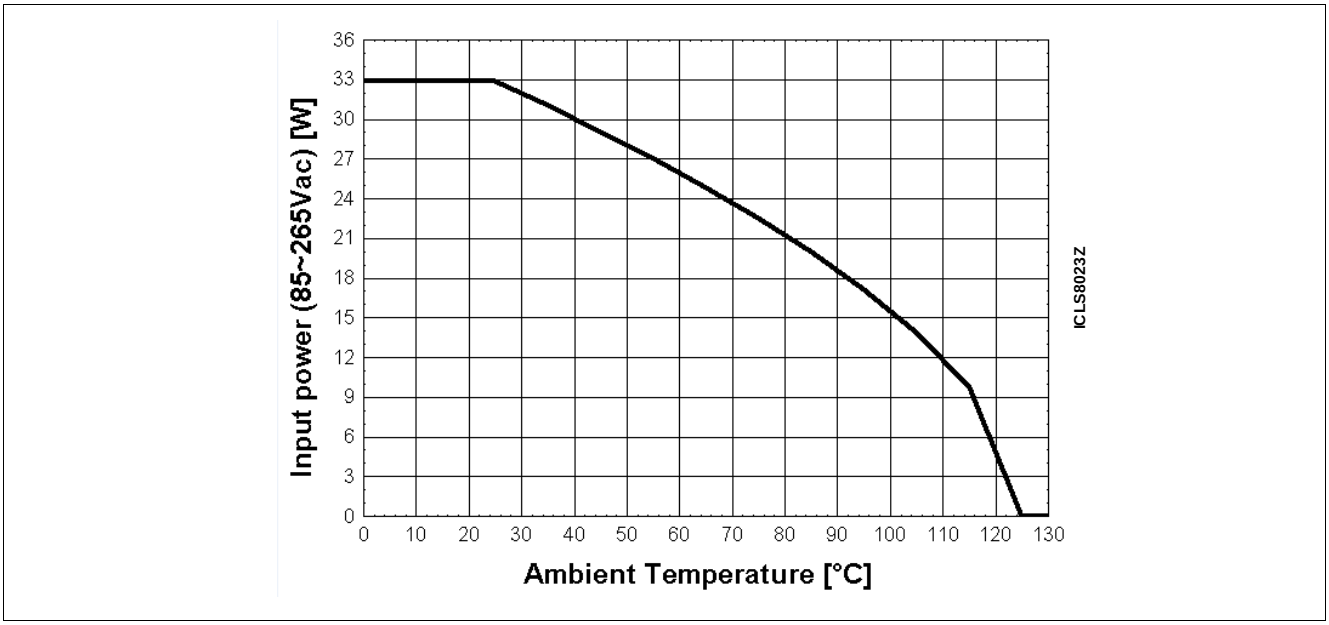


Figure 34 Input power curve Vin = 85~265 Vac; P_{in} = f(T_a)

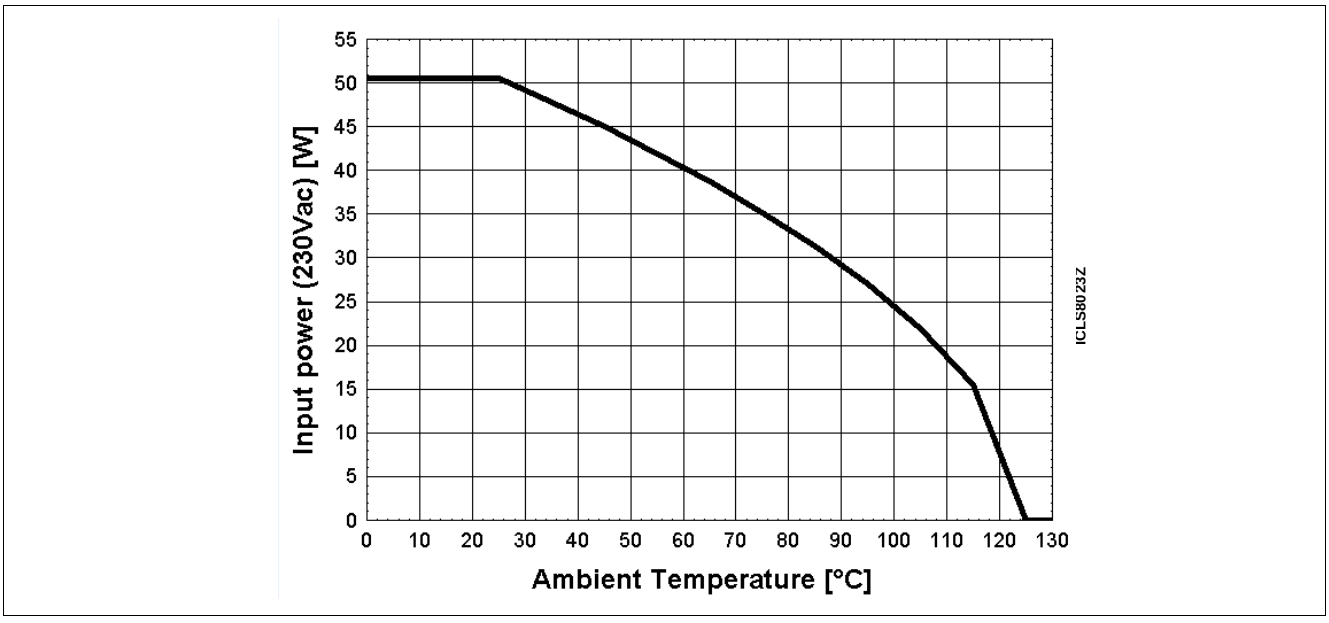
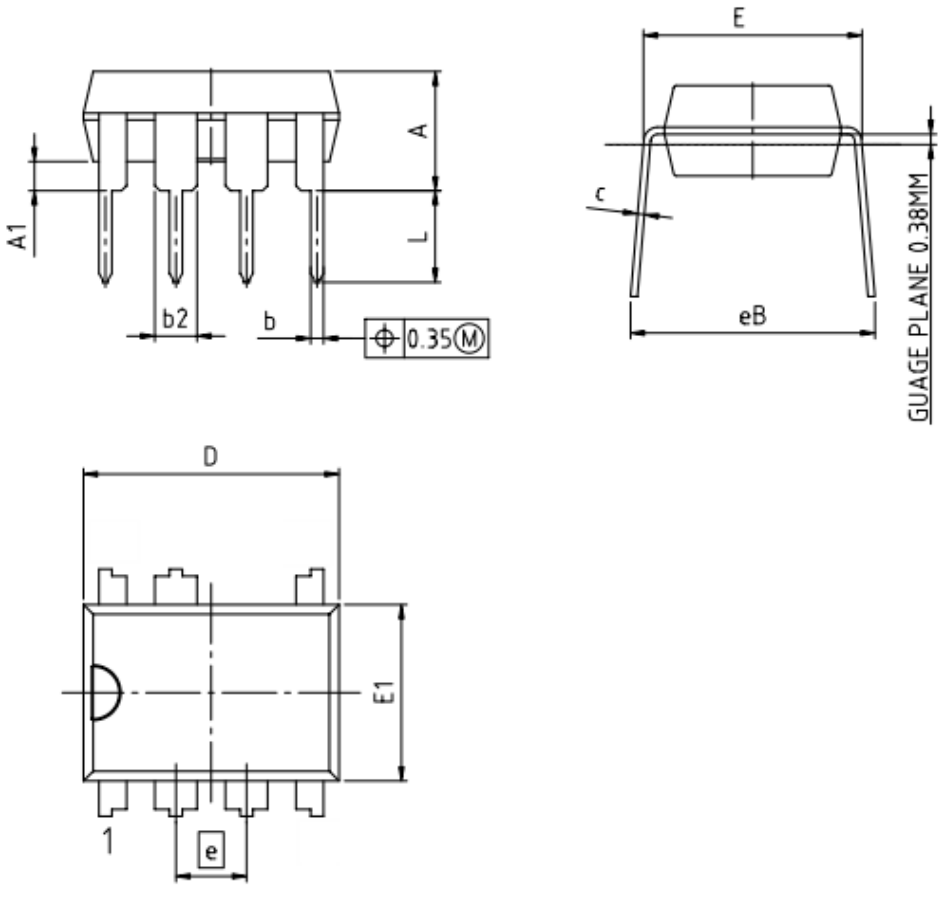


Figure 35 Input power curve Vin = 230 Vac ± 15 %; P_{in} = f(T_a)

7 Outline Dimensions

7.1 Outline Dimensions of PG-DIP-7



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	4.37	-	0.172
A1	0.38	-	0.015	-
b	0.38	0.58	0.014	0.022
b2	-	1.700	-	0.067
c	0.21	0.38	0.008	0.014
D	9.1	9.77	0.358	0.385
E	7.49	8.25	0.295	0.325
E1	6.1	6.6	0.240	0.260
e	2.54 BSC		0.1 BSC	
N	7		7	
eB	7.9	10.9	0.311	0.429
L	2.92	-	0.115	-

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Figure 36 PG-DIP-7 (Pb-free lead plating plastic dual inline outline)

8 Marking

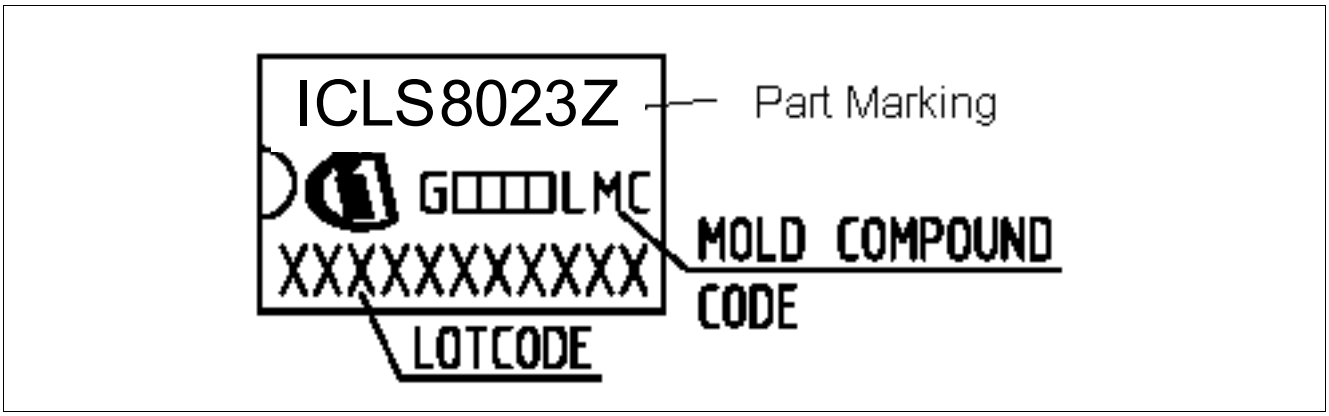

Figure 37 Marking for ICLS8023Z

w w w . i n f i n e o n . c o m

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