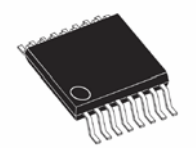
# ALED6001

## Automotive-grade PWM-dimmable single channel LED driver with integrated boost controller

**Datasheet - production data**



**TSSOP-16**

## Features

- AECQ100 qualification
- Switching controller section
  - 5.5 V to 36 V input voltage range
  - Very low shutdown current: $I_{SHDN}$ < 10 µA
  - Internal +5 V LDO for gate driver supply
  - Internal +3.3 V LDO for device supply
  - Fixed frequency peak current mode control
  - Adjustable (100 kHz to 1 MHz) switching frequency
  - External synchronization for multi-device applications
  - High performance external MOSFET driver
  - Cycle-by-cycle external MOSFET OCP
  - Fixed internal soft-start
  - Programmable output OVP
  - Boost, buck-boost and SEPIC topologies supported
  - Thermal shutdown with autorestart
  - Output short-circuit detection
- LED control section
  - Up to 60 V output voltage
  - Constant current control loop
  - High-side output current sensing circuitry
  - 30 to 300 mV differential sensing voltage
  - ± 4% output current reference accuracy
  - Output overcurrent protection
  - Sensing resistor failure protection
  - PWM dimming with auxiliary series switch
  - Analog dimming

## Applications

- Automotive exterior lighting
- Daytime running lights
- High and low beam lights
- Fog lights
- Position lights / blinkers

## Description

The ALED6001 is an automotive-grade (AECQ100 compliant) LED driver that combines a boost controller and high-side current sensing circuitry optimized for driving one string of high-brightness LEDs. The device is compatible with multiple topologies such as boost, SEPIC and floating load buck-boost. PWM dimming of the LED brightness is achieved by means of an external MOSFET in series with the LED string and directly driven by a dedicated pin. The pin that manages the LED current setting, usually connected to an external resistor, can also be used as analog control if a microcontroller is located in the LED module. The high-side current sensing, in combination with a P-channel MOSFET, provides effective protection in case the positive terminal of the LED string is shorted to ground. The high precision current sensing circuitry allows an LED current regulation reference within ± 4% accuracy over the entire temperature range and production spread. A fault output (open-drain) informs the host system of faulty conditions: device overtemperature, output overvoltage (disconnected LED string) and LED overcurrent.

**Table 1. Device summary**

| Order code | Package | Packaging |
|---|---|---|
| ALED6001 | HTSSOP-16 (exposed pad) | Tube |
| ALED6001TR | | Tape and reel |

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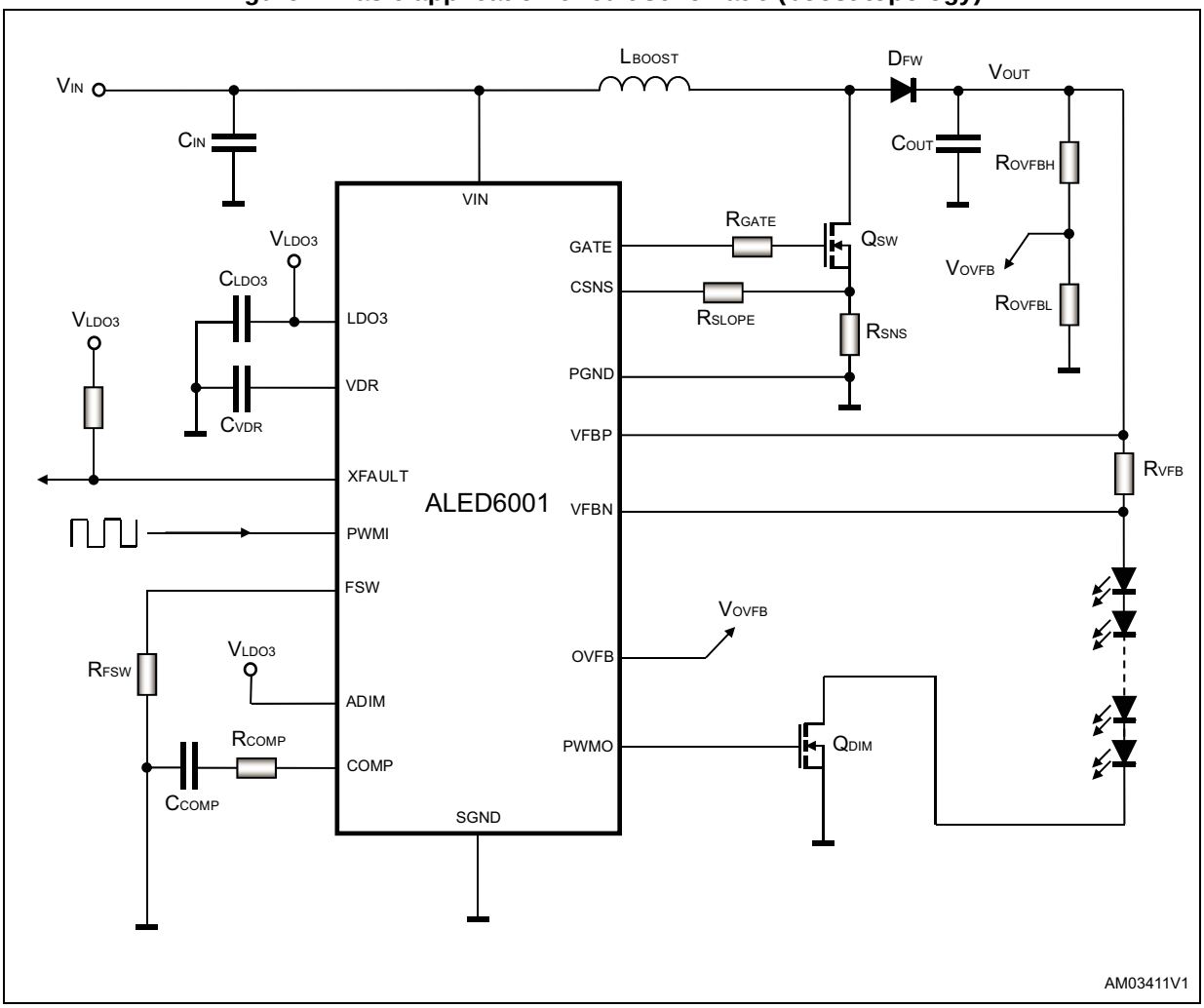
# 1 Typical application circuit

**Figure 1. Basic application circuit schematic (boost topology)**



# 2 Pin function

**Figure 2. Pin connection (through top view)**

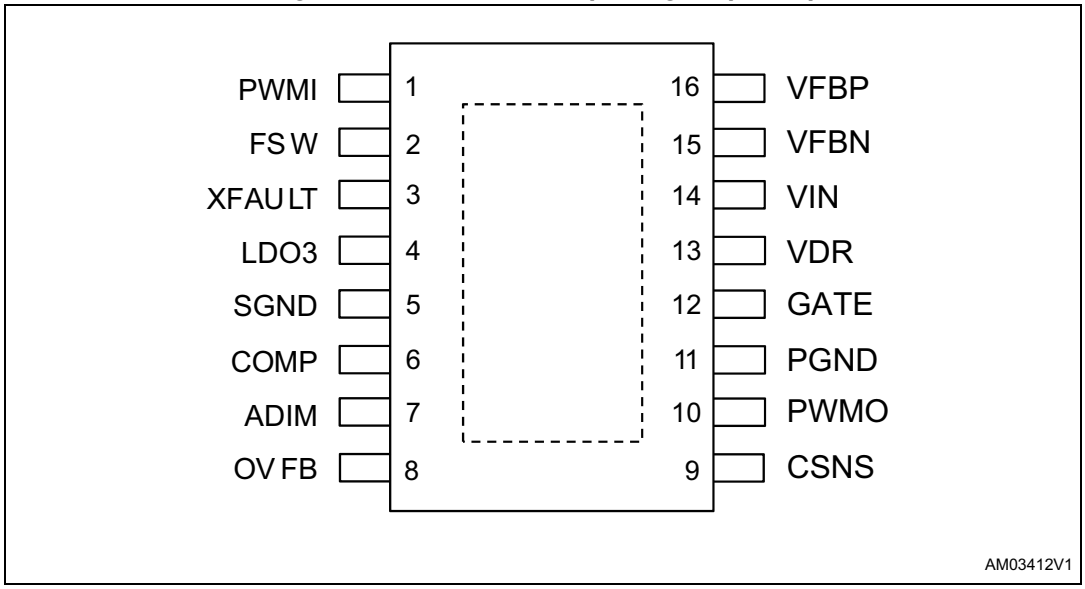
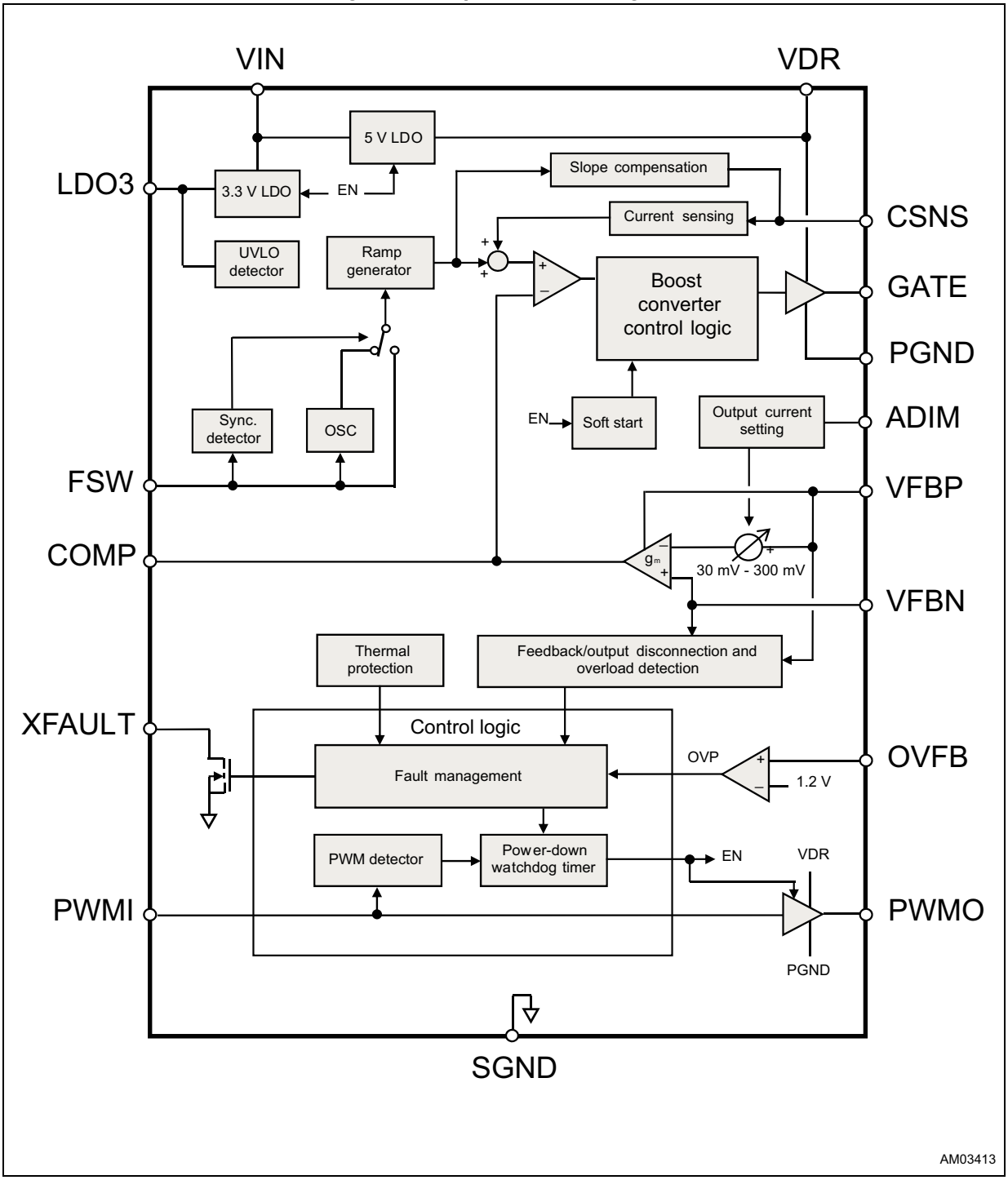


**Table 2. Pin description**

| No. | Pin | |
|---|---|---|
| 1 | PWMI | Device enable and PWM dimming control input. |
| 2 | FSW | Switching frequency setting. A resistor between this pin and SGND sets the desired switching frequency. This pin is also used as synchronization input. If tied high (e.g.: connected to LDO3 pin) a 600 kHz switching frequency is set. |
| 3 | XFAULT | Fault indicator, open-drain output. This pin is tied low by the device in case of faulty condition. See *Section 7.4 on page 20* for details. |
| 4 | LDO3 | 3.3 V linear regulator output and device supply. Connect a 1 µF (typ.) bypass MLCC between this pin and SGND as close as possible to the chip. |
| 5 | SGND | Signal ground. Return for analog circuitry. All setting components must refer to this grounding pin. |
| 6 | COMP | Boost controller loop compensation. A simple RC series must be connected between this pin and SGND for proper loop compensation. See *Section 7.2.3 on page 14* for details. |
| 7 | ADIM | Analog dimming control input. The current at the output is linearly controlled by the voltage applied to this pin (0.3 V to 1.2 V). When the device is set to operate in standalone mode, a partition of the LDO3 voltage must be applied to this pin through a resistor divider. |
| 8 | OVFB | Output overvoltage protection feedback input. Connect to the central tap of a resistor divider at the output. |
| 9 | CSNS | Boost controller power switch current sensing input. Connect to the source of the external Power MOSFET for proper switch overcurrent protection. |
| 10 | PWMO | PWM dimming control output. This pin provides a PWM output signal (in phase with the one applied to the PWMI pin) for direct control of a dimming N-channel MOSFET. |
| 11 | PGND | Power ground. Return for the VDR linear regulator and the power switch gate drivers. Also used as reference for the Power MOSFET current sensing circuitry. Connect to ground as close as possible to the quiet terminal of the power switch sensing resistor. |
| 12 | GATE | Power switch gate driver output. Connect to the gate of the Power MOSFET through a small value resistor. |
| 13 | VDR | 5 V linear regulator output and gate driver supply. Connect a 1 µF (typ.) bypass MLCC between this pin and PGND as close as possible to the chip. |
| 14 | VIN | Supply voltage input. Connect this pin to the supply power rail. A 1 µF (typ.) bypass MLCC must be connected between this pin and PGND as close as possible to the chip. |
| 15 | VFBN | Output current differential sensing input, negative terminal. Connect to the hot terminal (load side) of the high-side sensing resistor. |
| 16 | VFBP | Output current differential sensing input, positive terminal. Connect to the quiet terminal (output capacitor side) of the high-side sensing resistor. |
| - | TPAD | Thermal pad. Connect to a suitable ground plane area in order to ensure proper heat dissipation. Electrically connected to PGND and SGND. |

# 3 Block diagram

**Figure 3. Simplified block diagram**



# 4 Absolute maximum ratings

**Table 3. Absolute maximum ratings(1)**

| Parameter | Pin | Min. | Max. | Unit |
|---|---|---|---|---|
| Maximum pin voltage | VIN to SGND | | 40 | V |
| | VFBP and VFBN to SGND | | 65 | |
| | VDR to SGND | -0.3 | 6 | |
| | LDO3 to SGND | -0.3 | 3.6 | |
| | COMP, CSNS and OVFB to SGND | -0.3 | 3.6 | |
| | PGND to SGND | -0.3 | 0.3 | |
| | XFAULT, FSW, ADIM and GATE to SGND | -0.3 | 6 | |
| | PWMI and PWMO to SGND | -0.3 | 6 | |
| HBM ESD susceptibility JEDEC JS001 | All pins | -2000 | 2000 | |
| VIN, VFBP, VFBN and ADIM ESD susceptibility | VIN, VFBP, VFBN, ADIM to SGND | -4000 | 4000 | |
| CDM ESD resistivity to SGND ANSI/ESD STM5.3.1 | Corner pins | -750 | 750 | |
| | Non-corner pins | -500 | 500 | |

1. Stresses beyond those listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in *Table 5* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

**Table 4. Thermal characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{J,OP}$ | Operating junction temperature | | -40 | | 150 | °C |
| $T_{STG}$ | Storage temperature range | | -50 | | 150 | |
| $T_{SHDN}$ | Thermal shutdown threshold | | 150 | 160 | 175 | |
| | Thermal shutdown hysteresis | | | 20 | | |
| | XFAULT release hysteresis | | | 40 | | |
| $R_{th,JA}$(1) | Junction to ambient thermal resistance | 1s0p | | 55 | | °C/W |
| | | 2s2p | | 45 | | |
| $R_{th,JC}$ | Junction to case thermal resistance | | | 37 | | |

1. The device mounted on a standard JESD51-5 test board.

# 5 Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **DC characteristics** | | | | | |
| $V_{VIN}$ | Supply input voltage range | | 5.5 | 36 | V |
| $V_{VDR}$ | VDR pin Input voltage range | VDR and VIN shorted together | 4.7 | 5.5 | |
| $V_{VFBx}$ | Feedback input common mode voltage range | | 4.4 | 60 | |
| $V_{FB}$ | Feedback input differential mode voltage range | VFBP to VFBN | 30 | 300 | mV |
| **AC characteristics** | | | | | |
| $f_{sw}$ | Switching frequency | | 100 | 1000 | kHz |
| $f_{PWMI}$ | Dimming frequency | | 0.1 | 20 | |
| $t_{PWMI,en}$ | Minimum PWMI pulse duration for device enable (turn on) | PWMI input, $f_{SW}$ = 800 kHz | 100 | | µs |
| $t_{PWMI,dim}$ | Minimum dimming on-time | PWMI input, $f_{SW}$ = 1 MHz | 6 | | µs |

# 6 Electrical characteristics

$V_{IN}$ = 12 V, $V_{VFBP}$ = 12 V, $V_{VFBN}$ = 12 V and $T_J$ =- 40 °C to 125 °C if not otherwise specified.

**Table 6. Electrical characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply section** | | | | | | |
| $V_{VIN}$ | Supply voltage range | | 5.5 | | 36 | V |
| | PWMI turn on threshold | | | 1.34 | 1.65 | |
| | PWMI turn off threshold | | 0.7 | 0.85 | 1.1 | |
| | PWMI pull-down resistor | PMWI at 3.3 V | 350 | 570 | 810 | kΩ |
| $t_{SHDN}$ | PWMI low to shutdown mode delay | | 10 | 15 | 22 | ms |
| $t_{START}$ | Start-up time | $C_{LDO3}$ = $C_{VDR}$ = 470 nF | | 100 | 180 | µs |
| $V_{LDO3}$ | 3.3 V LDO output voltage | 6 V ≤ $V_{IN}$ ≤ 36 V, $I_{LDO3}$ = 0.5 mA, PWMI high | 3.17 | 3.3 | 3.4 | V |
| | 3.3 V LDO line regulation | $I_{LDO3}$ = 20 mA, PWMI high 6 V ≤ $V_{IN}$ ≤ 36 V | | 5 | 20 | mV |
| | 3.3 V LDO load regulation | $V_{IN}$ = 6 V, PWMI high 0.5 mA ≤ $I_{LDO3}$ ≤ 20 mA | | 90 | 100 | |
| $V_{LDO3,ON}$ | LDO3 undervoltage lockout upper threshold | | 2.2 | 2.8 | 3.0 | V |
| $V_{LDO3,OFF}$ | LDO3 undervoltage lockout lower threshold | | 2.5 | 2.7 | 2.9 | |
| | LDO3 undervoltage lockout hysteresis | | 50 | 200 | 400 | mV |
| | 3.3 V LDO current limit | VLDO3 = 3.0 V | 25 | 38 | 46 | mA |
| $V_{VDR}$ | 5 V LDO output voltage | 6 V ≤ $V_{IN}$ ≤ 36 V $I_{VDR}$ = 0.5 mA, PWMI high | 4.75 | 5.0 | 5.2 | V |
| | 5 V LDO line regulation | $I_{VDR}$ = 40 mA, PWMI high 6 V ≤ $V_{IN}$ ≤ 36 V | | 10 | 40 | mV |
| | 5 V LDO load regulation | $V_{IN}$ = 6 V, PWMI high 0.5 mA ≤ $I_{VDR}$ ≤ 40 mA | | 120 | 200 | |
| | 5 V LDO dropout voltage | $I_{VDR}$ = 25 mA, $V_{VIN}$ = 4.8 V | | 150 | 300 | |
| $V_{VDR,ON}$ | VDR undervoltage lockout upper threshold | | 4.3 | 4.6 | 4.75 | V |
| $V_{VDR,OFF}$ | VDR undervoltage lockout lower threshold | | 4.1 | 4.4 | 4.6 | |
| | VDR undervoltage lockout hysteresis | | 100 | 150 | 340 | mV |
| | 5 V LDO current limit | $V_{VDR}$ = 4.5 V | 50 | 75 | 100 | mA |

**Table 6. Electrical characteristics (continued)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Power consumption** | | | | | | |
| $I_{VIN,SHDN}$ | Shutdown current | $V_{IN}$ = 16 V, PWMI low, -40 °C ≤ $T_J$ ≤ 25 °C | 1 | 4 | 10 | µA |
| | | $V_{IN}$ = 16 V, PWMI low, 25 °C ≤ $T_J$ ≤ 125 °C | 1 | 9 | 25 | |
| $I_{VIN,Q}$ | Quiescent current | $V_{IN}$ = 16 V, PWMI to LDO3, -40 °C ≤ $T_J$ ≤ 125 °C switching off-time | | 1 | 1.7 | mA |
| $I_{VIN,ON}$ | Operating current | $V_{IN}$ = 16 V, PWMI high, $f_{SW}$ = 200 kHz, $C_L$ = 3.3 nF | | 5 | 7 | |
| **Boost controller** | | | | | | |
| $t_{ON,min}$ | Minimum switching on-time | Pulse skipping mode | | 140 | 180 | ns |
| $K_{FSW}$ | Switching frequency constant | $R_{FSW}$ = 250 kΩ | 45 | 50 | 55 | MHz • kΩ |
| $f_{SW}$ | Adjustable switching frequency | $R_{FSW}$ = 500 kΩ | 90 | 100 | 110 | kHz |
| | | $R_{FSW}$ = 250 kΩ | 180 | 200 | 220 | |
| | | $R_{FSW}$ = 50 kΩ | 870 | 1000 | 1070 | |
| | Fixed switching frequency | FSW pin high (LDO3) | 490 | 600 | 710 | |
| | Synchronization signal frequency capture range | $t_{CLK,H}$ = 250 ns, $V_{CLK,L}$ = 0.8 V, $V_{CLK,H}$ = 3.0 V | 100 | | 1000 | |
| | FSW synchronization input high level | $f_{CLK}$ = 100 kHz to 1 MHz, $t_{CLK,H}$ = 250 ns | 2.8 | | | V |
| | FSW synchronization input low level | | | | 0.5 | |
| | Synchronization input high level pulse width | $f_{CLK}$ = 100 kHz to 1 MHz, $V_{CLK,L}$ = 0.5 V, $V_{CLK,H}$ = 2.8 V | 250 | | | ns |
| $R_{GATE}$ | Power switch gate driver output resistance | Pull-up | | 3 | 6 | Ω |
| | | Pull-down | | 1 | 3 | |
| $t_{r,GATE}$ | Power switch gate driver rise time (20 to 80%) | $V_{VDR}$ = 5 V, $C_L$ = 3.3 nF | | 15 | 30 | ns |
| $t_{f,GATE}$ | Power switch gate driver fall time (80 to20%) | | | 7 | 14 | |
| $t_{SS}$ | Internal soft-start duration | | 2.7 | 3.5 | 4.6 | ms |
| $K_S$ | Slope compensation constant | | 3 | 5 | 7 | A/s |
| $V_{CSNS,OCP}$ | Power switch OCP detection threshold | CSNS pin to PGND | 300 | 360 | 400 | mV |

**Table 6. Electrical characteristics (continued)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Output current sensing section** | | | | | | |
| $V_{FB}$ | Feedback voltage ($V_{VFBP}$ - $V_{VFBN}$ differential current sensing voltage) | $V_{ADIM}$ = 0.3 V | 20 | 30 | 40 | mV |
| | | $V_{ADIM}$ = 0.6 V | 110 | 120 | 130 | |
| | | $V_{ADIM}$ = 1.2 V | 280 | 300 | 304 | |
| | Feedback reference voltage accuracy | $V_{ADIM}$ to LDO3 | 290 | 300 | 310 | |
| $V_{ADIM,OFF}$ | ADIM pin voltage turn off threshold | | 240 | 270 | 290 | |
| | ADIM pin voltage turn off hysteresis | | 1 | 10 | 20 | |
| $I_{VFBP}$ | Feedback positive input current | $V_{VFBP}$ = 12.0 V<br>$V_{VFBN}$ = 11.7 V | -32 | -25 | -18 | µA |
| $I_{VFBN}$ | Feedback negative input current | $V_{VFBP}$ = 12.0 V<br>$V_{VFBN}$ = 11.7 V | -7 | -5 | -4 | |
| **PWM dimming control** | | | | | | |
| $R_{PWMO}$ | PWMO gate driver output resistance | Pull-up | | 14 | 25 | Ω |
| | | Pull-down | | 3 | 8 | |
| $t_{r,PWMO}$ | PWMO gate driver rise time (20 to 80%) | $V_{VDR}$ = 5 V, $C_L$ = 3.3 nF | | 50 | 130 | ns |
| $t_{f,PWMO}$ | PWMO gate driver fall time (80 to 20%) | | | 30 | 60 | |
| **Fault management section** | | | | | | |
| | XFAULT output low level | $I_{XFAULT}$ = 4 mA | | 0.12 | 0.2 | V |
| | XFAULT high level leakage current | $V_{XFAULT}$ = 5 V | | 1 | 4 | µA |
| $V_{OVFB,th}$ | OVFB input overvoltage detection threshold | | 1.14 | 1.20 | 1.25 | V |
| | OVFB input overvoltage detection hysteresis | | 70 | 100 | 130 | mV |
| | OVFB pull-up current | $V_{OVFB}$ = 1 V | 0.7 | 1 | 1.2 | µA |
| | Open load/VFBP pin disconnection detection threshold (differential) | ($V_{VFBP}$ - $V_{VFBN}$) | -190 | -120 | -80 | mV |
| | Overload /VFBN pin disconnection detection threshold (differential) | | 550 | 600 | 650 | |
| | VFBx undervoltage detection threshold | $V_{VFBx}$ respect to SGND | 3.1 | 3.5 | 4.1 | V |

# 7 Device description

The ALED6001 device is a LED driver that integrates a boost controller, a high-side current sensing circuitry and a gate driver for an external dimming switch. It has been specifically designed for driving a single string of high-brightness LEDs. The device can support boost, floating buck-boost and SEPIC topologies in order to cover most of applications. A single pin, PWMI, combines both the device enable and PWM dimming control functions.

The brightness of the LED string can be controlled through PWM modulation, analog control of the output current level (by means of a dedicated pin) or a combination of the two.

## 7.1 Device supply

The ALED6001 device integrates two low dropout linear regulators to derive the + 3.3 V (typ.) main supply and the +5 V supply for the gate drivers. The VIN pin is the input terminal for both linear regulators. Both the linear regulators are enabled when a PWM signal is applied to the PMWI pin. If the PWMI pin is held low for more than 10 ms (min.), the shutdown mode is automatically entered and both the LDOs are turned-off for minimum power consumption. An undervoltage lockout (UVLO) protection is associated to each linear regulator: in case the output voltage of LDO3 and VDR is below their respective nominal value, the device is no allowed to operate and the XFAULT pin is tied low.

When an external +5 V rail is available, the related internal LDO can be bypassed by connecting together the VIN and VDR pins: in this case the VDR pin is used as supply input.

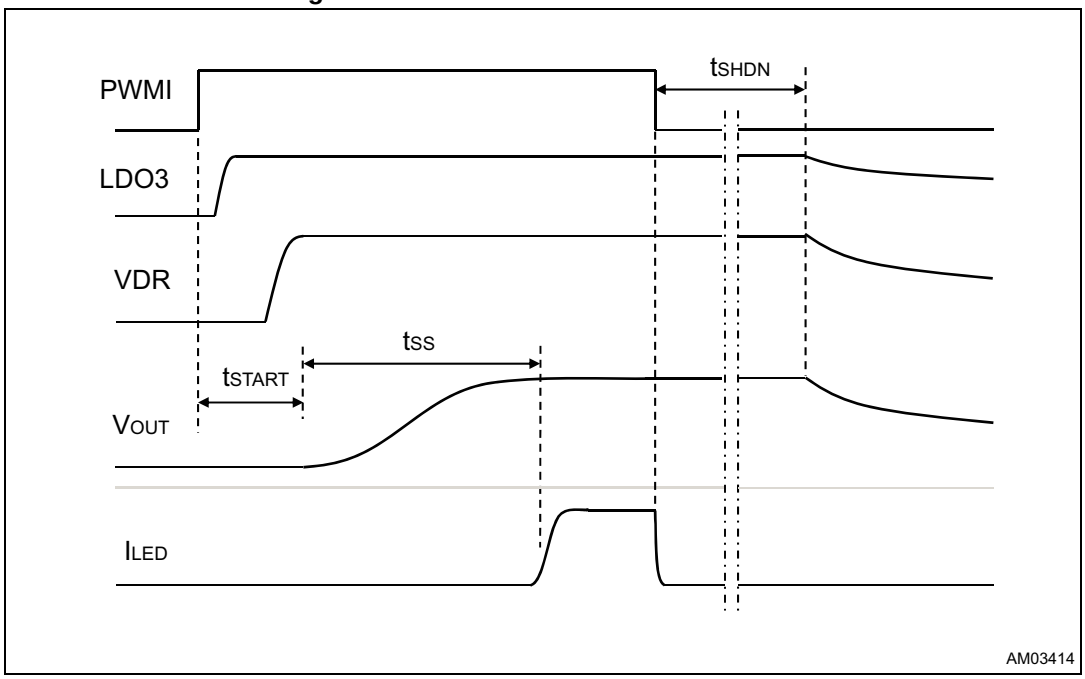
## 7.2 Boost controller

### 7.2.1 Turn on and power-down sequences

The ALED6001 is turned on and off by acting on the PWMI pin. This digital input combines two functions at the same time: device turn on/off and PWM dimming control.

When a high pulse having a 100 µs (typ.) minimum duration appears at the PWMI pin, the LDOs are turned on and, after the VDR has reached its nominal value, a soft-start sequence on the boost controller takes place. The output voltage is smoothly increased by releasing in steps the current limit of the boost converter within a fixed 3 ms (typ.) period, unless the feedback voltage reaches 75% of the nominal value in advance.

**Figure 4. Turn on and turn off waveforms**



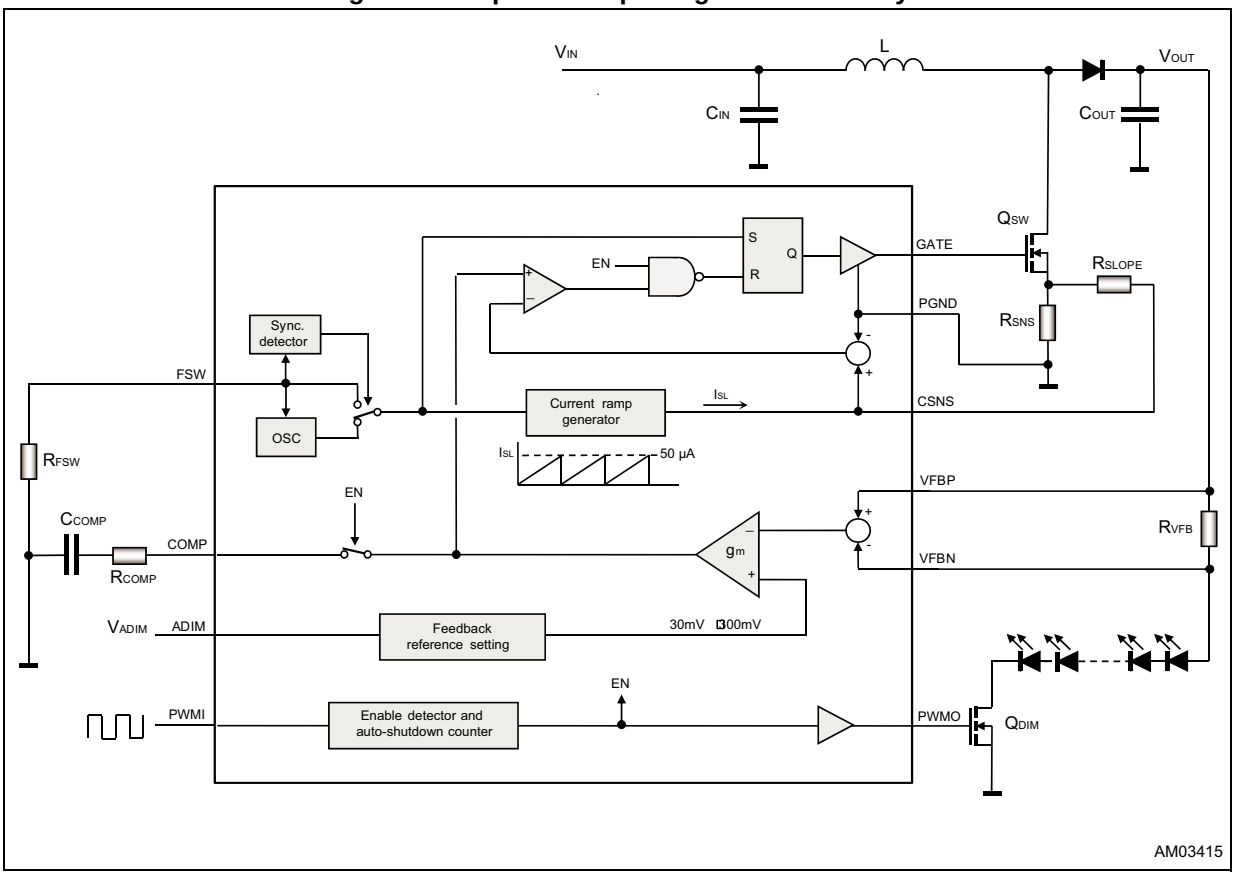

Suddenly after the pulse detection at the PWMI pin, an internal timer is enabled and cleared. The timer starts counting down on every subsequent falling edge. If the PWMI pin is held low for more than 10 ms (typ.), the timer is allowed to expire and the ALED6001 automatically turns off minimizing the current consumption.

The start-up time, defined as the delay between the rising edge at the PWMI pin and the first pulse at the GATE pin, clearly depends on the bypass capacitors connected on both LDO3 and VDR pins. With a typical 1 µF MLCC for both pins, the start-up time is in the order of 100 µs.

### 7.2.2 Boost controller operation

The boost controller of the ALED6001 device is based on peak current mode control architecture and can easily support boost, floating buck-boost and SEPIC topologies. The switching frequency of the converter is set through the FSW pin (external clock source or setting resistor toward ground) while the switching duty cycle is modulated by the control loop in order to keep the output (LED) current constant. As a consequence, the output voltage of the boost converter is determined by the LED string.

**Figure 5. Simplified output regulation circuitry**




The boost controller regulates the output (LED) current by measuring the voltage across the external sensing resistor. The internal circuitry related to the two pins connected to the sensing resistor (VFBP and VFBN) has been designed to implement a high-side sensing scheme and can sustain a relatively high voltage. The voltage drop across the sensing resistor is the actual feedback voltage for the boost regulator control loop and it can be linearly varied by means of the ADIM pin (see *Section 7.3: LED current regulation and brightness control on page 17* for details).

The COMP pin is the output of the transconductance amplifier involved in the regulation loop and a simple RC series must be connected between this pin and SGND to ensure proper loop stability.

### 7.2.3 Boost converter stability and slope compensation

As visible in *Figure 5*, the difference between the feedback voltage and the programmed is converted into an error current by the transconductance amplifier. This current, provided at the COMP pin, is turned into a voltage across the compensation network externally connected to the same pin. This voltage, in turn, determines the trip current for the following error amplifier.

When the boost converter operates in continuous conduction mode (CCM) and the switching duty cycle is higher than 50%, sub-harmonic instability may occur.

In order to prevent this, the trip current has to be properly shaped by summing a negative sawtooth ramp voltage (slope compensation) with the amplified error voltage.

In the ALED6001 the slope compensation is achieved by injecting a sawtooth current into the CSNS pin. Therefore the voltage across the CSNS pin is given by:

**Equation 1**

$$v_{CSNS}(t) = i_{MOS}(t) \bullet R_{SHUNT} + i_{SL}(t) \bullet R_{CSNS}$$

The $R_{SNS}$ resistor is usually designed so that the peak voltage is about 15% of the overcurrent threshold at the CSNS pin in order to have a good S/N ratio, while the $R_{SLOPE}$ resistor is calculated for the desired slope compensation amount (typically at least half the downslope of the inductor current during the switching off-time):

**Equation 2**

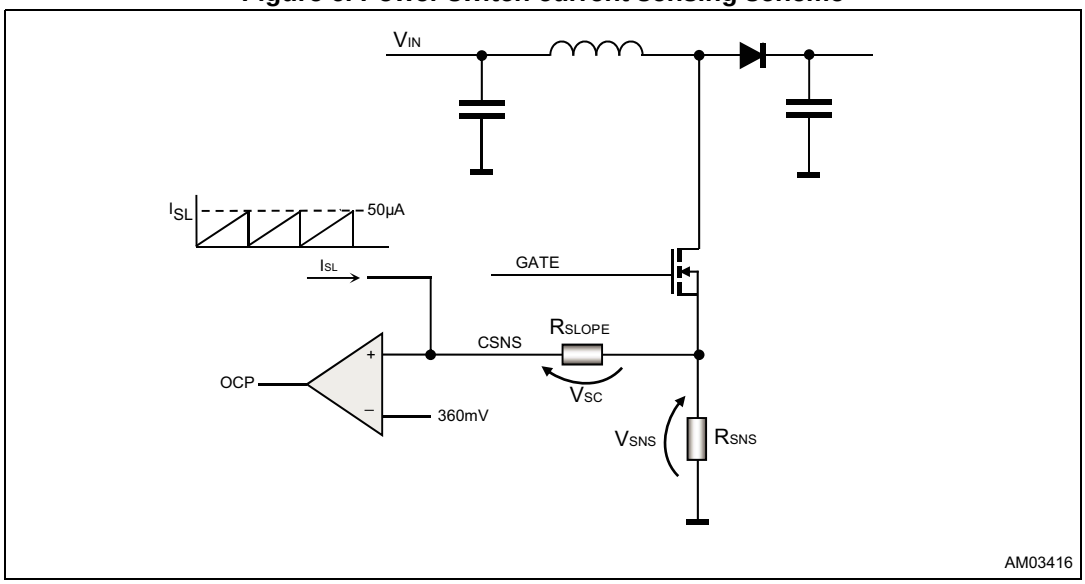
$$R_{SNS} \cong \frac{50mV}{I_{L,PEAK}}$$

**Equation 3**

$$R_{SLOPE} \geq \frac{V_{OUT} - V_{IN,min}}{f_{SW} \bullet L} \bullet \frac{R_{SNS}}{I_{SL}}$$

Where $I_{SL}$ = 50 µA is the maximum current injected by the slope compensation circuitry in the CSNS pin.

**Figure 6. Power switch current sensing scheme**



### 7.2.4 Switching frequency oscillator and external synchronization

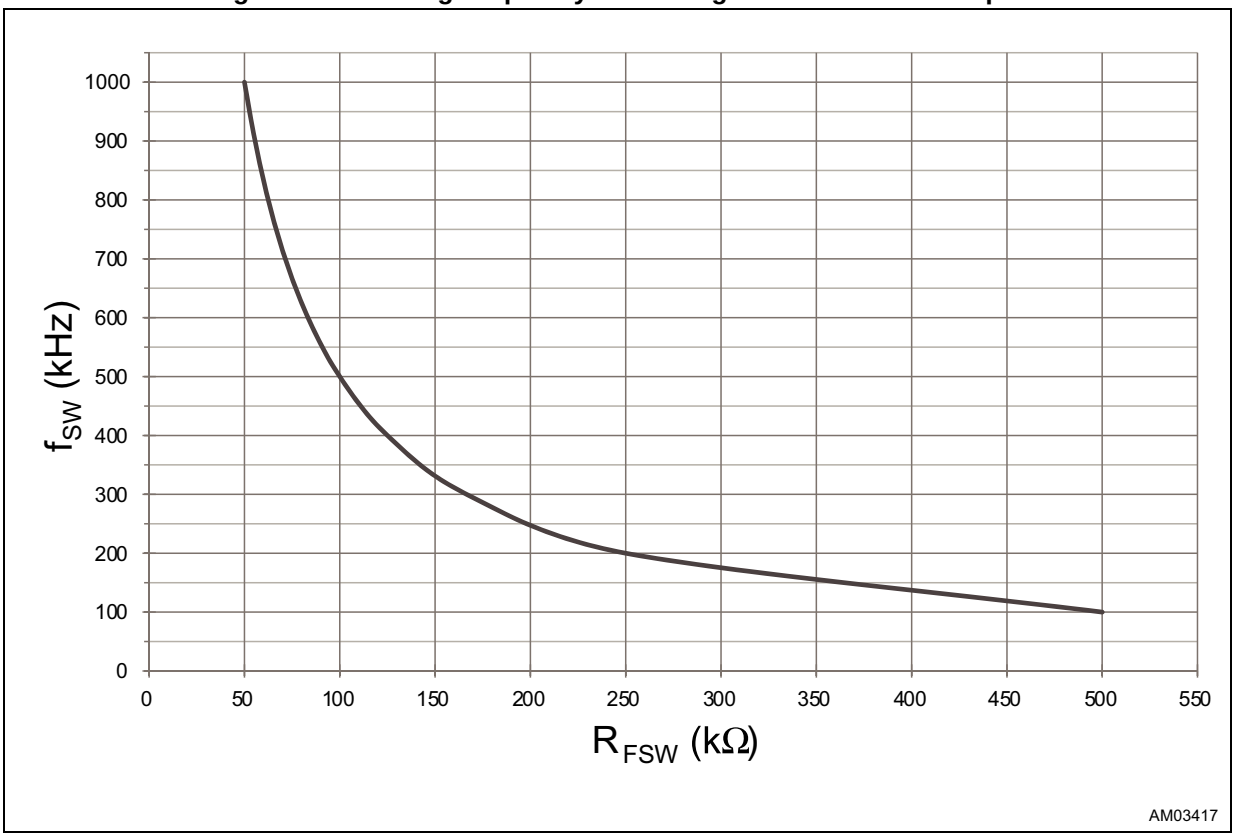
The switching frequency of the boost controller is simply set by connecting a resistor between the FSW pin and ground. The resistor can be calculated according to *Equation 4*:

**Equation 4**

$$R = \frac{K_{FSW}}{f_{SW}}$$

Where $K_{FSW} = 5 \bullet 10^{10}$ Hz • Ω (typ.) and 100 kHz ≤ $f_{SW}$ ≤ 1 MHz.

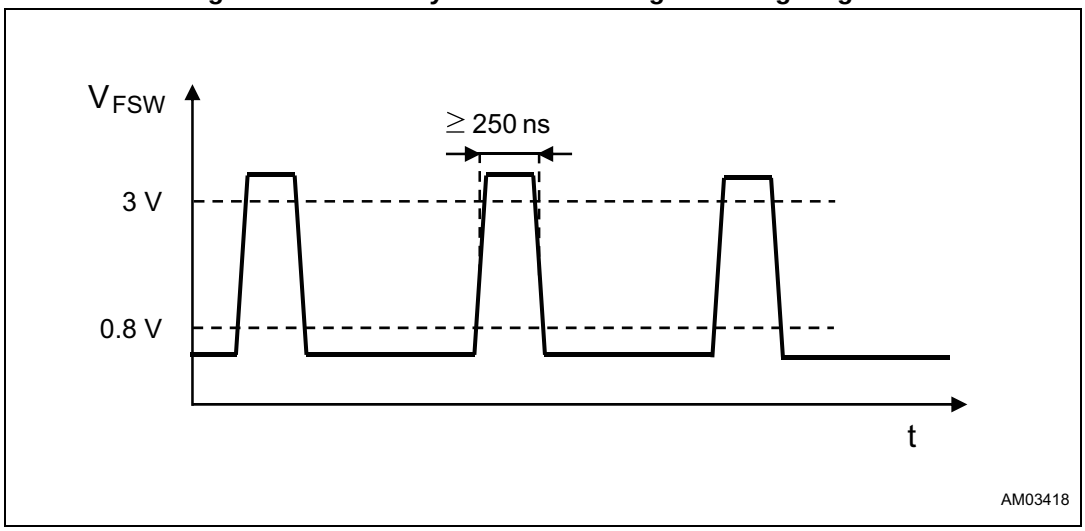
**Figure 7. Switching frequency vs. setting resistor at the FSW pin**




If the FSW pin is tied high (e.g.: connecting it to LDO3), a 600 kHz (typ.) default switching frequency is set.

In case the boost controller of the ALED6001 has to be externally synchronized, the FSW pin can be used as synchronization clock input. In this case the external clock must have a frequency in the 100 kHz - 1 MHz range and a 250 ns minimum pulse duration in order to ensure internal oscillator locking.

**Figure 8. External synchronization signal timing diagram**

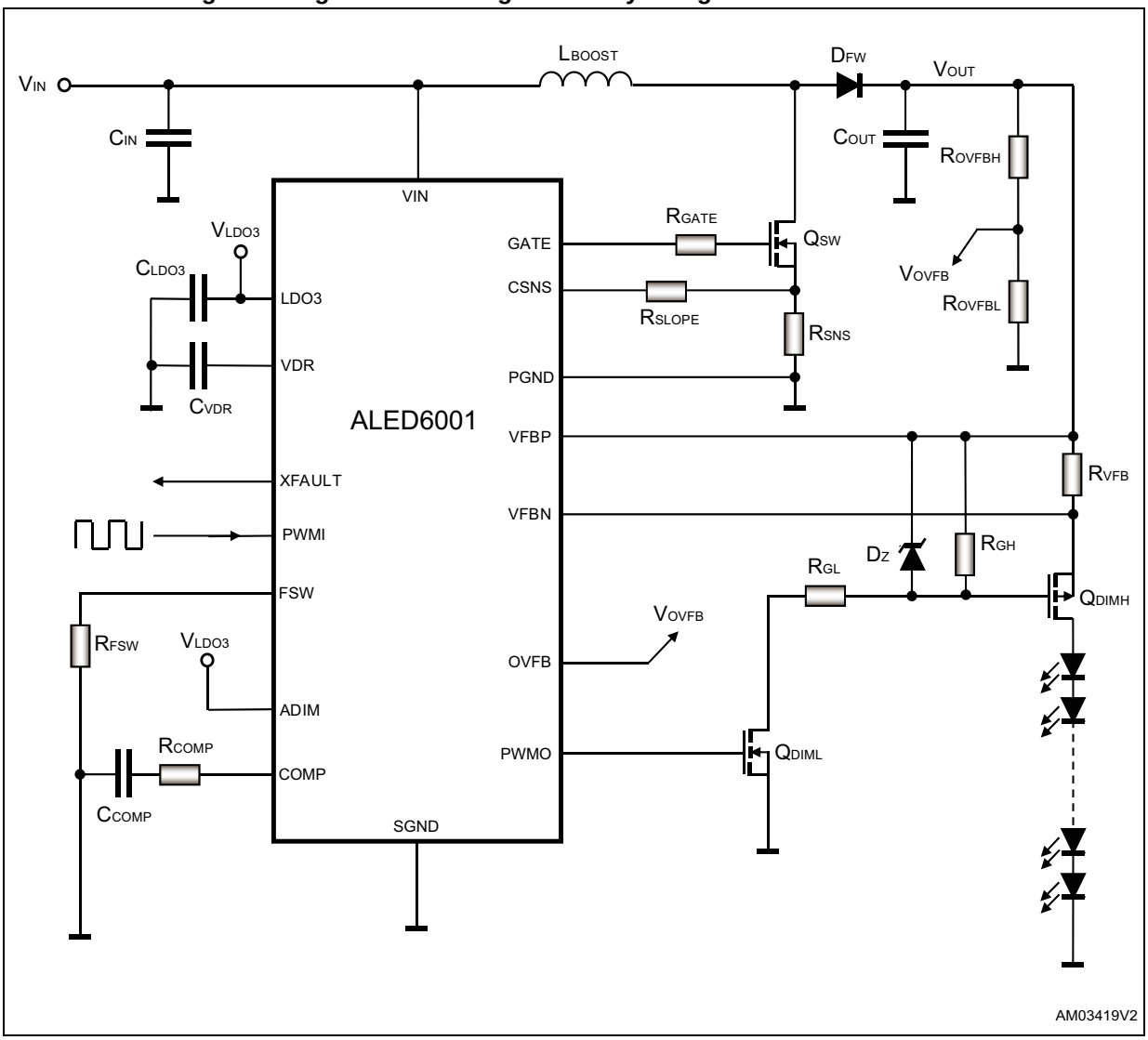



## 7.3 LED current regulation and brightness control

The brightness of the LEDs connected at the output of the ALED6001 can be controlled by applying the desired PWM signal at the PWMI pin. The boost controller is turned on and off according to the duty cycle of the PWMI control signal. When the PWMI is high (and the soft-start has been completed), the output (LED) current is regulated by keeping constant the voltage drop across the external sensing resistor connected between the VFBP and VFBN pins.

A buffered replica of PWMI is available at the PWMO for driving a dimming N-channel MOSFET when superior dimming performance is required. In some applications a high-side dimming switch could be desirable (e.g.: protection against output short-circuit to ground or LED strings using the chassis as return) and a P-channel MOSFET can be used as shown in *Figure 9*. Some additional components may be needed to avoid excessive voltage between the gate and the source of such MOSFET.

**Figure 9. High-side dimming control by using a P-channel MOSFET**

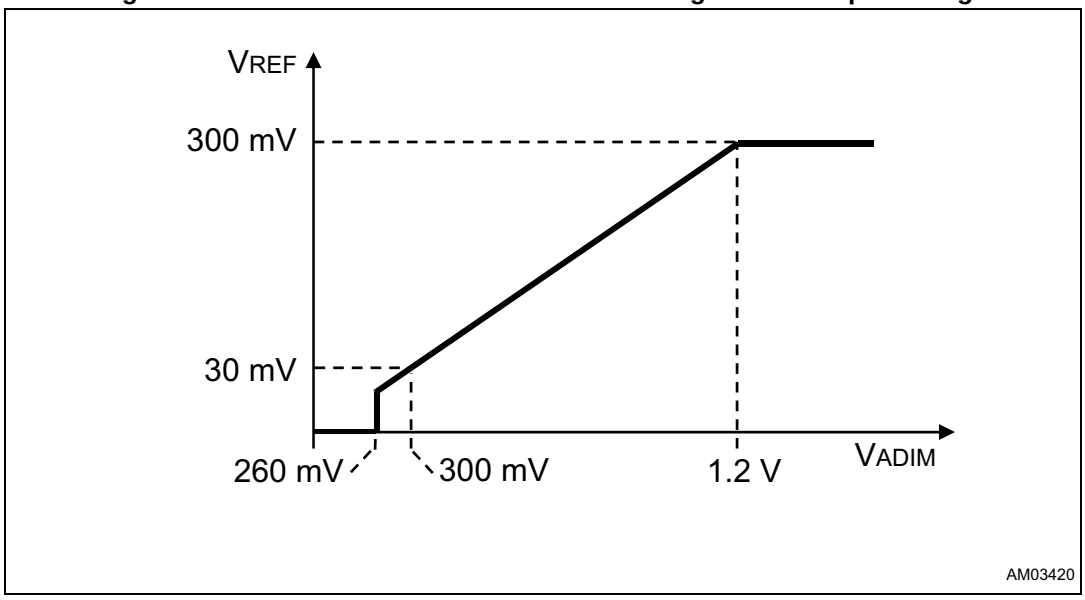



The regulation loop continuously compares the differential voltage drop with an internal reference and adjusts the switching duty cycle accordingly. In order to provide design flexibility and analog dimming capability, the internal feedback reference can be changed through the ADIM pin. As visible in *Figure 10*, the reference voltage is proportional to the voltage at the ADIM pin within a limited range.

**Equation 5**

$$I_{LED} = \begin{cases} 0 & \text{if } V_{ADIM} < 260mV \\ \frac{0.3 \cdot (V_{ADIM} - 200\text{mV})}{R_{VFB}} & \text{if } 300\text{mV} \le V_{ADIM} \le 1.2\text{V} \\ \frac{300\text{mV}}{R_{VFB}} & \text{if } V_{ADIM} > 1.2V \end{cases}$$

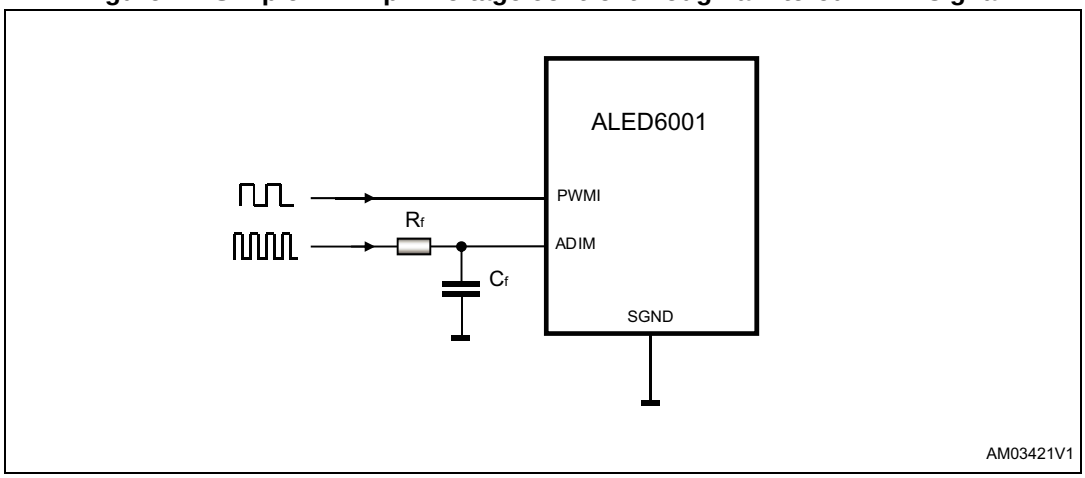
**Figure 10. Differential feedback reference voltage vs. ADIM pin voltage**




In case a fixed output (LED) current is needed or simple PWM dimming is used, the ADIM pin must be connected to the central tap of a resistor divider (supplied by the LDO3 pin) for the desired LED current level. Because of the best LED current accuracy overtemperature is obtained at full scale, a voltage higher than 1.2 V should be applied at the ADIM pin in case the analog dimming is not needed.

If an analog dimming control is required, the voltage at the ADIM pin can be changed runtime within its functional range. A simple way to perform an analog dimming is easily achieved by extracting the average value of a PWM signal through a simple RC low-pass filter (*Figure 10*).

**Figure 11. Simple ADIM pin voltage control through a filtered PWM signal**




If the voltage at the ADIM pin is lower than 240 mV, both the PWMO and GATE pins are forced low and the boost converter is temporary disabled. As soon as the ADIM pin voltage is driven inside the operating range, normal operation is resumed.

## 7.4 Device protections

### 7.4.1 Linear regulators undervoltage lockout

Both the 5 V and 3.3 V linear regulators of the ALED6001 are equipped with an undervoltage lockout (UVLO) protection. The UVLO protections avoid improper device operation in case at least one of the two outputs (VDR and LDO3) is below the allowed level. In particular, the ALED6001 performs the soft-start sequence only after both VDR and LDO3 cross their respective upper UVLO threshold.

### 7.4.2 Power switch overcurrent

The current flowing through the external Power MOSFET is monitored, cycle-by-cycle, by sensing the voltage across the shunt resistor in series with its source. If the voltage drop exceeds the overcurrent protection (OCP) level, the ongoing switching cycle is suddenly terminated (cycle-by-cycle Power MOSFET OCP). Normal operation is automatically resumed once the root cause has been removed. The XFAULT pin is not affected by OCP.

As explained in *Section 7.2 on page 12* the slope compensation is added by injecting a sawtooth current at the CSNS pin. As a consequence, the OCP threshold depends on both the slope compensation amount and the boost converter's operating point:

**Equation 6**

$$I_{MOS,OCP} = \frac{V_{CSNS,OCP} - D \bullet I_{SL} \bullet R_{SLOPE}}{R_{SNS}}$$

Where $V_{CSNS,OCP}$ = 360 mV (typ.), $I_{SL}$ = 50 µA (typ.) and *D* is the switching duty cycle.

### 7.4.3 Output overvoltage and OVFB pin disconnection

The output overvoltage fault detection is achieved by comparing the voltage at the OVFB pin with an internal threshold. Because of this fault can potentially damage both the device and the external components, a latched turn off condition is triggered once this event has been detected. A resistor divider connected to the output of the boost converter sets the desired OVP threshold.

The OVFB is internally pulled-up in order to protect the device against an OVFB pin disconnection fault: if the pin is left floating, the OVP is suddenly triggered regardless of the output voltage level. This small pull-up current ($I_{OVFB,PU}$) must be taken into account when designing an OVP output divider involving high resistance values. *Equation 7* allows setting the desired output OVP level ($R_{OVPH}$ and $R_{OVPL}$ are the two resistors of the output divider whose central tap is connected to the OVFB pin of the ALED6001):

**Equation 7**

$$V_{OUT,OVP} = \frac{R_{OVPH} + R_{OVPL}}{R_{OVPL}} V_{TH,OVFB} - R_{OVPL} \bullet I_{OVFB,PU}$$

Where $V_{TH,OVFB}$ = 1.2 V (typ.) and $I_{OVFB,PU}$ = 1 µA (typ.).

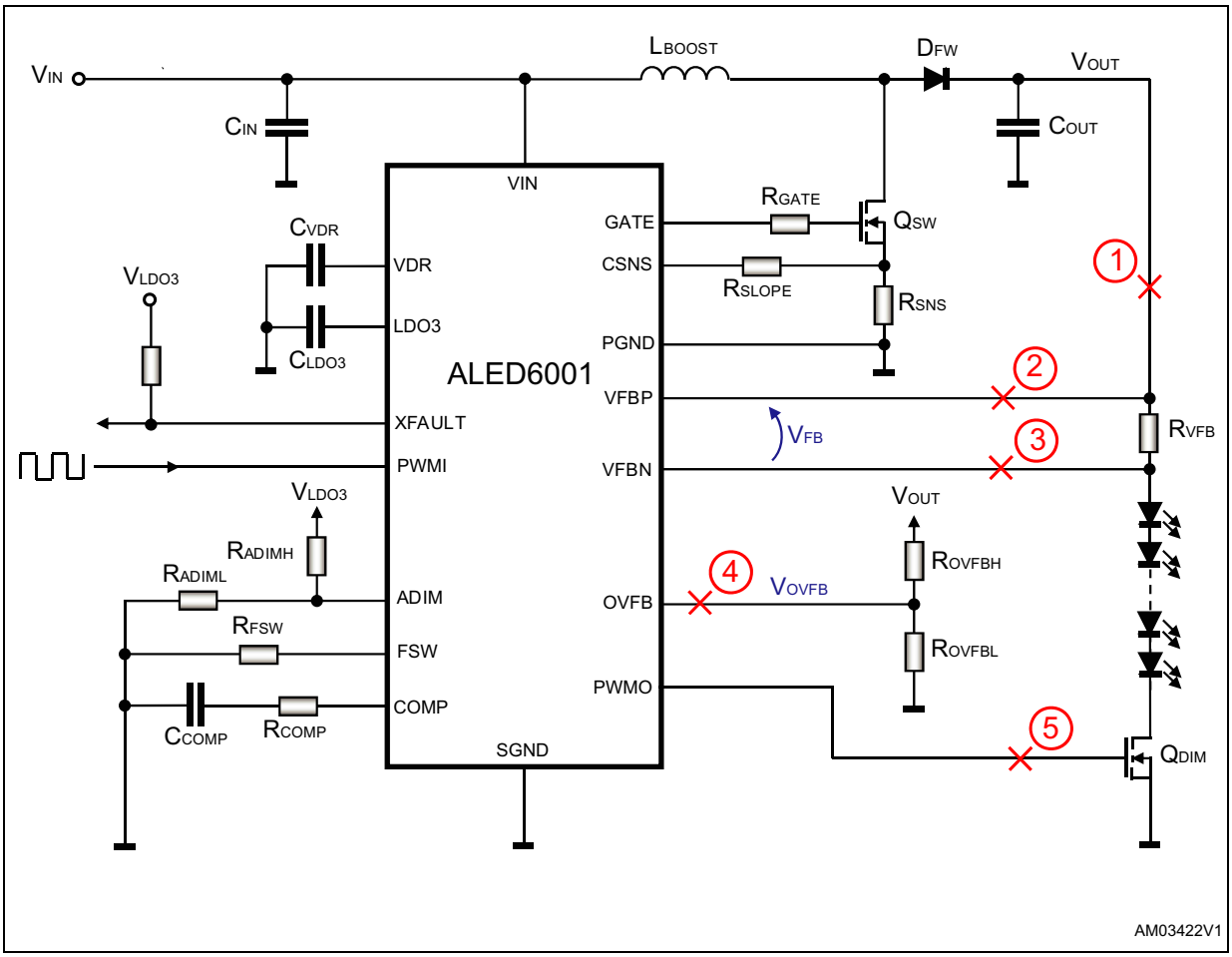
Once the OVP faulty condition is detected, the ALED6001 device suddenly stops switching. Both GATE and PWMO are forced low and the XFAULT pin is lowered. The condition is latched and normal operation is resumed by toggling the PWMI pin (PWMI has to be low for more than 10 ms) after the root cause has been removed.

### 7.4.4 Output rail disconnection detection or output short-circuit to ground

If the connection between the output rail and the output sensing resistor is lost, the voltage of both the VFBP and VFBN pins falls down to zero. The ALED6001 detects this faulty condition by comparing the absolute voltage of both VFBP and VFBN pins with an internal 3.3 V threshold and latches-off as a consequence (the GATE and PWMO pins forced low, XFAULT pin lowered). Normal operation is resumed by toggling the PWMI pin (PWMI has to be low for more than 10 ms) after the root cause has been removed.

When the ALED6001 is operating with a boost topology, a similar condition occurs in case of output-to-ground short-circuit. Of course, because of the inherent path between input and output, a real protection against this faulty condition can be achieved only if the device is capable of disconnecting the boost output by means of the dimming switch (e.g.: in case a P-channel MOSFET is used as a high-side dimming switch).

**Figure 12. Load disconnection (1 and 5), open feedback (2 and 3) and open OVFB faulty conditions**



### 7.4.5 Thermal shutdown

The ALED6001 implements an autorestarting thermal protection in order to avoid damages due to excessive die temperature. Once the chip temperature reaches the upper overtemperature protection (OTP) threshold, the ongoing operation is suddenly stopped, both the PWMO and XFAULT pins are held low and the 5 V linear regulator (VDR pin) is turned off. As soon as the die temperature drops below the autorestarting threshold, a new soft-start sequence takes place if the PWMI pin is still high and a 1 ms (typ.) deglitch delay has expired.

The XFAULT pin goes low as soon as the OTP threshold is crossed and it is released once the device temperature drops below a third threshold, lower than the restart one, in order to provide a stable information to the host system.

**Table 7. Faulty conditions management summary**

| Faulty condition | | Detection mechanism | Consequence |
|---|---|---|---|
| 1 | Output rail/load disconnection | $V_{VFBx}$<3.5 V | Device turning-off (latched condition). GATE, PWMO and XFAULT pins are forced low. |
| 2 | Open feedback (VFBP) | $V_{VFBP}$ - $_{VVFBN}$ <-120 mV | |
| 3 | Open feedback (VFBN) | $V_{VFBP}$ - $_{VVFBN}$ > 600 mV | |
| | LED overcurrent | | |
| | **Output to GND short-circuit**(1) | | |
| 4 | Open OVFB path | $V_{OVFB}$ > 1.2 V (internal pull-up) | |
| 5 | Open PWMO (loss of dimming MOSFET control) | $V_{OVFB}$ > 1.2 V | |
| Output overvoltage | | | |
| Power switch overcurrent | | $V_{CSNS}$ > 360 mV | Ongoing switching cycle terminated |
| IC overtemperature | | $T_J$ > 160 °C (typ.) | Device turning-off (VDR off, LDO3 active). GATE, PWMO and XFAULT pins are forced low. Autorestart if $T_J$ < 140 °C (typ.) and PWMI still high. XFAULT pin is released If $T_J$ <120 °C (typ.). |

1. Output-to-ground short-circuit protection can be achieved only if the device can effectively disconnect the output by acting on the PWMO pin (e.g.: a high-side P-channel MOSFET is used as a dimming switch).

# 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

## 8.1 HTSSOP-16 package information

**Figure 13. HTSSOP-16 package outline**

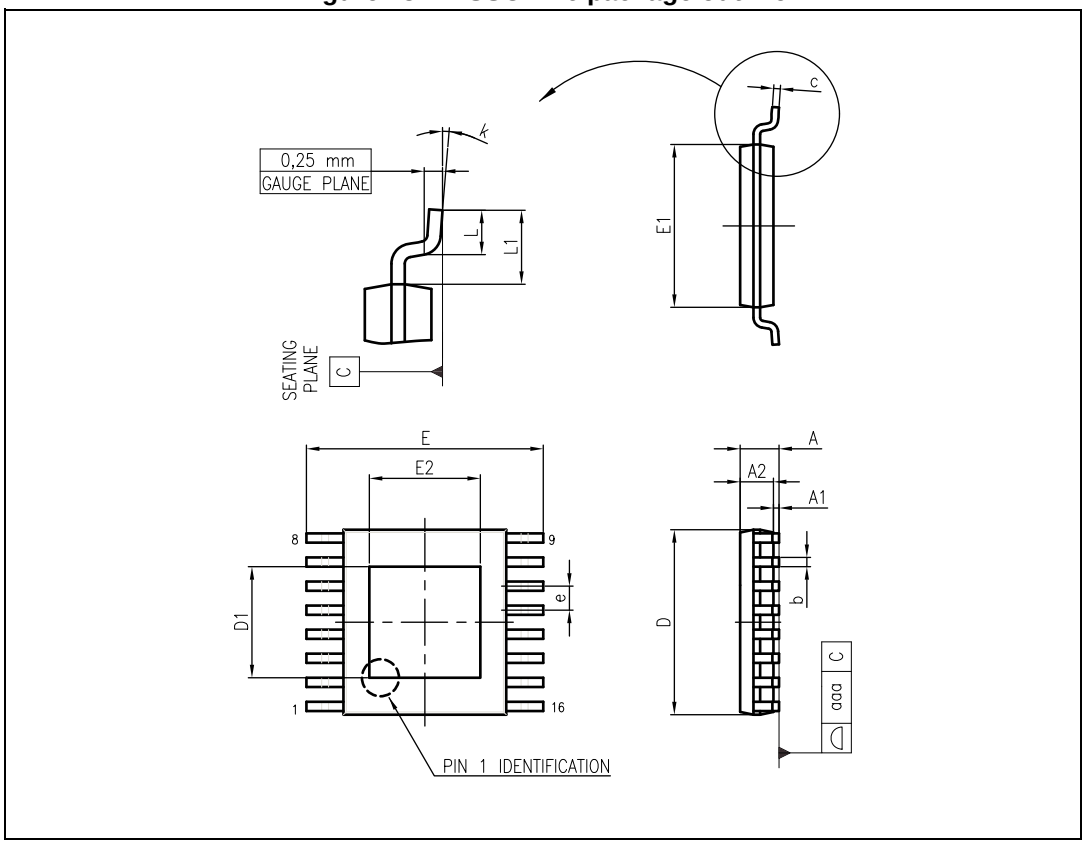


**Table 8. HTSSOP-16 package mechanical data(1)**

| Symbol | Dimensions (mm) | | | Note |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| A | | | 1.20 | |
| A1 | | | 0.15 | |
| A2 | 0.80 | 1.00 | 1.05 | |
| b | 0.19 | | 0.30 | |
| c | 0.09 | | 0.20 | |
| D | 4.90 | 5.00 | 5.10 | (2) |
| D1 | | 3.00 | | (3) |
| E | 6.20 | 6.40 | 6.60 | |
| E1 | 4.30 | 4.40 | 4.50 | (4) |
| E2 | | 3.00 | | (3) |
| e | | 0.65 | | |
| L | 0.45 | 0.60 | 0.75 | |
| L1 | | 1.00 | | |
| k | 0.00 | | 8.00 | |
| aaa | | | 0.10 | |

1. HTSSOP stands for “Thermally Enhanced Variations”.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
3. The size of exposed pad is variable depending of leadframe design pad size. End user should verify “D1” and “E2” dimensions for each device application.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

# 9 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 01-Oct-2014 | 1 | Initial release. |
| 17-Nov-2015 | 2 | Updated features in cover page.<br>Minor text changes. |