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Designer's Guide to the ISL55210 and ISL55211 Evaluation Boards

Circuit Comments

The ISL55210 (and fixed gain ISL55211) wideband differential I/O amplifiers are intended principally as the last stage interface to high performance 12 to 16-bit ADC's. While these are very capable FDA type devices, the EVM is configured to support a particular type of last stage interface to ADC's. Specifically, it is set up to take a single-ended input from a 50Ω source and convert it to differential using an input 1:1.4 turns ratio transformer driving the two input resistors to the amplifier. The outputs also drive differentially on the EVM but, since most lab equipment is single-ended 50Ω, the EVM also includes a differential resistive divider as part of its output load, which then drives through a 1:1 transformer to get an attenuated replica of the differential output swing available as a single-ended signal to 50Ω test equipment.

The input transformer necessarily makes this implementation AC-coupled and the EVM adds 1µF in several places to protect against accidental DC shorts. The particular transformer used (Mini-Circuits, ADT2-1T) limits the usable bandwidth for the signal path to approximately 100kHz to 400MHz while the amplifiers themselves provide in excess of 1GHz closed loop bandwidth. The 1:1 transformer used on the output side is only there to passively sense the on board differential output signal and would not normally be used in a final application driving a differential ADC.

The EVM schematic is shown in Figure 1. To provide a ready to use circuit, while retaining some flexibility to change the configurations, some elements are not populated in the EVM as delivered. Elements that are not populated are shown as green in the schematic of Figure 1.

The nominal supply voltage for the board and devices is a single 3.3V supply. From this, the ISL55210/11 TQFN-EVAL1Z generates an internal common mode voltage of approximately 1.2V. That voltage can be overridden by populating the two resistors and potentiometer shown as R19 to R21 in Figure 1.

The primary test purpose for this board is to implement different interstage differential passive filters intended for the ADC interface along with the ADC input impedances. The board is delivered with only the output resistors loaded to give a 200Ω differential load. This is done using the two 85Ω resistors as R9 and R10, then the four 0Ω elements (R10, R12, R24, and R25) and finally the two shunt elements R13 and R14 set to 35.5Ω. The 50Ω measurement load on the output side of the 1:1 transformer reflecting in parallel with the two 35Ω resistors takes the nominal AC shunt impedance to 71Ω||50Ω = 29.3Ω. This adds to the two 85Ω series output elements to give a total load across the amplifier outputs of 170Ω + 29.3Ω = 199.3Ω.

To test a particular ADC interface RLC filter and converter input impedance, we would replace R11 and R12 with RF chip inductors, load C10 and C11 with the specified ADC input capacitance and R26 with the specified ADC differential input resistance. With these loaded, the remaining resistive elements (R24, R25, R13, R14) are set to hit a desired total parallel impedance to implement the desired filter (must be less than the ADC input differential resistance) and achieve a 25Ω source looking into each side of the tap point transformer.

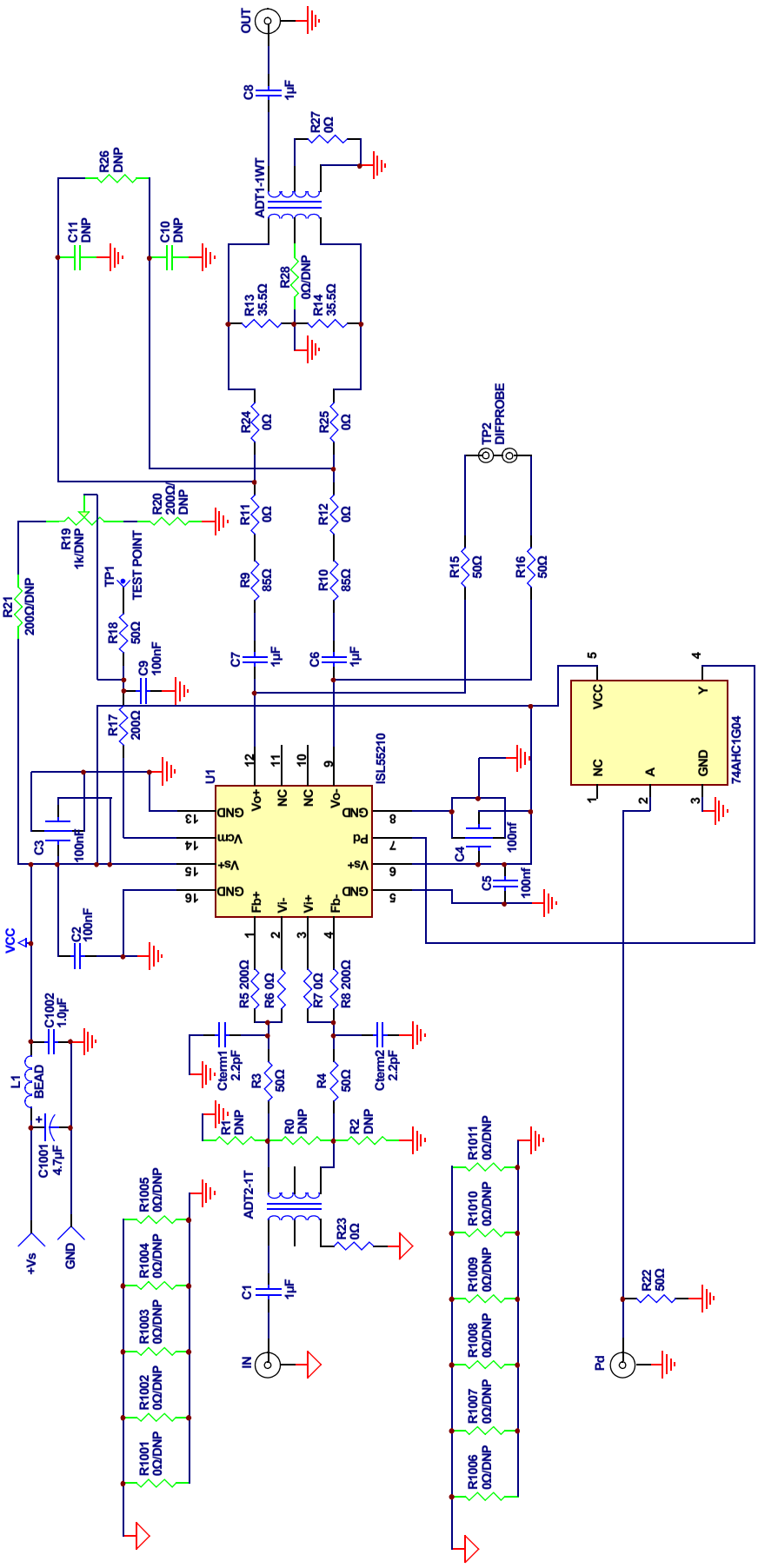

FIGURE 1. ISL55210/11 TQFN-EVAL1Z BOARD SCHEMATIC

Frequency Response Measurements Using the ISL55210

The output interface as delivered, gives a 200Ω differential load to the amplifier while providing a very good source match to 50Ω looking back into the 1:1 transformer. To do this, it necessarily inserts an attenuation into this measurement path. For the values shown above, this is a 0.147V/V gain from the amplifier differential outputs to the measurement 50Ω or -16.64dB. The two transformers also add about 0.4dB insertion loss midband for each of them. The amplifier is configured to provide a 1.4*4 = 5.6V/V gain from the single-ended input to differential output voltage (or 14.96dB). Including the insertion loss and measurement path loss, the board as delivered will measure approximately 14.96dB – 16.64dB – 0.8dB = -2.48dB midband gain using a network analyzer. The measured response of Figure 2 shows very close to this -2.5dB measured response. Here, we also stepped the input test power up from -11dBm to +1dB in 6dB steps. This is producing an output swing stepping from $1V_{P-P}$, $2V_{P-P}$, and $4V_{P-P}$. The $4V_{P-P}$ output is showing the effect of slew limiting at approximately 744MHz (the glitch in the response). The actual high and low frequency -3dB points are being set by the input transformer. This device is specified to give approximately a 400kHz to 450MHz -3dB span and we do see the higher end cutoff of that transformer in the sweep. Accounting for the reduced input amplitude delivered by this bandlimiting transformer, the glitch at 744MHz solves to an implied differential slew rate of 5440V/µs.

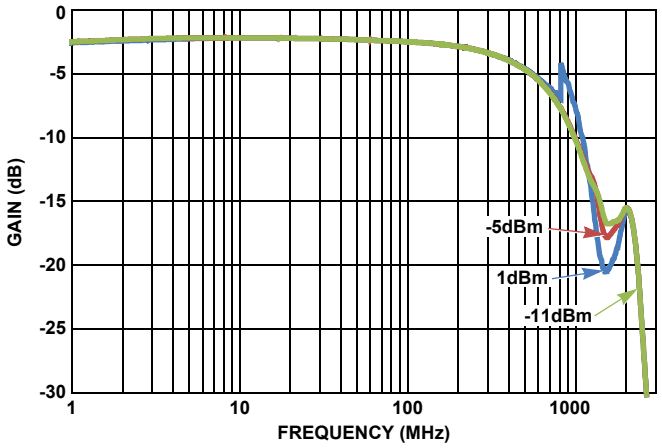

FIGURE 2. MEASURED RESPONSE PARAMETRIC ON INPUT POWER

Adding back in the 16.24dB measurement path loss and 0.4dB 1:1 output transformer insertion loss, scales this plot to show the actual frequency response from the input to the differential outputs of the ISL55210.

This is slightly below the predicted 14.96dB, since the input transformer also has a slight insertion loss of approximate 0.4dB.

To easily change the gain on a board, using the ISL55210 change the feedback resistors R5 and R8 from the 200Ω shown in Figure 1. Increasing these to 400Ω for instance will increase the gain to the output differential voltage by 6dB or up to 21dB for the board as delivered. The input resistors R3 and R4 are set to provide a match to a 50Ω source through the 1:2 ohm ratio input transformer. To scale this resistor up, while retaining a match, R0 is included in the layout. If the sum of R3 + R4 does not provide the desired termination impedance (they both go to the virtual ground nodes of the amplifier inputs – so the differential impedance is simply their sum), adding R0 as a parallel element can be used to achieve the desired input match with no gain interaction. This resistor is used for the ISL55211 since its internal resistors are scaled up. R1 and R2 are not populated but intended to provide a means of level shifting an output common mode voltage higher than nominal back to an input common mode voltage that is in range.

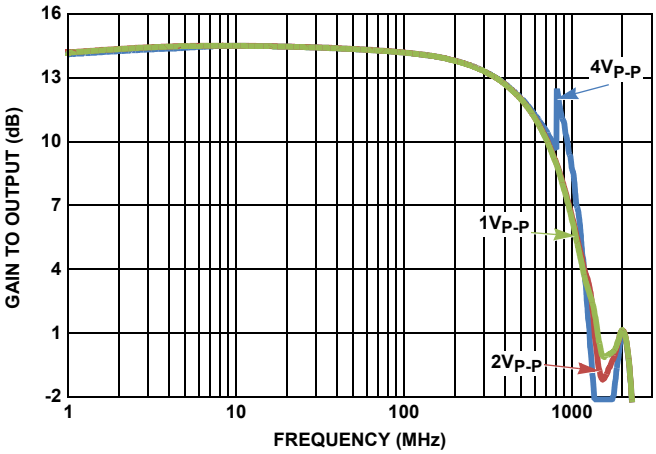

FIGURE 3. FREQUENCY RESPONSE NORMALIZED TO AMPLIFIER OUTPUTS

Taking the circuit of Figure 1 and stepping just the two feedback resistors up from 200Ω to 800Ω gives the frequency response family of Figure 4. Here, the response curves are normalized to come in at 0dB midband gain, to show the change in BW more clearly, but the actual gain to the differential outputs is stepping up from 14.9dB to 27dB. The two inverting node capacitors in Figure 1 (2.2pF) suppress a >1.5GHz resonance at the lower gains but are removed for the plots in Figure 4 when the feedback resistors are ≥600Ω. Initially, there is little apparent reduction in amplifier bandwidth at increased gains as the input transformer is setting the response. At the highest gain of 27dB, the $1V_{P-P}$ output bandwidth has reduced from 600MHz at a gain of 15dB to approximately 250MHz.

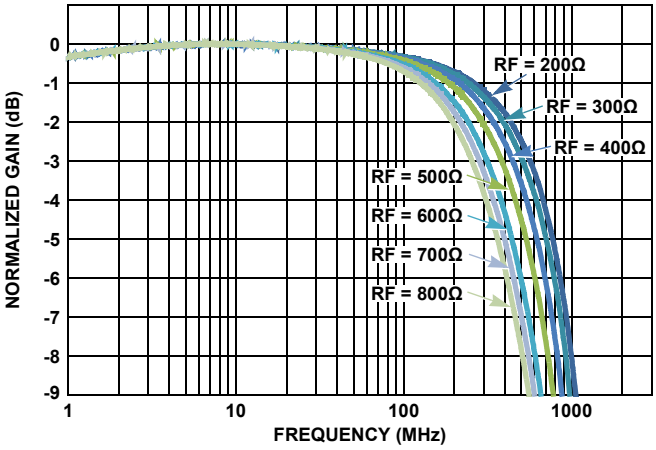

FIGURE 4. FREQUENCY RESPONSE vs AMPLIFIER GAIN SETTING $1V_{P-P}$ OUTPUT

On the other end of the frequency spectrum, the 1µF blocking caps and transformers set a high pass response that is flat above 200kHz. Using a 100Hz to 500MHz sweep shows this region in Figure 5.

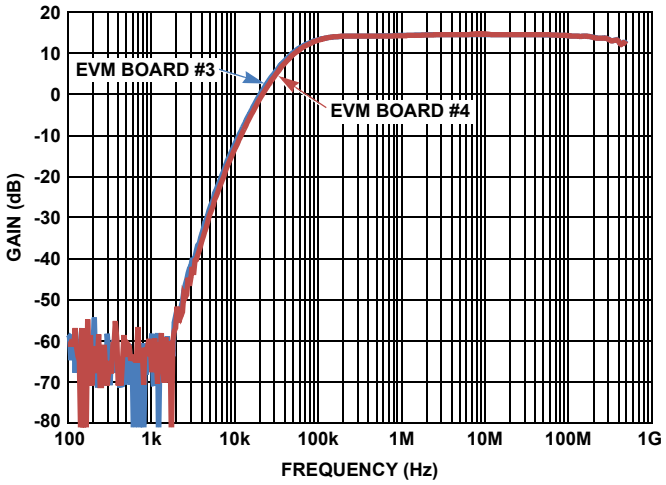

FIGURE 5. 100Hz TO 500MHz SWEEP OF THE FREQUENCY RESPONSE

Expanding this plot to show only the passband region is Figure 6. on 2 separate EVM boards.

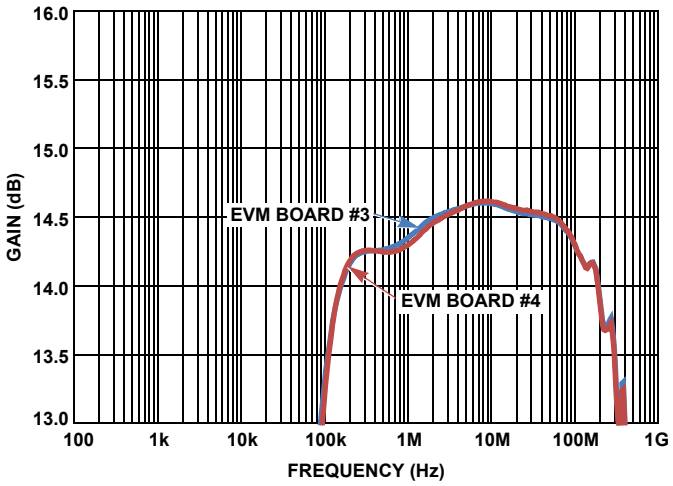

FIGURE 6. EXPANDED RESPONSE SHOWING PASSBAND DETAILS

Disable/Enable Control Pin

Going back to Figure 1, a single logic gate is included on the board to assert the shutdown control pin high. The 50Ω input termination to ground holds this inverter input low with no connection to the control pin, setting the logic output at $+V_{CC}$ turning the ISL55210 (or ISL55211) on. Driving this input control high will disable the ISL55210, reducing its supply current to <400µA.

Since the circuit of Figure 1 is a differential inverting FDA type topology, even with the amplifier turned off by the disable pin control, a signal path through the feedback elements will still be in place. Figure 7 shows a fixed 10MHz input signal with the disable control toggled at a 50kHz rate. The ISL55210 reaches an attenuated output signal within 4µs of the disable pin voltage and turns back on in less than 400ns.

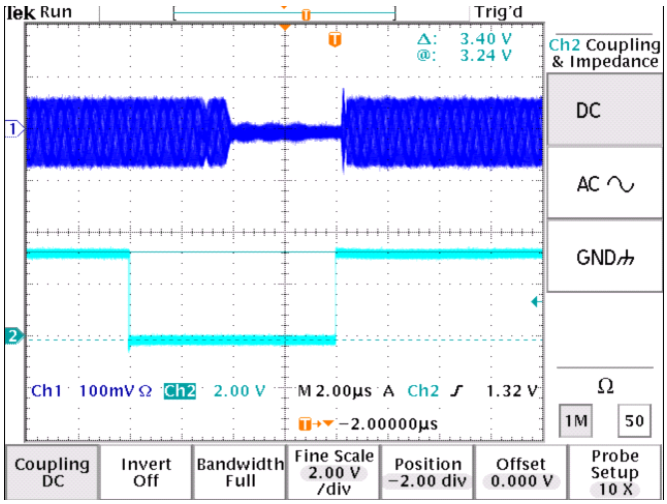

FIGURE 7. DISABLE/ENABLE TEST

Distortion Performance Using the ISL55210

The purely differential signal path of the ISL55210 gives extremely low harmonic distortion through high frequencies. Testing with a two tone input at equal test powers for each tone, will be reviewed here. In these tests, two signal generators at Fo±∆f are combined and applied to the input port. The 3rd order intermodulation terms will fall at Fo±3*∆f while the 2nd order intermodulation distortion terms will fall at 2*∆f and 2*Fo. For these tests, a ∆f = 1MHz was used giving 3rd order terms at ±3MHz away from Fo, and 2nd order terms at 2MHz and a 2*Fo. The 2MHz term was essentially unmeasurable due to the very high loop gain at low frequencies for the ISL55210, so it will not be reported. However, the 2*Fo term will often be the dominant spurious for the same reason – loop gain is rolling off at higher frequencies. In the SFDR plots, it is very important to consider that the IM2 data is physically the 2*Fo spurious and happening at 2X the average test frequency of the two input tones (which is what is shown on the x-axis). The IM3 data is physically very close in frequency to Fo and very difficult to filter as it is physically close to the x-axis frequency for the plots. It is the 2*Fo term that sets the SFDR limit in most cases but it can be easily attenuated by the RLC post filter option included on the EVM. For instance, a 120MHz filter implemented at the output of the ISL55210 will start to attenuate the 2*F0 IM2 term for test frequencies above 60MHz. This filter will also be helping with the simple 2nd and 3rd harmonic distortion terms as well. In this example, single tone test frequencies above 40MHz will see their HD3 term attenuated while 2nd harmonics for inputs above 60MHz will also start to be attenuated.

The intended application for the ISL55210 is to drive the differential inputs of the high speed Intersil ADC family. These devices generally have a specified maximum differential input voltage of $1.45V_{P-P}$. For SFDR testing, this maximum level is usually backed off by 1dB - or to about $1.31V_{P-P}$. Two equal test tones need to be half this level again to keep their envelope in range, or about $0.652V_{P-P}$ for each test tone at the differential output.

As an initial test, measure the IM2 and IM3 with just the 200Ω load at higher frequencies (before we add a 2nd order RLC filter for the IM2). Sweeping from 100MHz to 300MHz with $0.65V_{P-P}$ on each test tone at the differential output gives the SFDR results shown in Figure 8.

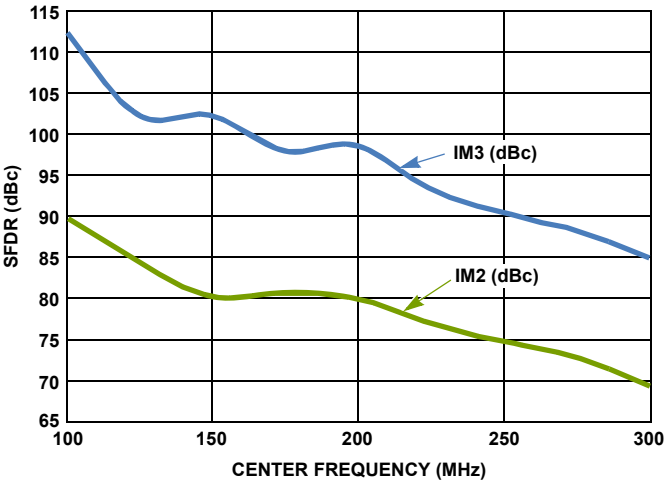

FIGURE 8. 2-TONE INTERMODULATION SFDR WITH 200Ω LOAD AND NO FILTERING

Now, to test the delivered SFDR in an example 1st Nyquist zone application, we will add an RLC filter to the board. SFDR can normally be improved by reducing the loading. In the circuit of Figure 8, the total load is the 200Ω feedback in parallel with 100Ω or 67Ω. We should be able to greatly improve the IM2 by going to a bit higher gain and lighter load in the filter. Going to a 400Ω feedback resistor only increases the noise gain from 3 to 5 and then going to a 354Ω differential filter load takes this test to a 122Ω load on each output – almost double the load of Figure 8. The filter introduces a 1dB insertion loss to the ADC input pins, so to deliver the same test level as if the converter were in place, the input signal level for this test needs to be reduced by not 6dB but 5dB. This will produce the same differential signal swing at the output of the filter as the prior test. The circuit is modified to this.

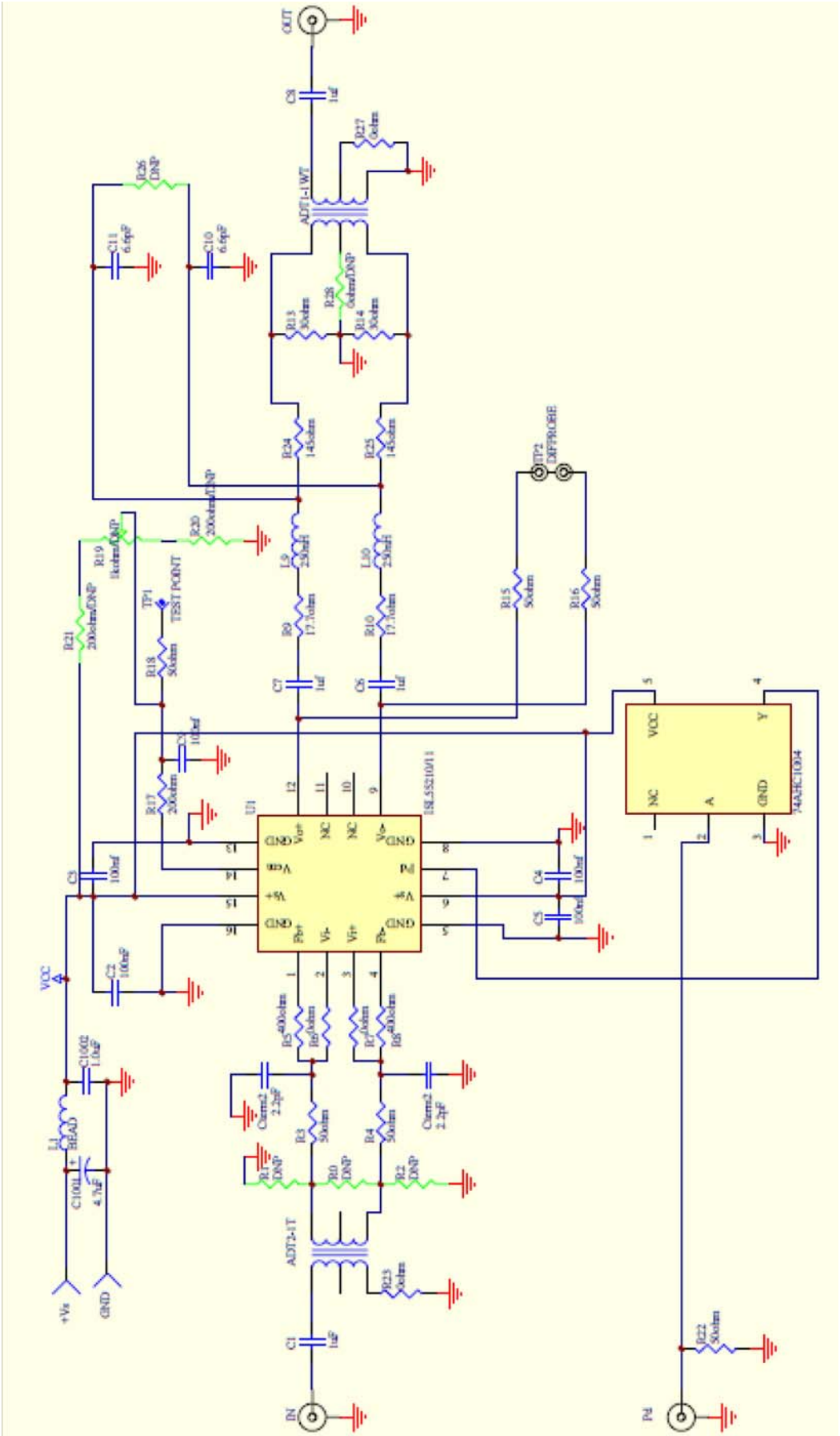

FIGURE 9. MODIFIED IM TEST CIRCUIT. INCREASED GAIN AND OUTPUT RLC FILTER

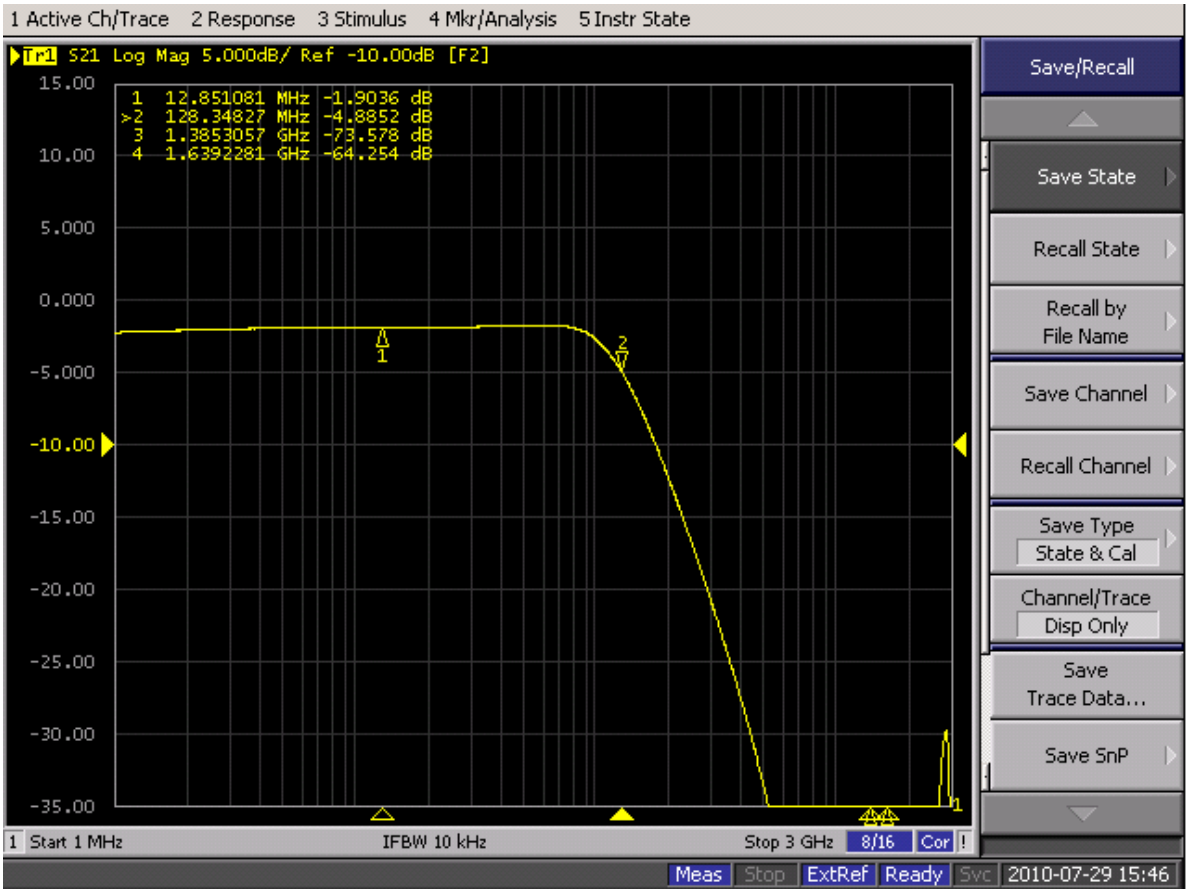

FIGURE 10. EVM BOARD WITH INCREASED GAIN AND RLC FILTER ADDED

The measured frequency response for this circuit is shown in Figure 10. This is a screen shot from the network analyzer so it is showing the gain after the -21.3 loss through the measurement path. It is showing a slight peaking and approximate 130MHz 2nd order roll-off very close to the expected filter shape.

As expected, this modification to the board greatly improved the IM2 terms. At 100MHz, we now see an IM2 of 92dBc SFDR vs the earlier 200Ω load test of 78dBc SFDR. The IM3 also improved and is actually hitting the measurement limit of the system (IM3 is probably better than what we are showing here). The IM2 at the output of the amplifier is coming up with frequency, but above 70MHz, the post filter is helping to hold it approximately flat (for the F1+F2 terms). The board is now delivering approximately 20dB gain from a single-ended input to a differential filtered output with very flat gain from 200kHz to 100MHz and exceptionally low IM spurious for a signal swing the would match the -1dBFS for the Intersil high speed ADC's.

Contact sales support for help with designing a filter for your application (http://www.intersil.com/contacts/).

The examples shown here use a particular set of transformers that seem to give good results. There are certainly alternate possible transformers (such as the 1:2 turn ratio ADT4-1WT) that can also be used on this board.

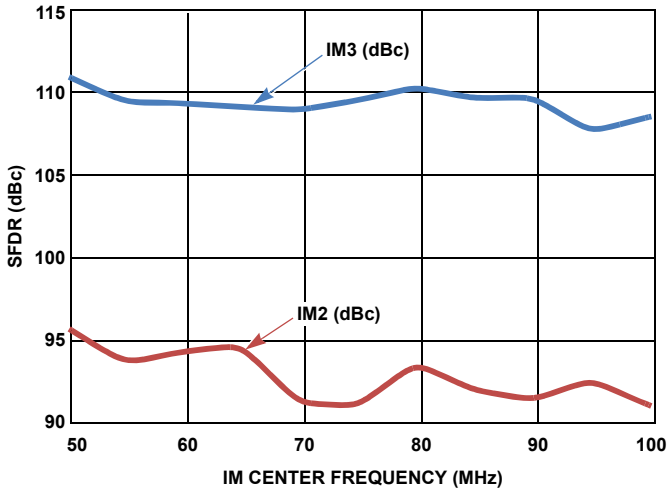

FIGURE 11. 50MHz TO 100MHz IM MEASUREMENTS WITH RLC FILTER