FDBL86066-F085

N-Channel POWERTRENCH® MOSFET

100 V, 240 A, 4.1 mΩ

Features

- Typical $R_{DS(on)}$ = 3.3 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 47 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current − Continuous, (V_{GS} = 10 V) T_C = 25°C (Note 1)	185	A
	Pulsed Drain Current, T_C = 25°C	(See Figure 4)	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	93.6	mJ
P_D	Power Dissipation	300	W
	Derate Above 25°C	2	W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting T_J = 25°C, L = 30 μH, I_{AS} = −79 A, V_{DD} = 100 V during inductor charging and V_{DD} = 0 V during time in avalanche.

ON Semiconductor®

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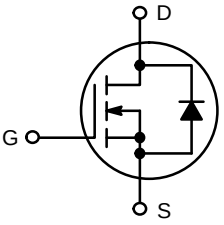
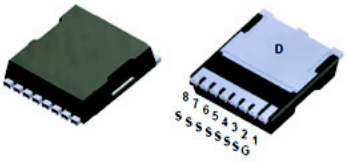
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
100 V	4.1 mΩ @ 10 V	240 A

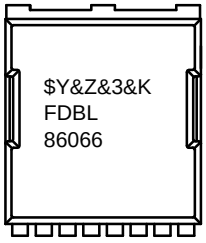


N-CHANNEL MOSFET



H−PSOF8L
CASE 100CU

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDBL86066	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3)	43	

3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
I_{DSS}	Drain-to-Source Leakage Current	V_{DS} = 100 V, V_{GS} = 0 V T_J = 25°C T_J = 175°C (Note 4)	 – –	 – –	 1 1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	2.9	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 80 A T_J = 25°C T_J = 175°C (Note 4)	 – –	 3.3 7.3	 4.1 8.8	mΩ
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	3240	–	pF
C_{oss}	Output Capacitance		–	1950	–	pF
C_{rss}	Reverse Transfer Capacitance		–	26	–	pF
R_g	Gate Resistance	V_{GS} = 0.5 V, f = 1 MHz	–	0.5	–	Ω
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 80 A	–	47	69	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 V to 2 V, V_{DD} = 50 V, I_D = 80 A	–	6	–	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 80 A	–	15	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 50 V, I_D = 80 A	–	10	–	nC
SWITCHING CHARACTERISTICS						
t_{on}	Turn-On Time	V_{DD} = 50 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	–	35	ns
$t_{d(on)}$	Turn-On Delay		–	18	–	ns
t_r	Rise Time		–	9	–	ns
$t_{d(off)}$	Turn-Off Delay		–	36	–	ns
t_f	Fall Time		–	13	–	ns
t_{off}	Turn-Off Time		–	–	68	ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	I_{SD} = 80 A, V_{GS} = 0 V	–	0.9	1.25	V
		I_{SD} = 40 A, V_{GS} = 0 V	–	0.85	1.2	
t_{rr}	Reverse Recovery Time	I_F = 80 A, dI_{SD}/dt = 300 A/μs	–	36	54	ns
Q_{rr}	Reverse Recovery Charge		–	84	126	nC
t_{rr}	Reverse Recovery Time	I_F = 80 A, dI_{SD}/dt = 1000 A/μs	–	32	48	ns
Q_{rr}	Reverse Recovery Charge		–	243	365	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

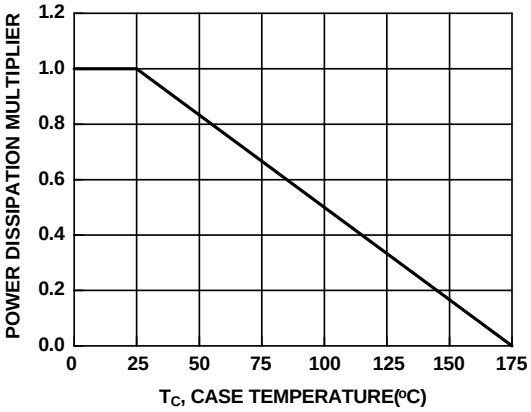


Figure 1. Normalized Power Dissipation vs. Case Temperature

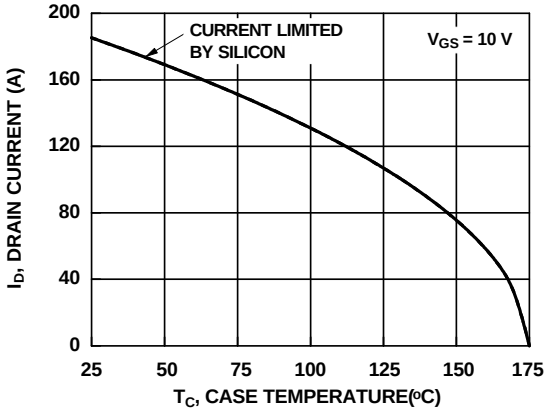


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

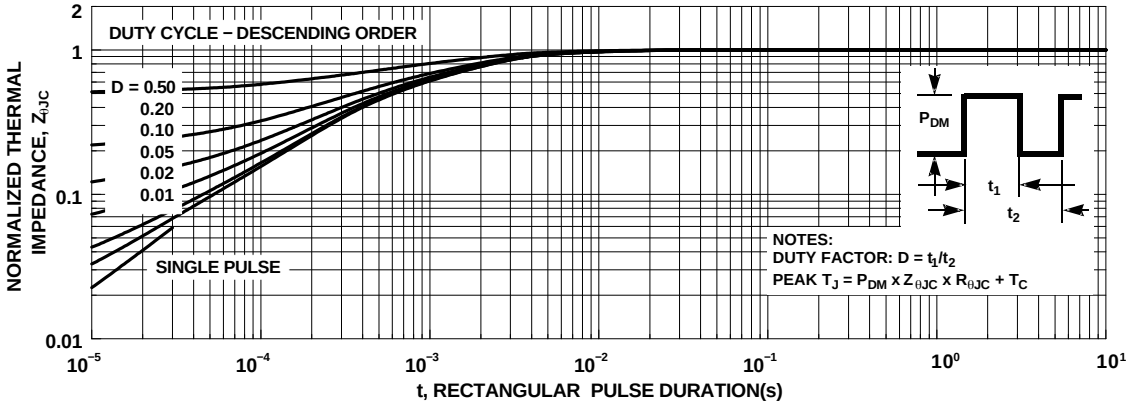


Figure 3. Normalized Maximum Transient Thermal Impedance

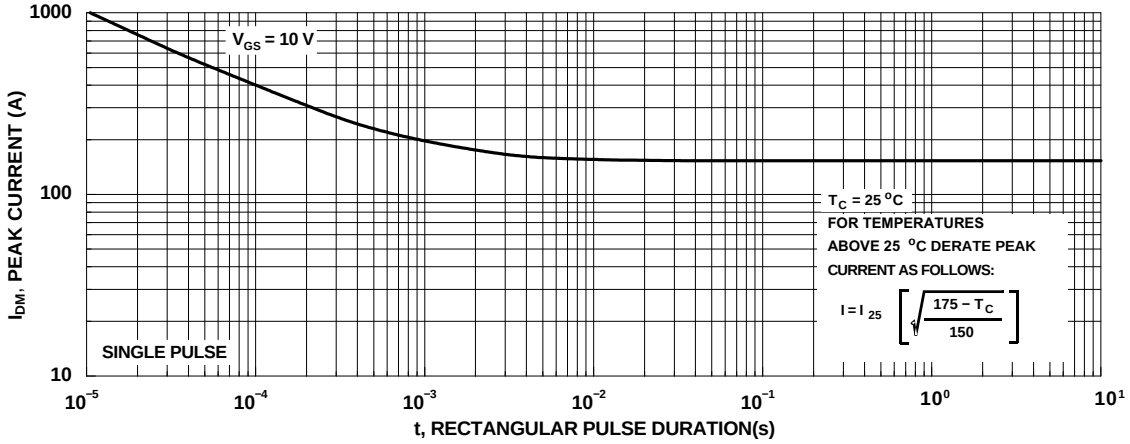


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

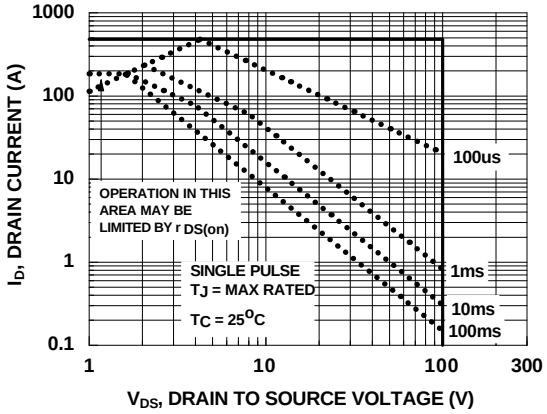


Figure 5. Forward Bias Safe Operating Area

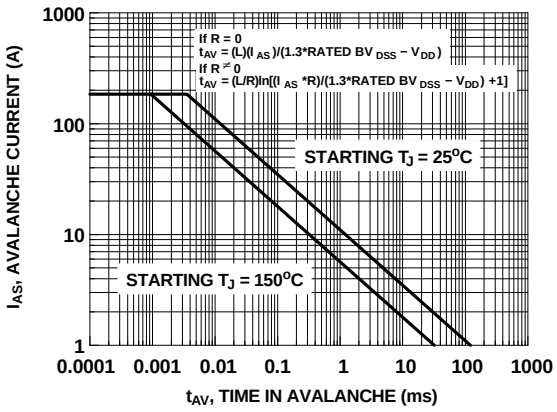


Figure 6. Unclamped Inductive Switching Capability

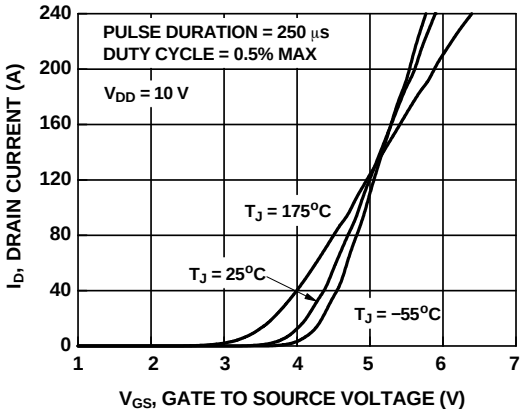


Figure 7. Transfer Characteristics

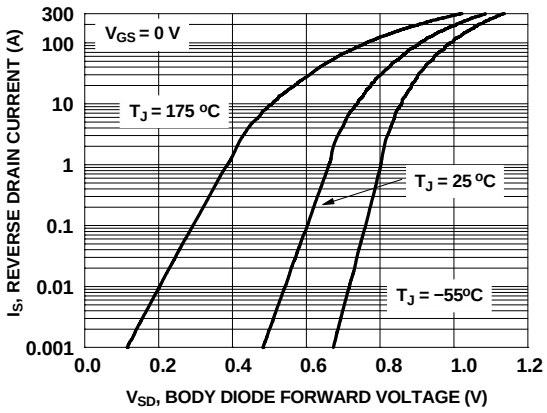


Figure 8. Forward Diode Characteristics

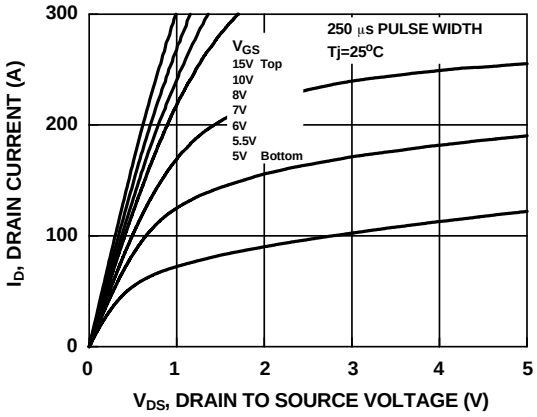


Figure 9. Saturation Characteristics

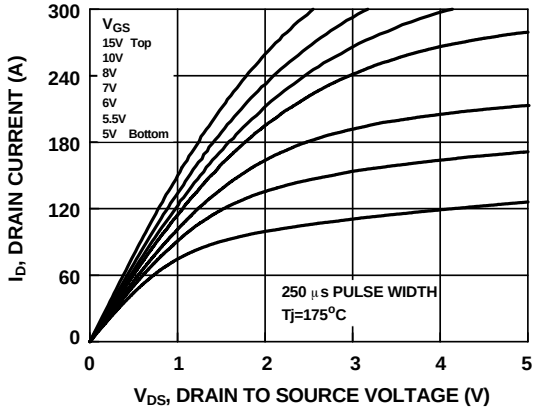


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

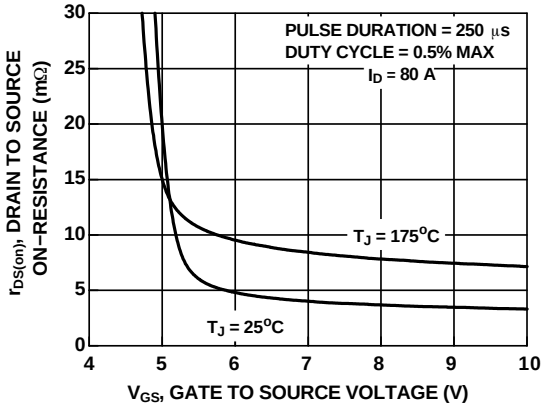


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

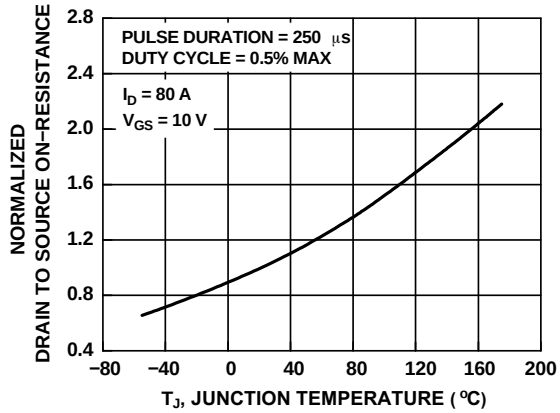


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

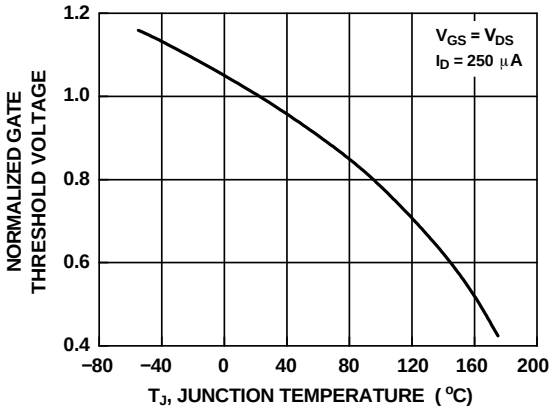


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

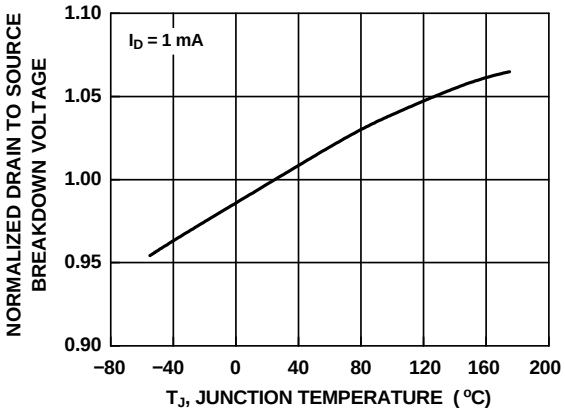


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

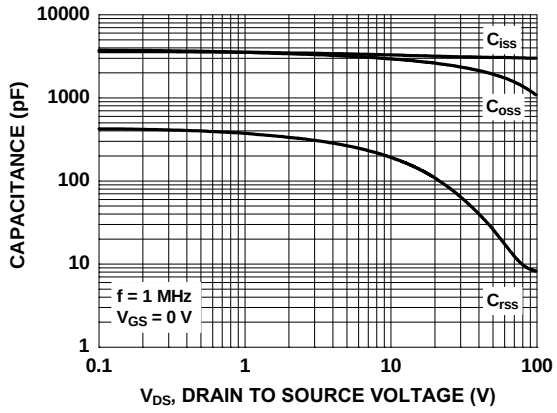


Figure 15. Capacitance vs. Drain to Source Voltage

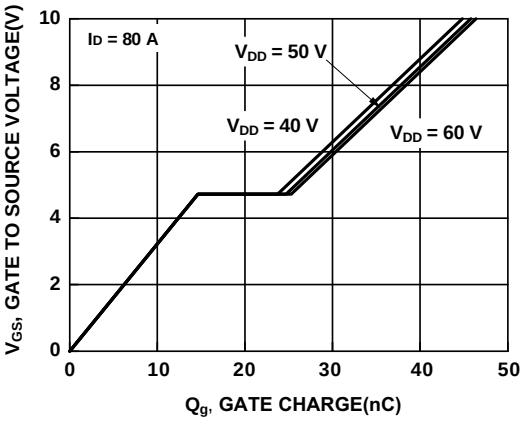
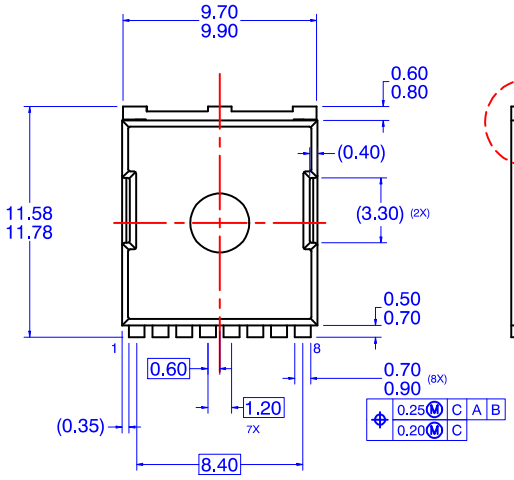


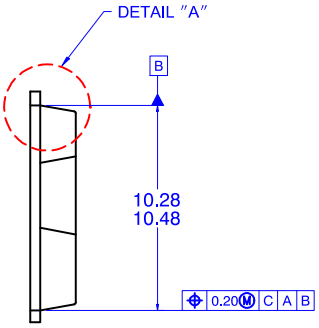
Figure 16. Gate Charge vs. Gate to Source Voltage

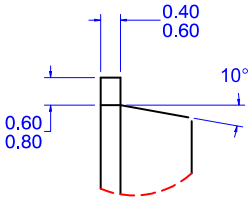
PACKAGE DIMENSIONS

H−PSOF8L 11.68x9.80
CASE 100CU
ISSUE O

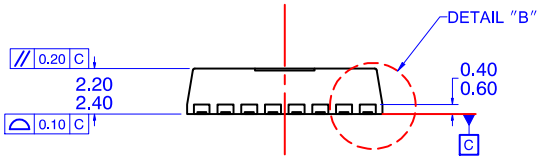


TOP VIEW

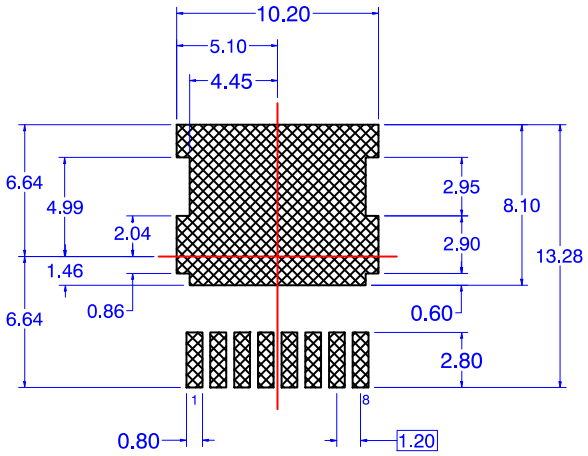




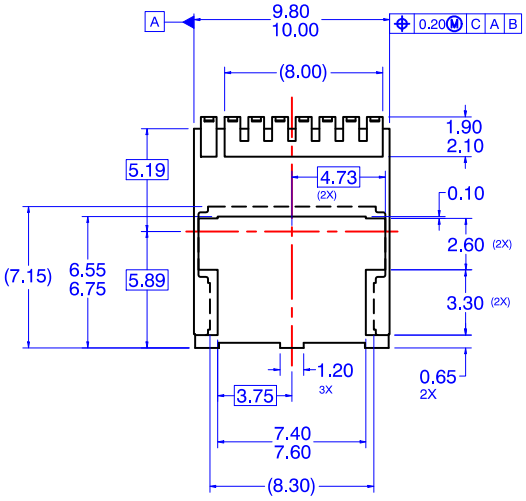
DETAIL "A"



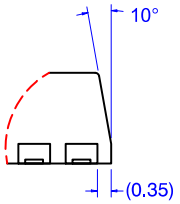
SIDE VIEW



LAND PATTERN
RECOMMENDATION



BOTTOM VIEW



DETAIL "B"

NOTES: UNLESS OTHERWISE SPECIFIED
A) PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A, DATED NOVEMBER 2009.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Marking	Package	Reel Size	Tape Width	Quantity
FDBL86066−F085	FDBL86066	H−PSOF8L (Pb-Free / Halogen Free)	13″	24 mm	2000 Units

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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