# PIC18F2420/2520/4420/4520 Rev. B4 Silicon Errata

The PIC18F2420/2520/4420/4520 Rev. B4 parts you have received conform functionally to the Device Data Sheet (DS39631**E**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2420/2520/4420/4520 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

**The following silicon errata apply only to PIC18F2420/2520/4420/4520 devices with these Device/Revision IDs**:

| Part Number | Device ID | Revision ID |
|---|---|---|
| PIC18F2420 | 0001 0001 010 | 0 0111 |
| PIC18F2520 | 0001 0001 000 | 0 0111 |
| PIC18F4420 | 0001 0000 110 | 0 0111 |
| PIC18F4520 | 0001 0000 100 | 0 0111 |

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F2420/2520/4420/4520 silicon.

## 1. Module: MSSP

In SPI Slave mode with slave select enabled (SSPM<3:0> = 0100), the minimum time between the falling edge of the $\overline{SS}$ pin and first SCK edge is greater than specified in parameter 70 in Table 26-16 and Table 26-17 of the above referenced data sheet.

The updated specification is shown in bold in Table 1.

**Work around**

None.

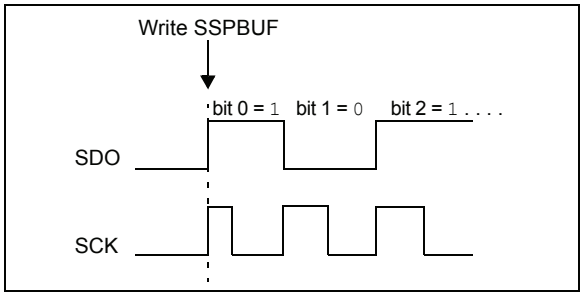
**Date Codes that pertain to this issue:**

All engineering and production devices.

## 2. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

**FIGURE 1: SCK PULSE VARIATION USING TIMER2/2**




**Work around**

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit and then turn Timer2 back on. Refer to Example 1 for sample code.

**EXAMPLE 1: AVOIDING THE INITIAL SHORT SCK PULSE**

```
LOOP BTFSS  SSPSTAT, BF     ;Data received?
                            ;(Xmit complete?)
     BRA    LOOP            ;No
     MOVF   SSPBUF, W       ;W = SSPBUF
     MOVWF  RXDATA          ;Save in user RAM
     MOVF   TXDATA, W       ;W = TXDATA
     BCF    T2CON, TMR2ON   ;Timer2 off
     CLRF   TMR2            ;Clear Timer2
     MOVWF  SSPBUF          ;Xmit New data
     BSF    T2CON, TMR2ON   ;Timer2 on
```

**Date Codes that pertain to this issue:**

All engineering and production devices.

**TABLE 1: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING)**

| Param No. | Symbol | Characteristic | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| 70 | TssL2scH, TssL2scL | $\overline{SS}$ ↓ to SCK ↓ or SCK ↑ Input | **3 TCY** | — | ns | |

### 3. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

One bit has been added to the BAUDCON register and one bit has been renamed. The added bit is RXDTP and is in the location, BAUDCON<5>. The renamed bit is the TXCKP bit (BAUDCON<4>), which had been named SCKP.

The TXCKP (BAUDCON<4>) and RXDTP (BAUDCON<5>) bits enable the TX and RX signals to be inverted (polarity reversed).

Register 18-3, on page 204, will be changed as shown.

**Work around**

None required.

**Date Codes that pertain to this issue:**

All engineering and production devices.

**REGISTER 18-3: BAUDCON: BAUD RATE CONTROL REGISTER**

| R/W-0 | R-1 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ABDOVF | RCIDL | RXDTP | TXCKP | BRG16 | — | WUE | ABDEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **ABDOVF**: Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL**: Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is Active

bit 5 **RXDTP**: Receive Data Polarity Select bit
Asynchronous mode:
1 = Receive data (RX) is inverted. Idle state is a low level.
0 = No inversion of receive data (RX). Idle state is a high level.
Synchronous mode:
1 = Data (DT) is inverted. Idle state is a low level.
0 = No inversion of data (DT). Idle state is a high level.

bit 4 **TXCKP**: Transmit/Clock Polarity Select bit
Asynchronous mode:
1 = Transmit data (TX) is inverted. Idle state is a low level.
0 = No inversion of transmit data (TX). Idle state is a high level.
Synchronous mode:
1 = Idle state for clock (CK) is a high level
0 = Idle state for clock (CK) is a low level

bit 3 **BRG16:** 16-bit Baud Rate Register Enable bit
1 = 16-bit Baud Rate Generator – SPBRGH and SPBRG
0 = 8-bit Baud Rate Generator – SPBRG only (Compatible mode); SPBRGH value ignored

bit 2 **Unimplemented:** Read as '0'

**REGISTER 18-3: BAUDCON: BAUD RATE CONTROL REGISTER (CONTINUED)**

bit 1 **WUE:** Wake-up Enable bit

Asynchronous mode:

1 = EUSART will continue to sample the RX pin with the interrupt generated on the falling edge; bit cleared in hardware on following rising edge

0 = RX pin is not monitored or rising edge detected

Synchronous mode:

Unused in this mode.

bit 0 **ABDEN**: Auto-Baud Detect Enable bit

Asynchronous mode:

1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.

0 = Baud rate measurement disabled or completed

Synchronous mode:

Unused in this mode.

### 4. Module: 10-Bit Analog-to-Digital Converter

When the AD clock source is selected as 2 TOSC or RC (when ADCS<2:0> = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

**Work around**

Select the AD clock source as 4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC or 64 TOSC and avoid selecting 2 TOSC or RC.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 5. Module: MSSP

With MSSP in SPI Master mode, FOSC/64 or Timer2/2 clock rate, and CKE = 0, a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required after the MSSP Interrupt Flag bit, SSPIF, is set or the Buffer Full bit, BF, is set and before writing SSPBUF. If the delay is insufficiently short, a write collision may occur as indicated by the WCOL bit being set.

**Work around**

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents. Verify the WCOL bit is clear after writing SSPBUF. If the WCOL is set, clear the bit in software and rewrite the SSPBUF register.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 6. Module: Enhanced Capture/Compare/ PWM (ECCP)

With the ECCP configured for Half-Bridge PWM mode (CCP1M<3:0> = 1110), the output may be corrupted for particular duty cycle selections. Affected duty cycle values are 0 though 3, and every subsequent increment of 4 (i.e., 7, 11, 15, 19, etc.).

**Work around**

None.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 7. Module: Resets (BOR)

An unexpected Reset may occur if the Brown-out Reset module (BOR) is disabled, and then re-enabled, when the High/Low-Voltage Detection module (HLVD) is not enabled (HLVDCON<4> = 0).

This issue affects BOR modes: BOREN<1:0> = 10 and BOREN<1:0> = 01. In both of these modes, if the BOR module is re-enabled while the device is active, unexpected Resets may be generated.

**Work around**

If BOR is required, and power consumption is not an issue, use BOREN<1:0> = 11. For BOREN<1:0> = 10 mode, either switch to BOREN<1:0> = 11 mode or enable the HLVD (HLVDCON<4> = 1) prior to entering Sleep.

If power consumption is an issue and low power is desired, Microchip does not recommend using BOREN<1:0> = 10 mode. Instead, use BOREN<1:0> = 01 and follow the steps below when entering and exiting Sleep.

1. Disable BOR by clearing SBOREN (RCON<6> = 0).
2. Enter Sleep mode (if desired).
3. After exiting Sleep mode, enable the HLVD (HLVDCON<4> = 1).
4. Wait for the internal reference voltage (TIRVST) to stabilize (typically 20 μs).
5. Re-enable BOR by setting SBOREN (RCON<6> = 1).
6. Disable the HLVD by clearing HLVDEN (HLVDCON<4> = 0).

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 8. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTA <7>, = 0)
- The EUSART is re-enabled (RCSTA <7> = 1)
- A two-cycle instruction is executed

**Work around**

Add a 2-TCY delay after re-enabling the EUSART.

1. Disable Receive Interrupts (RCIE bit, PIE1<5>, = 0).
2. Disable the EUSART (RCSTA <7>, = 0).
3. Re-enable the EUSART (RCSTA <7> = 1).
4. Re-enable Receive Interrupts (PIE1<5> = 1).

   (This is the first TCY delay.)
5. Execute a NOP instruction.

   (This is the second TCY delay.)

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 9. Module: Master Synchronous Serial Port (MSSP)

When configured for $I^2C$™ slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read after the SSPIF interrupt (PIR1<3>) has occurred, but before the first rising clock edge of the next byte being received.

**Work around**

The issue can be resolved in either of these ways:

- Prior to the $I^2C$ slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

**Date Codes that pertain to this issue:**

All engineering and production devices.

## REVISION HISTORY

Rev A Document (1/2008)
Initial release of this document. Includes silicon issues 1 (MSSP), 2 (MSSP – SPI Mode), 3 (Enhanced Universal Synchronous Receiver Transmitter – EUSART) and 4 (10-Bit Analog-to-Digital Converter).

Rev B Document (10/2008)
Added silicon issues 5 (MSSP), 6 (Enhanced Capture/Compare/PWM – ECCP) and 7 (Resets – BOR).

Rev C Document (8/2009)
Added silicon issues 8 (EUSART) and 9 (MSSP).

**NOTES:**

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