

# TLS810A1LDV33

## Ultra Low Quiescent Current Linear Voltage Regulator

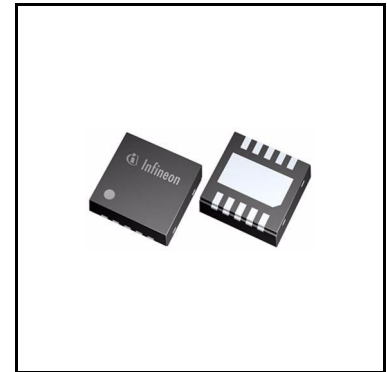


### 1 Overview

**Quality Requirement Category: Automotive**

#### Features

- Ultra Low Quiescent Current of 5  $\mu\text{A}$
- Wide Input Voltage Range of 2.75 V to 42 V
- Output Current Capacity up to 100 mA
- Low Drop Out Voltage of typ. 250 mV @ 100 mA
- Output Current Limit Protection
- Overtemperature Shutdown
- Available in PG-TSON-10 Package
- Wide Temperature Range
- Green Product (RoHS Compliant)
- AEC Qualified



#### Applications

- Applications with direct battery connection
- Automotive general ECUs
- Infotainment, alarm, dashboard
- RKE, immobilizer, gateway

#### Description

The TLS810A1 is a linear voltage regulator featuring wide input voltage range, low drop out voltage and ultra low quiescent current.

With an input voltage range of 2.75 V to 42 V and ultra low quiescent of only 5  $\mu\text{A}$ , the regulator is perfectly suitable for automotive or any other supply systems connected permanently to the battery.

The TLS810A1LDV33 is the fixed 3.3 V output version with an accuracy of 2 % and output current capability up to 100 mA.

The new regulation concept implemented in TLS810A1 combines fast regulation and very good stability while requiring only a small ceramic capacitor of 1  $\mu\text{F}$  at the output.

The tracking region starts already at input voltages of 2.75 V (extended operating range). This makes the TLS810A1 also suitable to supply automotive systems that need to operate during cranking condition.

# TLS810A1LDV33

## Ultra Low Quiescent Current Linear Voltage Regulator

---



### Overview

Internal protection features like output current limitation and overtemperature shutdown are implemented to protect the device against immediate damage due to failures like output short circuit to GND, over-current and over-temperature.

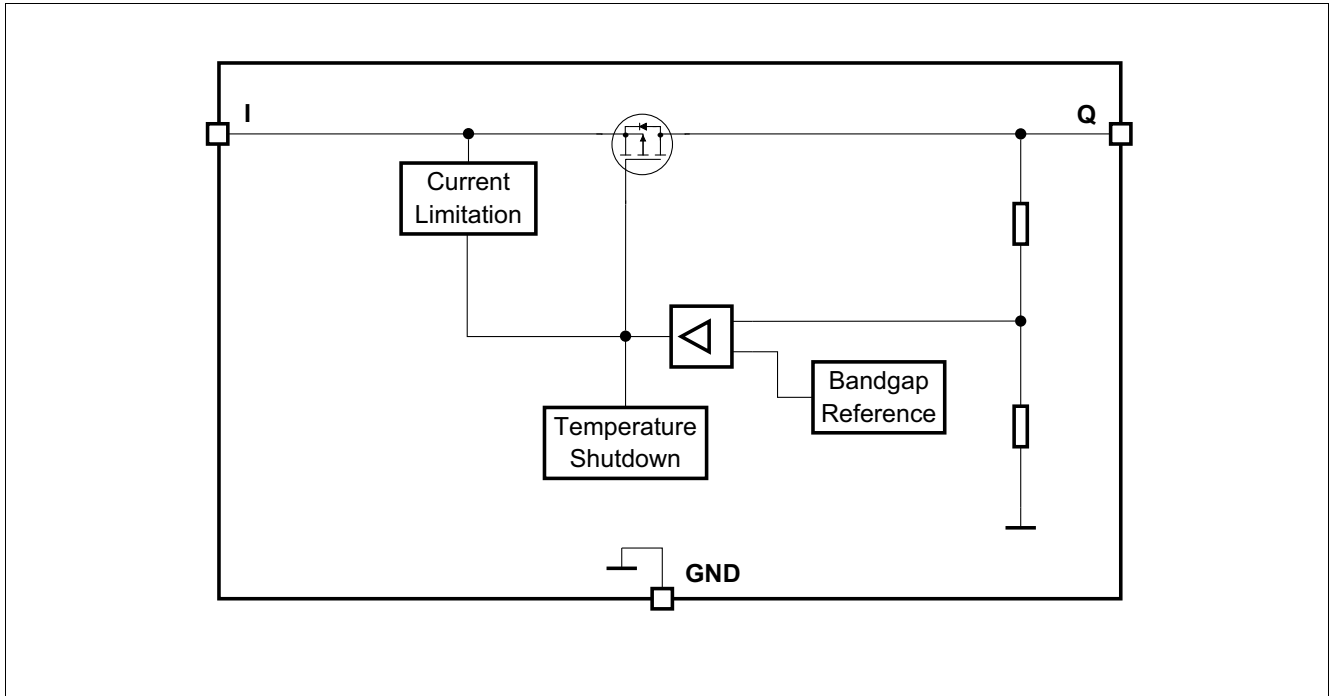
Type	Package	Marking
TLS810A1LDV33	PG-TSON-10	810A1V3

## Table of Contents

<b>1</b>	<b>Overview</b> .....	<b>1</b>
	<b>Table of Contents</b> .....	<b>3</b>
<b>2</b>	<b>Block Diagram</b> .....	<b>4</b>
<b>3</b>	<b>Pin Configuration</b> .....	<b>5</b>
3.1	Pin Assignment in PG-TSON-10 Package .....	5
3.2	Pin Definitions and Functions in PG-TSON-10 Package .....	5
<b>4</b>	<b>General Product Characteristics</b> .....	<b>6</b>
4.1	Absolute Maximum Ratings .....	6
4.2	Functional Range .....	7
4.3	Thermal Resistance .....	8
<b>5</b>	<b>Block Description and Electrical Characteristics</b> .....	<b>9</b>
5.1	Voltage Regulation .....	9
5.2	Typical Performance Characteristics Voltage Regulation .....	11
5.3	Current Consumption .....	14
5.4	Typical Performance Characteristics Current Consumption .....	15
<b>6</b>	<b>Application Information</b> .....	<b>16</b>
6.1	Application Diagram .....	16
6.2	Selection of External Components .....	16
6.2.1	Input Pin .....	16
6.2.2	Output Pin .....	16
6.3	Thermal Considerations .....	17
6.4	Reverse Polarity Protection .....	18
6.5	Further Application Information .....	18
<b>7</b>	<b>Package Outlines</b> .....	<b>19</b>
<b>8</b>	<b>Revision History</b> .....	<b>20</b>

**Block Diagram**

**2 Block Diagram**

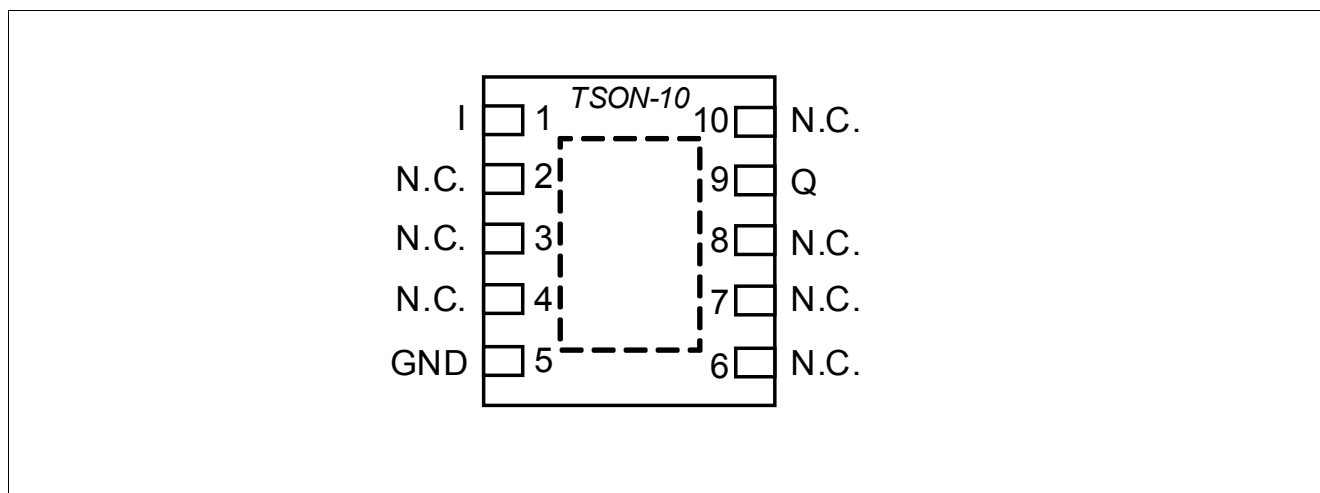


**Figure 1 Block Diagram TLS810A1**

**Pin Configuration**

### 3 Pin Configuration

#### 3.1 Pin Assignment in PG-TSON-10 Package



**Figure 2 Pin Configuration TLS805A1/TLS810A1 in PG-TSON-10 package**

#### 3.2 Pin Definitions and Functions in PG-TSON-10 Package

Pin	Symbol	Function
1	I	<b>Input</b> It is recommended to place a small ceramic capacitor (for example 100 nF) to GND, close to the IC terminals, in order to compensate line influences.
2	N.C.	<b>Not connected</b>
3	N.C.	<b>Not connected</b>
4	N.C.	<b>Not connected</b>
5	GND	<b>Ground</b>
6	N.C.	<b>Not connected</b>
7	N.C.	<b>Not connected</b>
8	N.C.	<b>Not connected</b>
9	Q	<b>Output</b> Connect an output capacitor $C_Q$ to GND close to the IC's terminals, respecting the values specified for its capacitance and ESR in <a href="#">Table 2 "Functional Range" on Page 7</a> .
10	N.C.	<b>Not connected</b>
Pad	-	<b>Exposed Pad</b> Connect to heatsink area. Connect to GND.

**General Product Characteristics**

**4 General Product Characteristics**

**4.1 Absolute Maximum Ratings**

**Table 1 Absolute Maximum Ratings<sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Voltage Input I</b>							
Voltage	$V_I$	-0.3	-	45	V	-	P_4.1.1
<b>Voltage Output Q</b>							
Voltage	$V_Q$	-0.3	-	7	V	-	P_4.1.2
<b>Temperatures</b>							
Junction Temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-	P_4.1.3
Storage Temperature	$T_{\text{stg}}$	-55	-	150	$^\circ\text{C}$	-	P_4.1.4
<b>ESD Absorption</b>							
ESD Susceptibility to GND	$V_{\text{ESD,HBM}}$	-2	-	2	kV	HBM <sup>2)</sup>	P_4.1.5
ESD Susceptibility to GND	$V_{\text{ESD,CDM}}$	-750	-	750	V	CDM <sup>3)</sup> at all pins	P_4.1.6

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 k $\Omega$ , 100 pF)

3) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

**Notes**

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

**General Product Characteristics**

**4.2 Functional Range**

**Table 2 Functional Range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage Range	$V_I$	$V_{Q,nom} + V_{dr}$	–	42	V	– <sup>1)</sup>	P_4.2.1
Extended Input Voltage Range	$V_{I,ext}$	2.75	–	42	V	– <sup>2)</sup>	P_4.2.2
Output Capacitor	$C_Q$	1	–	–	μF	– <sup>3)4)</sup>	P_4.2.3
Output Capacitor's ESR	$ESR(C_Q)$	–	–	100	Ω	– <sup>4)</sup>	P_4.2.4
Junction temperature	$T_j$	-40	–	150	°C	–	P_4.2.5

- 1) Output current is limited internally and depends on the input voltage, see Electrical Characteristics for more details.
- 2) When  $V_I$  is between  $V_{I,ext,min}$  and  $V_{Q,nom} + V_{dr}$ ,  $V_Q = V_I - V_{dr}$ . When  $V_I$  is below  $V_{I,ext,min}$ ,  $V_Q$  can drop down to 0 V.
- 3) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
- 4) Not subject to production testing, specified by design.

*Note:* Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

**General Product Characteristics**

**4.3 Thermal Resistance**

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 3 Thermal Resistance TLS810A1 in PG-TSON-10 Package<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	$R_{thJC}$	–	13	–	K/W	–	P_4.3.1
Junction to Ambient	$R_{thJA}$	–	60	–	K/W	2s2p board <sup>2)</sup>	P_4.3.2
Junction to Ambient	$R_{thJA}$	–	184	–	K/W	1s0p board, footprint only <sup>3)</sup>	P_4.3.3
Junction to Ambient	$R_{thJA}$	–	75	–	K/W	1s0p board, 300 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.4
Junction to Ambient	$R_{thJA}$	–	64	–	K/W	1s0p board, 600 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.5

- 1) Not subject to production test, specified by design
- 2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
- 3) Specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 1 copper layer (1 x 70µm Cu).



## 5 Block Description and Electrical Characteristics

### 5.1 Voltage Regulation

The output voltage  $V_Q$  is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and the pass transistor is driven accordingly.

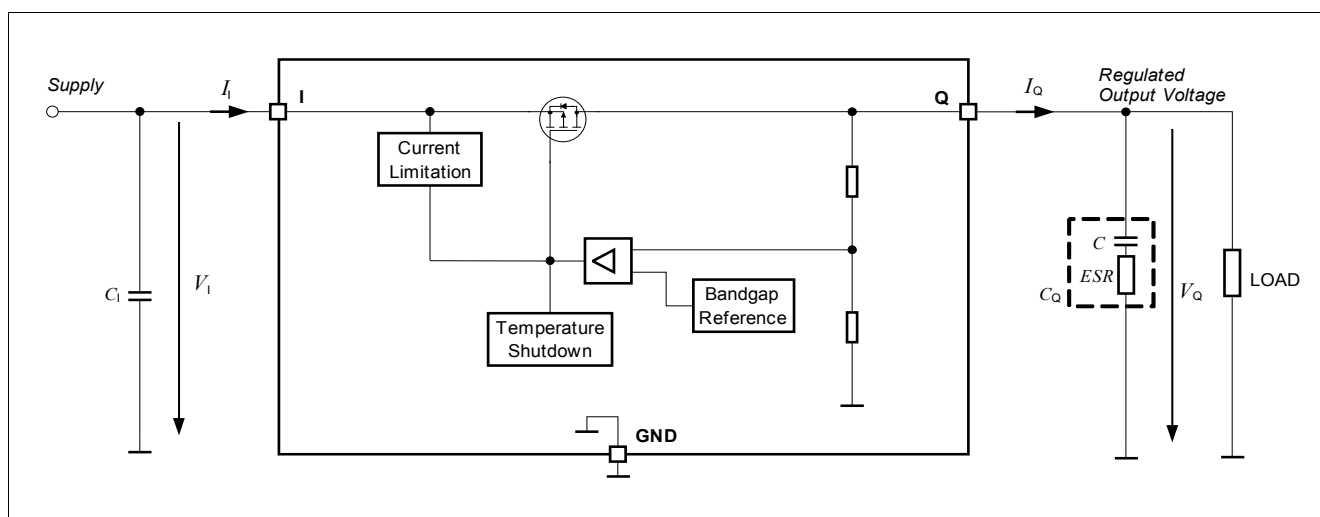
The control loop stability depends on the output capacitor  $C_Q$ , the load current, the chip temperature and the internal circuit structure. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in **“Functional Range” on Page 7** have to be maintained. For details see the typical performance graph **Output Capacitor Series Resistor ESR( $C_Q$ ) versus Output Current  $I_Q$**  on **Page 13**. Since the output capacitor is used to buffer load steps, it should be sized according to the application's needs.

An input capacitor  $C_I$  is not required for stability, but is recommended to compensate line fluctuations. An additional reverse polarity protection diode and a combination of several capacitors for filtering should be used, in case the input is connected directly to the battery line. Connect the capacitors close to the regulator terminals.

In order to prevent overshoots during start-up, a smooth ramping up function is implemented. This ensures almost no overshoots during start-up, mostly independent from load and output capacitance.

Whenever the load current exceeds the specified limit, for example in case of a short circuit, the output current is limited and the output voltage decreases.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (for example output continuously short-circuit) by switching off the power stage. After the chip has cooled down, the regulator restarts. This oscillatory thermal behaviour causes the junction temperature to exceed the maximum rating of 150°C and can significantly reduce the IC's lifetime.



**Figure 3 Block Diagram Voltage Regulation**

**Block Description and Electrical Characteristics**

**Table 4 Electrical Characteristics**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$ , all voltages with respect to ground (unless otherwise specified).  
 Typical values are given at  $T_j = 25^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$ .

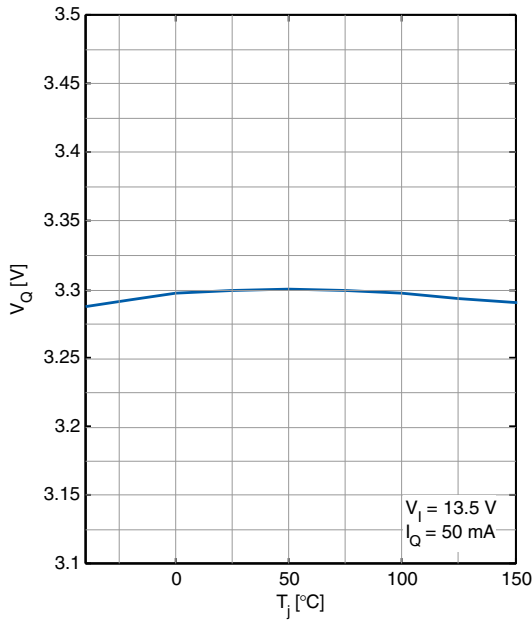
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage Precision	$V_Q$	3.23	3.30	3.37	V	$50\ \mu\text{A} \leq I_Q \leq 100\ \text{mA}$ , $4\ \text{V} \leq V_I \leq 28\ \text{V}$	P_5.1.1
Output Voltage Precision	$V_Q$	3.23	3.30	3.37	V	$50\ \mu\text{A} \leq I_Q \leq 50\ \text{mA}$ , $4\ \text{V} \leq V_I \leq 42\ \text{V}$	P_5.1.2
Output Current Limitation	$I_{Q,lim}$	110	190	260	mA	$0\ \text{V} \leq V_Q \leq V_{Q,nom} - 0.1\ \text{V}$	P_5.1.3
Line Regulation steady-state	$\Delta V_{Q,line}$	-	1	20	mV	$I_Q = 1\ \text{mA}$ , $6\ \text{V} \leq V_I \leq 32\ \text{V}$	P_5.1.4
Load Regulation steady-state	$\Delta V_{Q,load}$	-20	-1	-	mV	$V_I = 6\ \text{V}$ , $50\ \mu\text{A} \leq I_Q \leq 100\ \text{mA}$	P_5.1.5
Dropout Voltage <sup>1)</sup> $V_{dr} = V_I - V_Q$	$V_{dr}$	-	250	650	mV	$I_Q = 100\ \text{mA}$	P_5.1.6
Ripple Rejection <sup>2)</sup>	$PSRR$	-	60	-	dB	$I_Q = 50\ \text{mA}$ , $f_{ripple} = 100\ \text{Hz}$ , $V_{ripple} = 0.5\ V_{p-p}$	P_5.1.7
Overtemperature Shutdown Threshold <sup>2)</sup>	$T_{j,sd}$	151	175	-	$^\circ\text{C}$	$T_j$ increasing	P_5.1.8
Overtemperature Shutdown Threshold Hysteresis <sup>2)</sup>	$T_{j,sdh}$	-	10	-	K	$T_j$ decreasing	P_5.1.9

1) Measured when the output voltage  $V_Q$  has dropped 100 mV from the nominal value obtained at  $V_I = 13.5\text{V}$

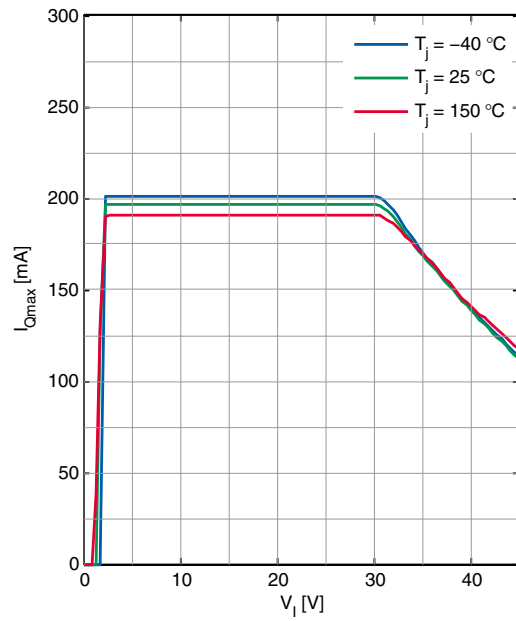
2) Not subject to production test, specified by design

**5.2 Typical Performance Characteristics Voltage Regulation**

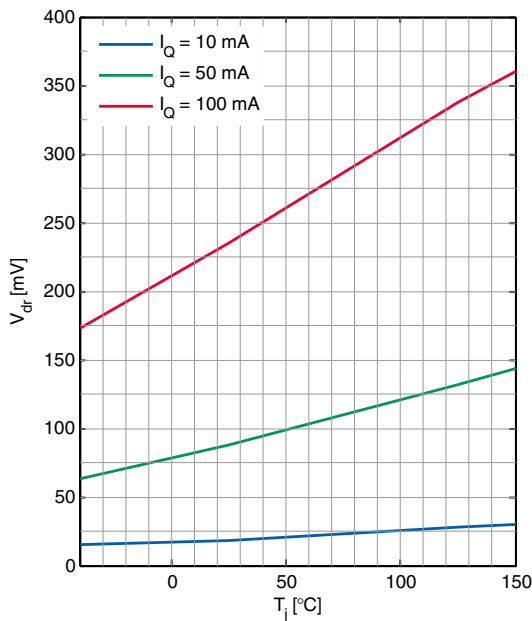
**Output Voltage  $V_Q$  versus Junction Temperature  $T_j$**



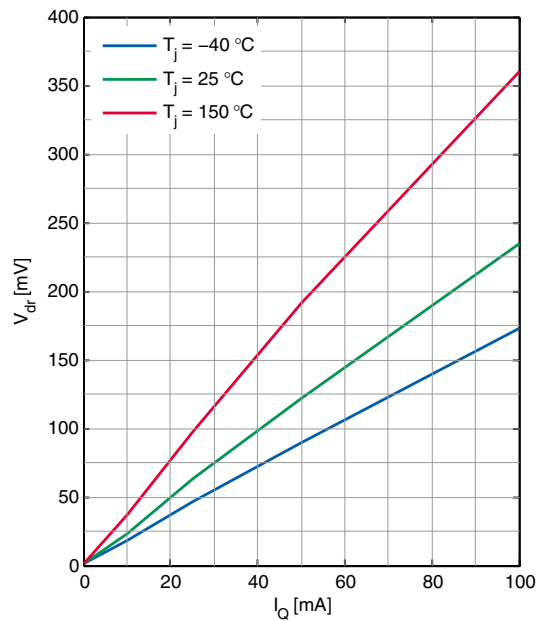
**Output Current  $I_Q$  versus Input Voltage  $V_I$**



**Dropout Voltage  $V_{dr}$  versus Junction Temperature  $T_j$**

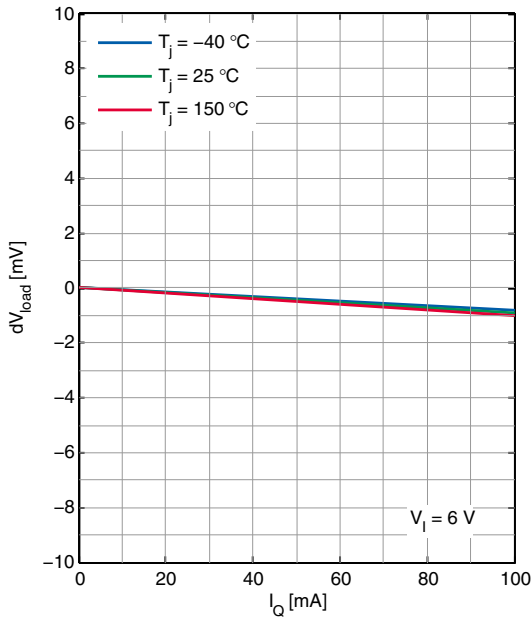


**Dropout Voltage  $V_{dr}$  versus Output Current  $I_Q$**

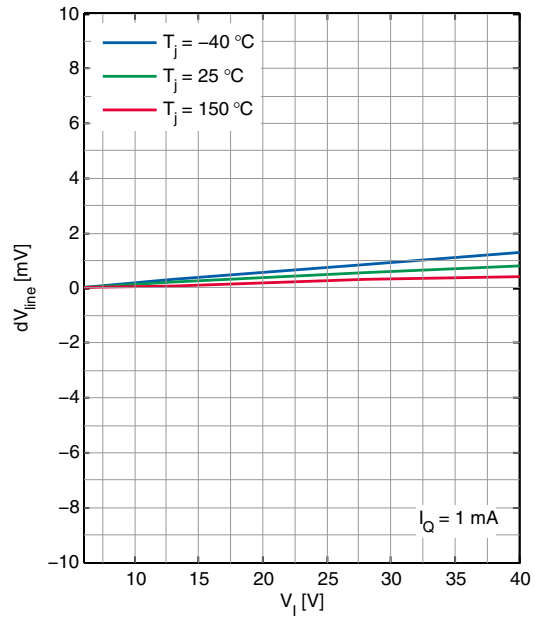


**Block Description and Electrical Characteristics**

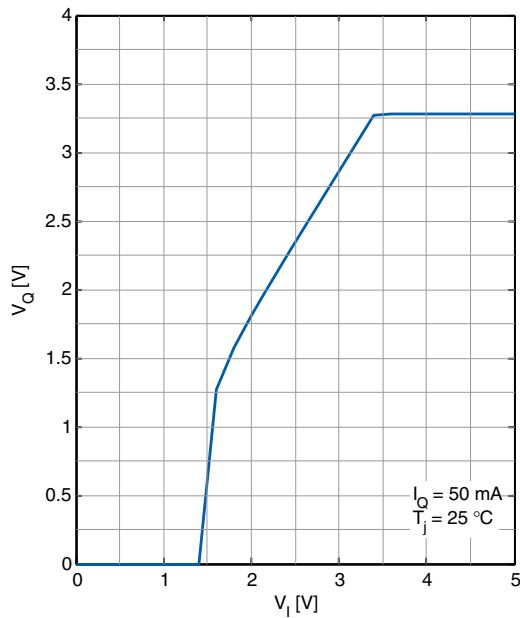
**Load Regulation  $dV_{Q,load}$  versus Output Current  $I_Q$**



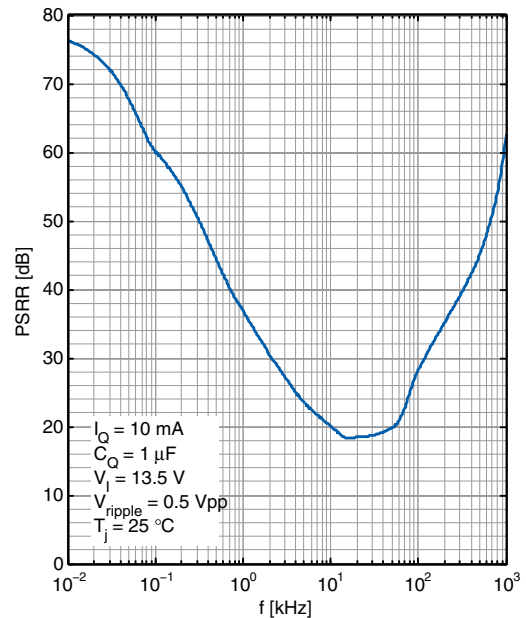
**Line Regulation  $dV_{Q,line}$  versus Input Voltage  $V_I$**



**Output Voltage  $V_Q$  versus Input Voltage  $V_I$**

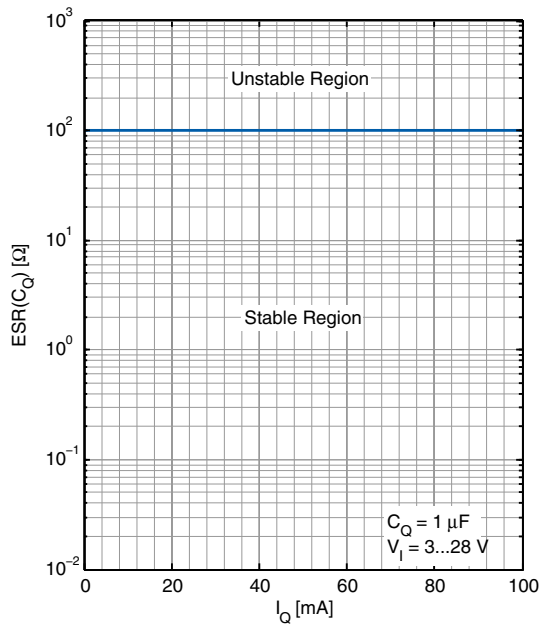


**Power Supply Ripple Rejection  $PSRR$  versus ripple frequency  $f_r$**



**Block Description and Electrical Characteristics**

**Output Capacitor Series Resistor  $ESR(C_Q)$  versus Output Current  $I_Q$**



**Block Description and Electrical Characteristics**

**5.3 Current Consumption**

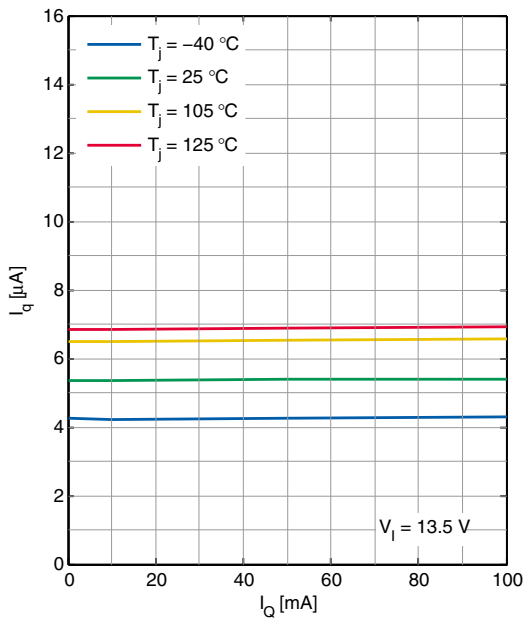
**Table 5 Electrical Characteristics Current Consumption**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$  (unless otherwise specified).

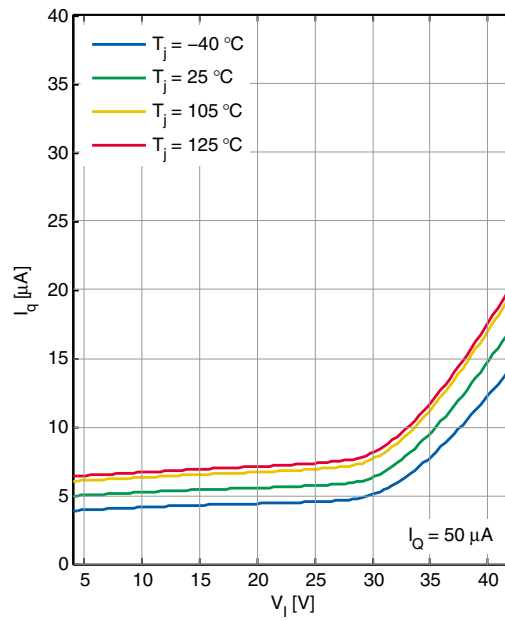
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption $I_q = I_I - I_Q$	$I_q$	–	5	7.5	$\mu\text{A}$	$I_Q = 50\ \mu\text{A}$ , $T_j = 25^\circ\text{C}$	P_5.3.1
Current Consumption $I_q = I_I - I_Q$	$I_q$	–	6	10	$\mu\text{A}$	$I_Q = 50\ \mu\text{A}$ , $T_j < 105^\circ\text{C}$	P_5.3.2
Current Consumption $I_q = I_I - I_Q$	$I_q$	–	6.5	11	$\mu\text{A}$	$I_Q = 50\ \mu\text{A}$ , $T_j < 125^\circ\text{C}$	P_5.3.3
Current Consumption $I_q = I_I - I_Q$	$I_q$	–	6.5	11	$\mu\text{A}$	$I_Q = 100\ \text{mA}$ , $T_j < 125^\circ\text{C}$	P_5.3.4

**5.4 Typical Performance Characteristics Current Consumption**

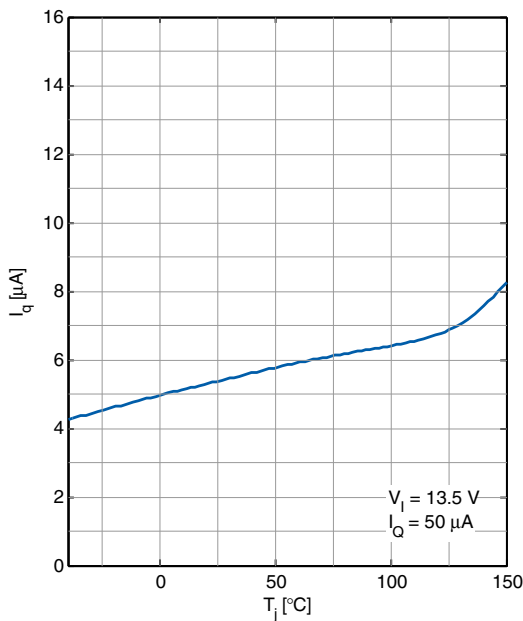
**Current Consumption  $I_q$  versus Output Current  $I_Q$**



**Current Consumption  $I_q$  versus Input Voltage  $V_I$**



**Current Consumption  $I_q$  versus Junction Temperature  $T_j$**

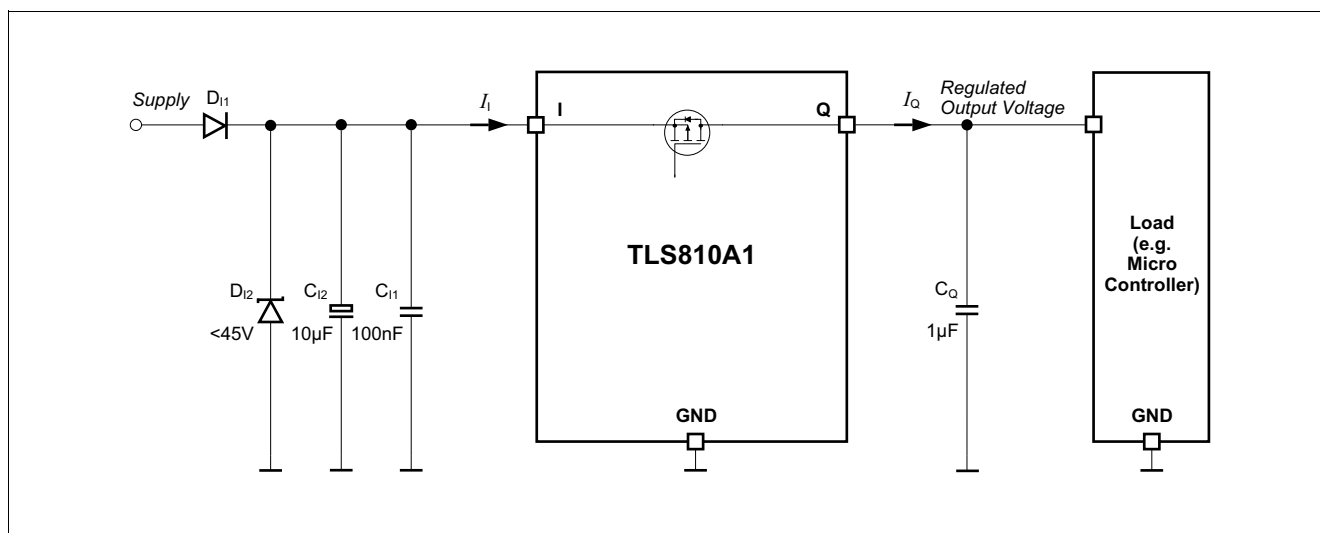


**Application Information**

**6 Application Information**

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

**6.1 Application Diagram**



**Figure 4 Application Diagram**

**6.2 Selection of External Components**

**6.2.1 Input Pin**

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line for example ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 μF to 470 μF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

**6.2.2 Output Pin**

An output capacitor is mandatory for the stability of linear voltage regulators.



## Application Information

The requirement to the output capacitor is given in “**Functional Range**” on Page 7. The graph **Output Capacitor Series Resistor ESR( $C_Q$ ) versus Output Current  $I_Q$**  on Page 13 shows the stable operation range of the device.

TLS810A1 is designed to be stable with extremely low ESR capacitors. According to the automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator’s output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

### 6.3 Thermal Considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (6.1)$$

with

- $P_D$ : continuous power dissipation
- $V_I$ : input voltage
- $V_Q$ : output voltage
- $I_Q$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  can then be calculated:

$$R_{thJA, max} = \frac{T_{j, max} - T_a}{P_D} \quad (6.2)$$

with

- $T_{j, max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in “**Thermal Resistance**” on Page 8.

### Example

Application conditions:

$$V_I = 13.5 \text{ V}$$

$$V_Q = 3.3 \text{ V}$$

$$I_Q = 70 \text{ mA}$$

$$T_a = 105^\circ\text{C}$$

Calculation of  $R_{thJA, max}$ :

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$$

$$= (13.5 \text{ V} - 3.3 \text{ V}) \times 70 \text{ mA} + 13.5 \text{ V} \times 0.011 \text{ mA}$$

## Application Information

$$= 0.714 \text{ W}$$

$$R_{\text{thJA,max}} = (T_{\text{j,max}} - T_{\text{a}}) / P_{\text{D}}$$

$$= (150^{\circ}\text{C} - 105^{\circ}\text{C}) / 0.714 \text{ W}$$

$$= 63.03 \text{ K/W}$$

As a result, the PCB design must ensure a thermal resistance  $R_{\text{thJA}}$  lower than 63.03 K/W. According to **“Thermal Resistance” on Page 8** only the FR4 2s2p board can be used.

### 6.4 Reverse Polarity Protection

TLS810A1 is not self protected against reverse polarity faults. To protect the device against negative supply voltage, an external reverse polarity diode is needed, as shown in **Figure 4Figure 32**. The absolute maximum ratings of the device as specified in **“Absolute Maximum Ratings” on Page 6** must be kept.

### 6.5 Further Application Information

- For further information you may contact <http://www.infineon.com/>



**Revision History**

## **8 Revision History**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.1	2016-12-20	Template updated
1.0	2016-09-21	Datasheet - Initial version

#### Trademarks of Infineon Technologies AG

$\mu$ HVIC™,  $\mu$ IPM™,  $\mu$ PFC™, AU-ConvertIR™, AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, CoolDP™, CoolGaN™, COOLiR™, CoolMOS™, CoolSET™, CoolSiC™, DAVE™, DI-POL™, DirectFET™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, GaNpowIR™, HEXFET™, HITFET™, HybridPACK™, iMOTION™, IRAM™, ISOFACE™, IsoPACK™, LEDriviR™, LITIX™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OPTIGA™, OptiMOS™, ORIGA™, PowIRaudio™, PowIRstage™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SIL™, RASIC™, REAL3™, SmartLEWIS™, SOLID FLASH™, SPOC™, StrongIRFET™, SupIRBuck™, TEMPFET™, TRENCHSTOP™, TriCore™, UHVIC™, XHP™, XMC™.

Trademarks updated November 2015

#### Other Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2016-12-20**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

**© 2016 Infineon Technologies AG.**

**All Rights Reserved.**

**Do you have a question about any aspect of this document?**

**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

#### IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

#### WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.