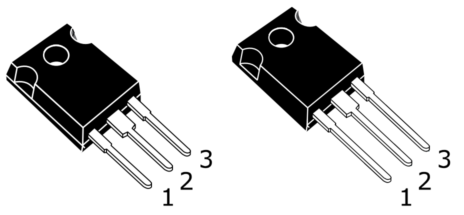
STW40N90K5, STWA40N90K5

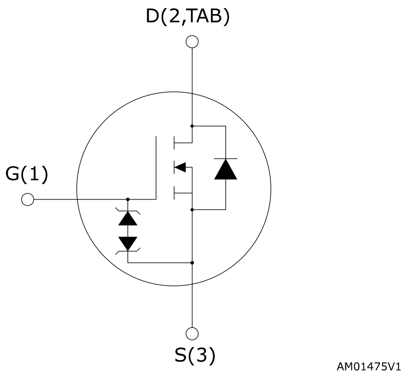
N-channel 900 V, 0.088 Ω typ., 40 A MDmesh™ K5 Power MOSFETs in TO-247 and TO-247 long leads packages

Datasheet - production data



TO-247 TO-247 long leads

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STW40N90K5	900 V	0.099 Ω	40 A
STWA40N90K5			

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STW40N90K5	40N90K5	TO-247	Tube
STWA40N90K5		TO-247 long leads	

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	40	A
I_D	Drain current (continuous) at T_C = 100 °C	25	A
I_D (1)	Drain current (pulsed)	160	A
P_{TOT}	Total dissipation at T_C = 25 °C	446	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1)Pulse width limited by safe operating area

(2)I_{SD} ≤ 40 A, di/dt ≤ 100 A/μs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS.}$, V_{DD}=450 V

(3)V_{DS} ≤ 720 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.28	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb	50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	13.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D= I_{AR}, V_{DD}= 50 V)	750	mJ

2 Electrical characteristics

(T_{case} =25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	900			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 900 V			1	µA
		V_{GS} = 0 V, V_{DS} = 900 V, T_C=125 °C(1)			50	µA
I_{GSS}	Gate-body leakage current	V_{DS}=0 V, V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 20 A		0.088	0.099	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS}=0 V, V_{DS} =100 V, f=1 MHz	-	3263	-	pF
C_{oss}	Output capacitance		-	212	-	pF
C_{rss}	Reverse transfer capacitance		-	1.3	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 V to 720 V	-	429	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	159	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	1.9	-	Ω
Q_g	Total gate charge	V_{DD} = 720 V, I_D = 40 A V_{GS} =10 V (see *Figure 15: "Test circuit for gate charge behavior"*)	-	89	-	nC
Q_{gs}	Gate-source charge		-	25	-	nC
Q_{gd}	Gate-drain charge		-	37.5	-	nC

Notes:

(1)Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

(2)energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 450 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Test circuit for resistive load switching times"*)	-	30.4	-	ns
t_r	Rise time		-	15.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	84.5	-	ns
t_f	Fall time		-	13.4	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		40	A
I_{SDM} (1)	Source-drain current (pulsed)		-		160	A
V_{SD} (2)	Forward on voltage	I_{SD} = 40 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 40 A, di/dt = 100 A/µs V_{DD}= 60 V (see *Figure 17: "Unclamped inductive load test circuit"*)	-	693		ns
Q_{rr}	Reverse recovery charge		-	22		µC
I_{RRM}	Reverse recovery current		-	63		A
t_{rr}	Reverse recovery time	I_{SD} = 40 A, di/dt = 100 A/µs V_{DD}= 60 V, T_J = 150 °C (see *Figure 17: "Unclamped inductive load test circuit"*)	-	884		ns
Q_{rr}	Reverse recovery charge		-	29		µC
I_{RRM}	Reverse recovery current		-	65.5		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

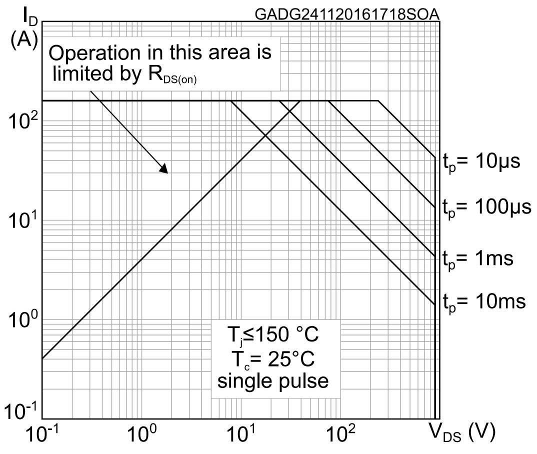


Figure 3: Thermal impedance

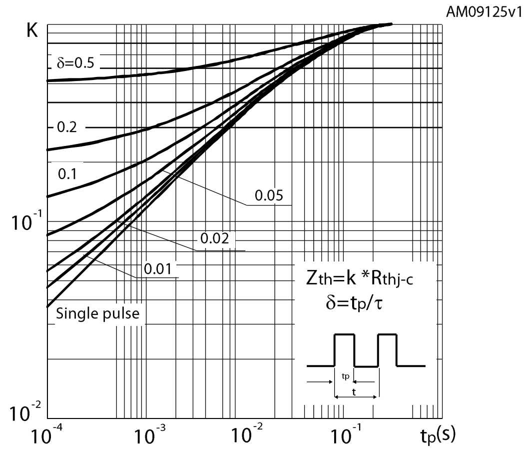


Figure 4: Output characteristics

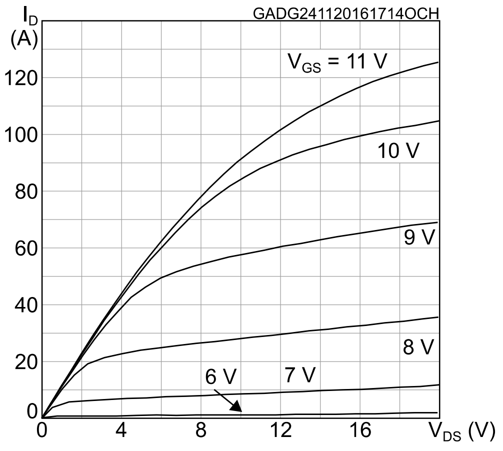


Figure 5: Transfer characteristics

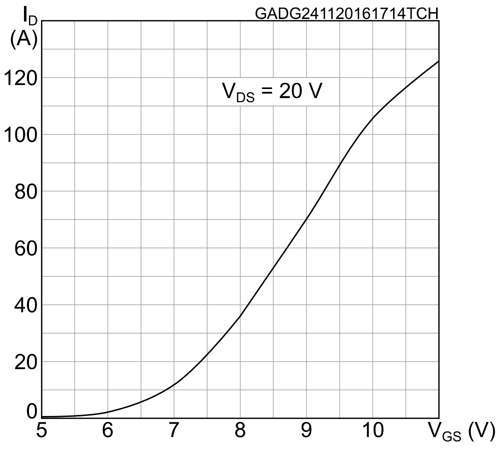


Figure 6: Gate charge vs gate-source voltage

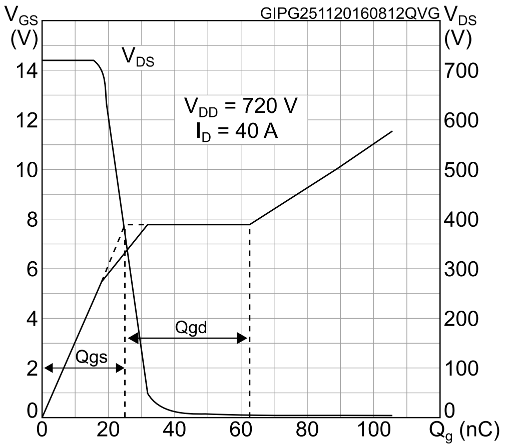


Figure 7: Static drain-source on-resistance

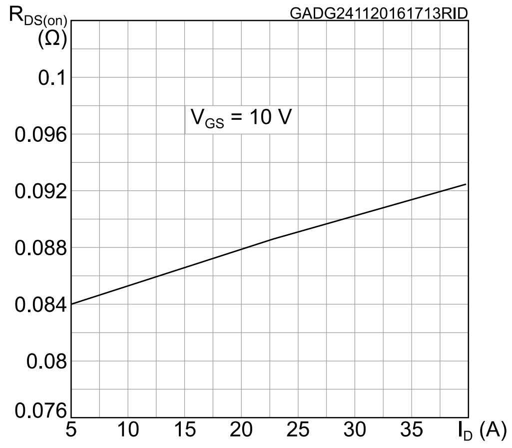


Figure 8: Capacitance variations

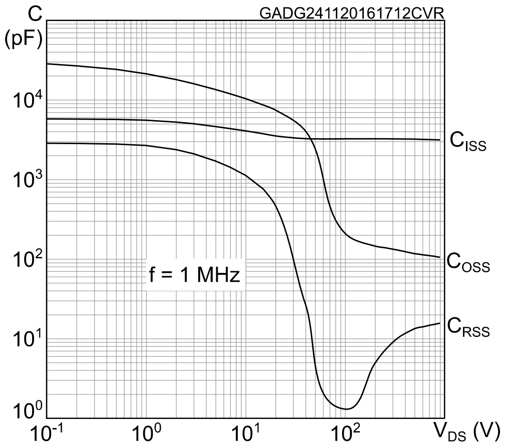


Figure 9: Normalized gate threshold voltage vs temperature

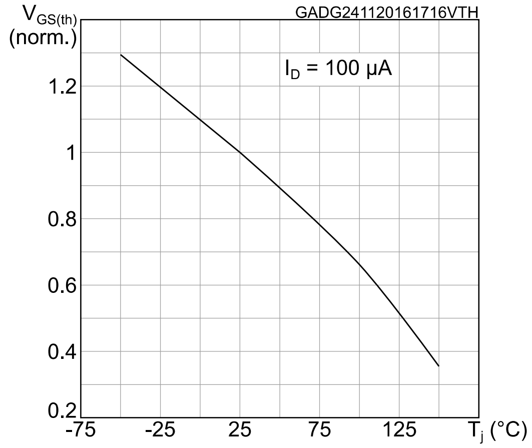


Figure 10: Normalized on-resistance vs temperature

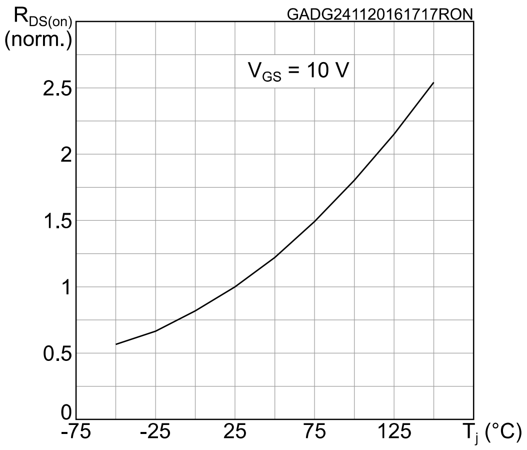


Figure 11: Normalized V(BR)DSS vs temperature

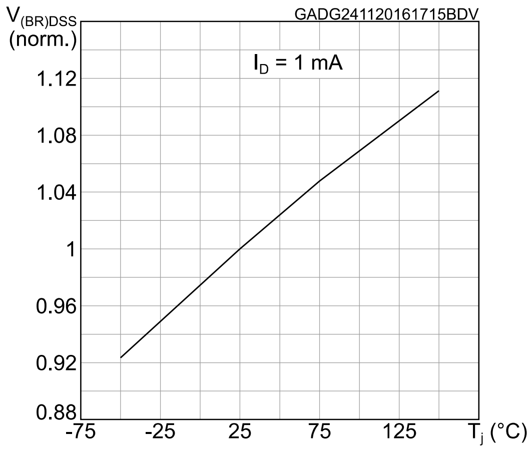


Figure 12: Source-drain diode forward characteristics

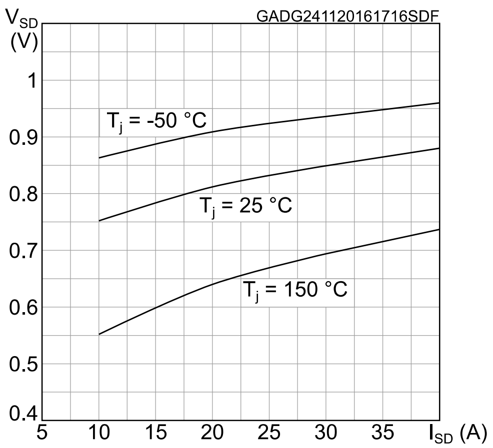
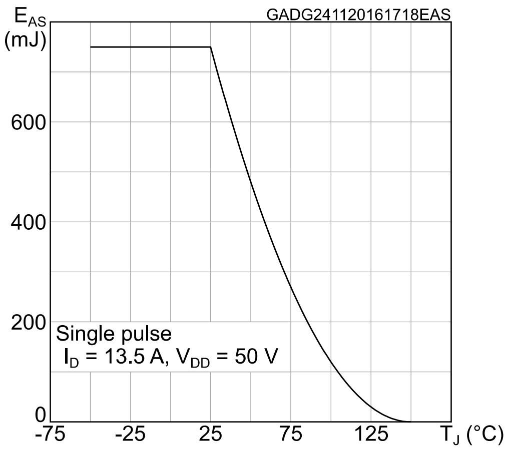


Figure 13: Maximum avalanche energy vs starting TJ



3 Test circuits

Figure 14: Test circuit for resistive load switching times

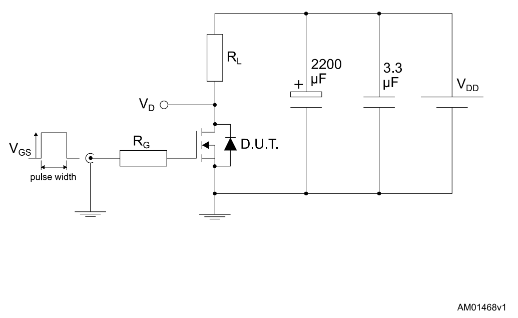


Figure 15: Test circuit for gate charge behavior

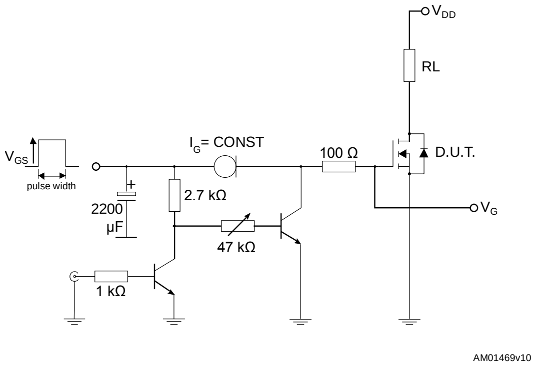


Figure 16: Test circuit for inductive load switching and diode recovery times

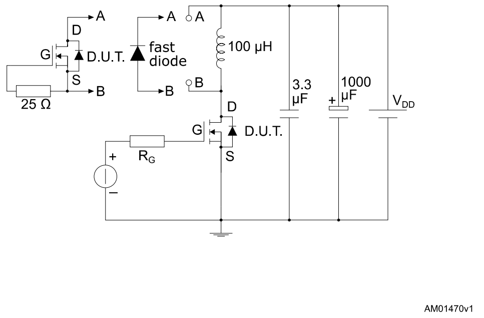


Figure 17: Unclamped inductive load test circuit

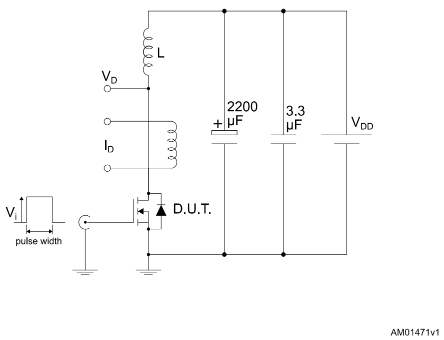


Figure 18: Unclamped inductive waveform

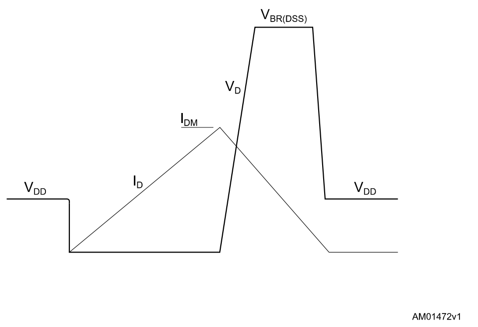
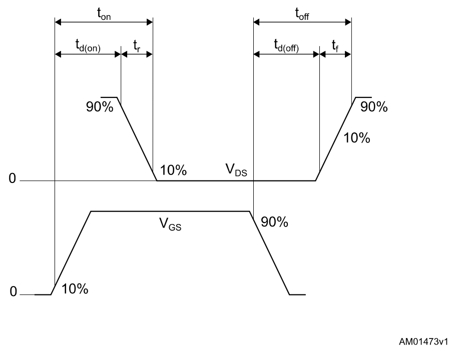


Figure 19: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 20: TO-247 package outline

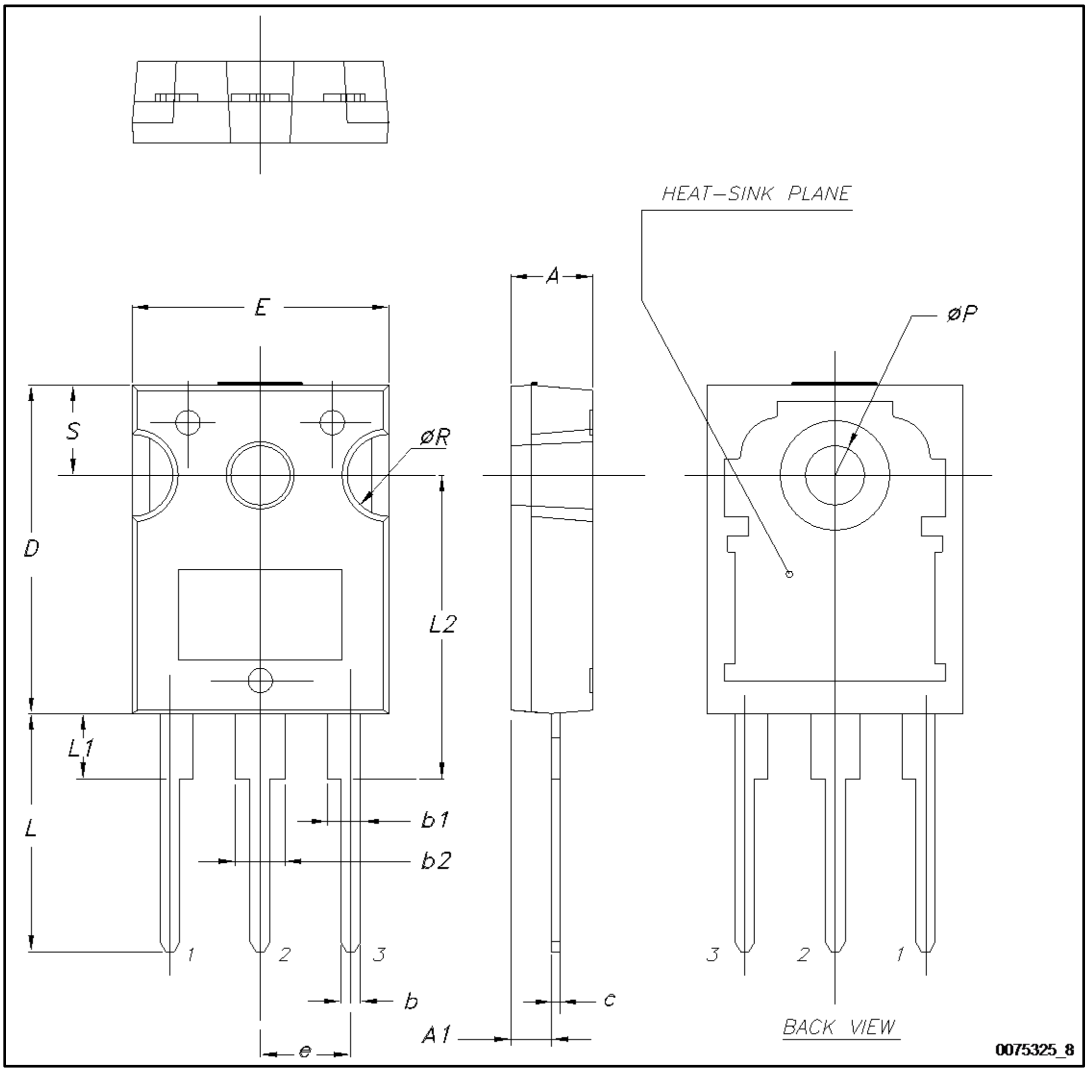


Table 10: TO-247 package mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

4.2 TO-247 long leads package information

Figure 21: TO-247 long lead package outline

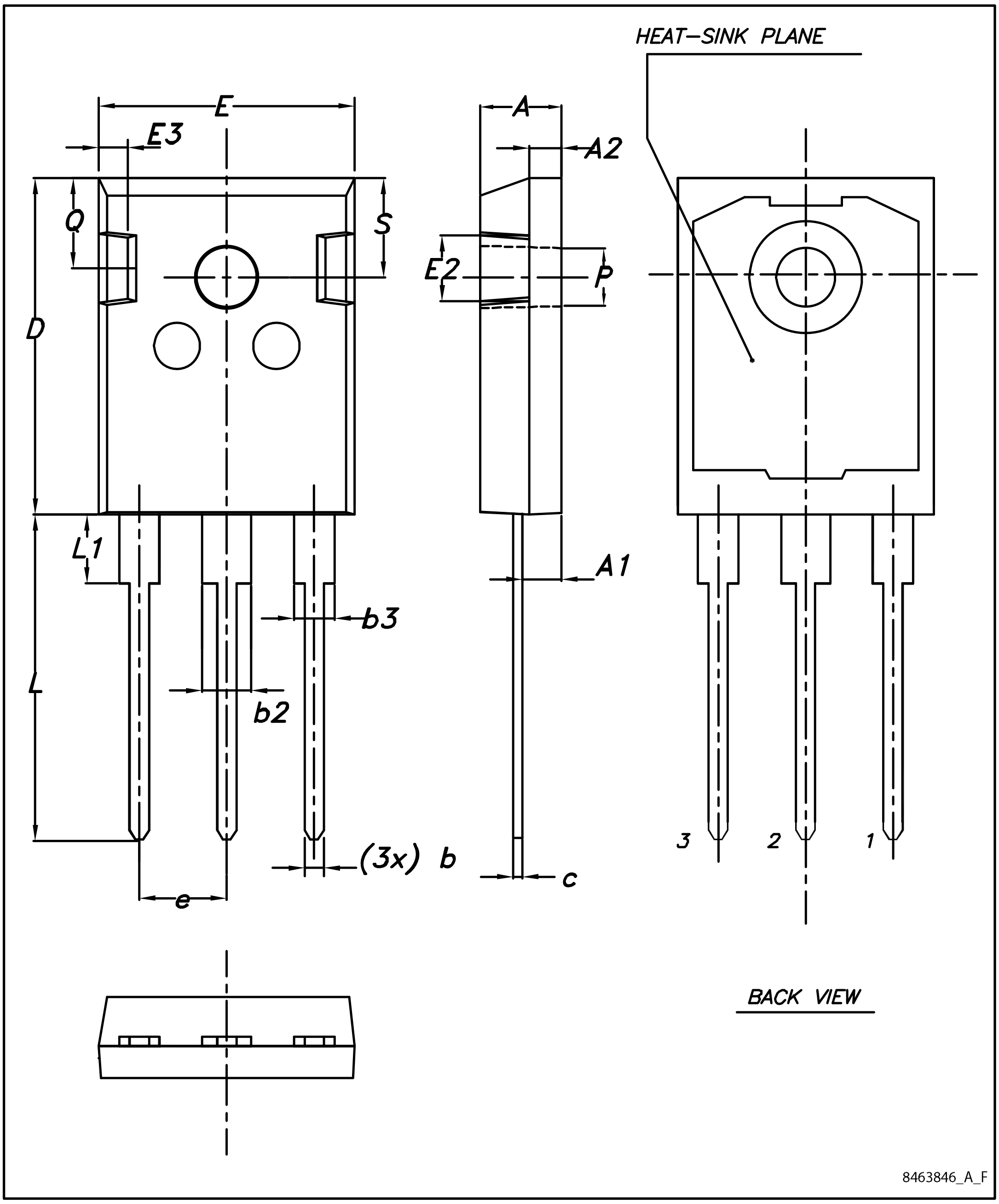


Table 11: TO-247 long lead package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
26-Jan-2016	1	First release.
25-Nov-2016	2	Updated *Section 1: "Electrical ratings"* and *Section 2: "Electrical characteristics"* Added *Section 2.1: "Electrical characteristics (curves)"*. Document status changed from preliminary to production data. Minor text changes.